



## N-Channel 20-V (D-S) 175° MOSFET

### CHARACTERISTICS

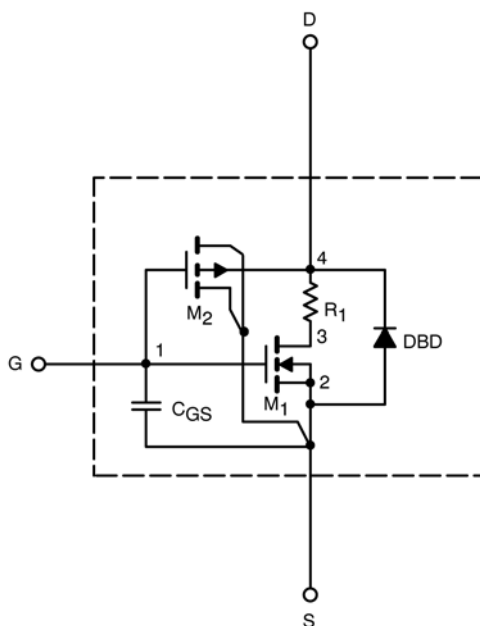
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



| SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED) |                     |                                                                                                                           |                |               |      |
|---------------------------------------------------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------|----------------|---------------|------|
| Parameter                                                     | Symbol              | Test Conditions                                                                                                           | Simulated Data | Measured Data | Unit |
| <b>Static</b>                                                 |                     |                                                                                                                           |                |               |      |
| Gate Threshold Voltage                                        | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA                                                               | 1.4            |               | V    |
| On-State Drain Current <sup>b</sup>                           | I <sub>D(on)</sub>  | V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V                                                                             | 964            |               | A    |
| Drain-Source On-State Resistance <sup>b</sup>                 | r <sub>DS(on)</sub> | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A                                                                             | 0.0041         | 0.0046        | Ω    |
|                                                               |                     | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125°C                                                     | 0.0057         |               |      |
|                                                               |                     | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A                                                                            | 0.0065         | 0.0073        |      |
| Forward Voltage <sup>b</sup>                                  | V <sub>SD</sub>     | I <sub>S</sub> = 50 A, V <sub>GS</sub> = 0 V                                                                              | 0.91           | 1.2           | V    |
| <b>Dynamic<sup>a</sup></b>                                    |                     |                                                                                                                           |                |               |      |
| Input Capacitance                                             | C <sub>iss</sub>    | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz                                                                  | 2418           | 2550          | pF   |
| Output Capacitance                                            | C <sub>oss</sub>    |                                                                                                                           | 816            | 900           |      |
| Reverse Transfer Capacitance                                  | C <sub>rss</sub>    |                                                                                                                           | 348            | 415           |      |
| Total Gate Charge <sup>c</sup>                                | Q <sub>g</sub>      | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A                                                    | 20             | 19            | nC   |
| Gate-Source Charge <sup>c</sup>                               | Q <sub>gs</sub>     |                                                                                                                           | 7.5            | 7.5           |      |
| Gate-Drain Charge <sup>c</sup>                                | Q <sub>gd</sub>     |                                                                                                                           | 6              | 6             |      |
| Turn-On Delay Time <sup>c</sup>                               | t <sub>d(on)</sub>  | V <sub>DD</sub> = 10 V, R <sub>L</sub> = 0.20 Ω<br>I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω | 11             | 11            | ns   |
| Rise Time <sup>c</sup>                                        | t <sub>r</sub>      |                                                                                                                           | 10             | 10            |      |
| Turn-Off Delay Time <sup>c</sup>                              | t <sub>d(off)</sub> |                                                                                                                           | 9              | 24            |      |
| Fall Time <sup>c</sup>                                        | t <sub>f</sub>      |                                                                                                                           | 9              | 9             |      |
| Source-Drain Reverse Recovery Time                            | t <sub>rr</sub>     | I <sub>F</sub> = 50 A, di/dt = 100 A/μs                                                                                   | 31             | 35            |      |

### Notes

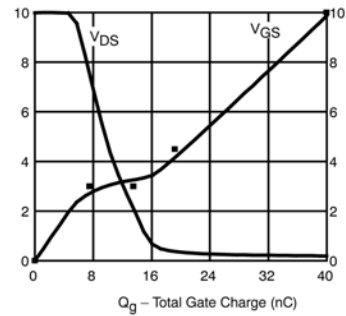
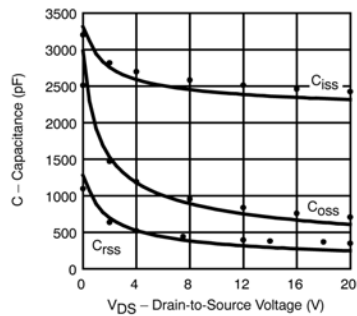
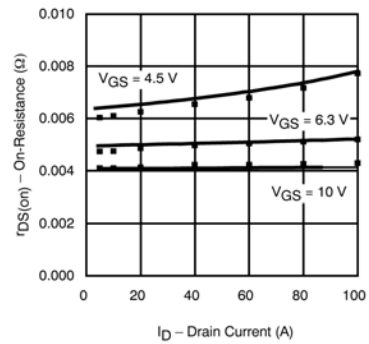
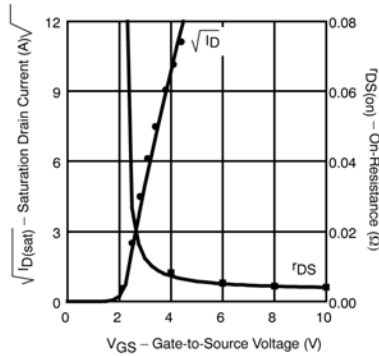
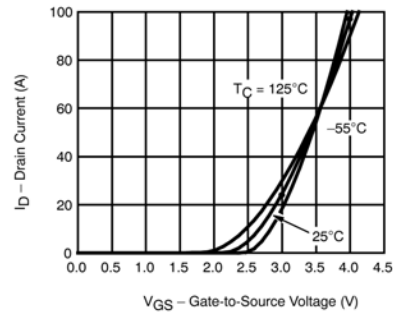
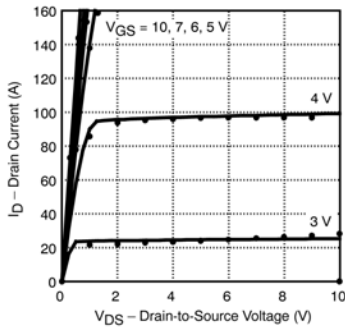
- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Independent of operating temperature.



# SPICE Device Model SUD50N02-06P

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.