



IGBT

TRENCHSTOP™ IGBT4 High Speed Chip

IGC18T120T8Q

Data Sheet

Industrial Power Control

Table of Contents

Features and Applications	3
Mechanical Parameters	3
Maximum Ratings	4
Static and Electrical Characteristics	4
Further Electrical Characteristics	5
Chip Drawing	6
Revision History	7
Relevant Application Notes	7
Legal Disclaimer	8

TRENCHSTOP™ IGBT4 High Speed Chip
Features:

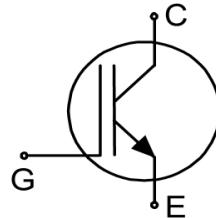
- 1200V trench & field stop technology
- Low switching losses
- Positive temperature coefficient
- Easy paralleling

Recommended for:

- Discrete components

Applications:

- High frequency drives
- Uninterruptible power supplies
- Welding
- Solar inverters



Chip Type	V_{CE}	I_{Cn} ¹	Die Size	Package
IGC18T120T8Q	1200V	15A	4.16mm x 4.34mm	Sawn on foil

Mechanical Parameters

Die size	4.16 x 4.34	
Emitter pad size	See chip drawing	
Gate pad size	1.185 x 0.702	
Area total	18.05	
Thickness	115	μm
Wafer size	200	mm
Maximum possible chips per wafer	1510	
Passivation frontside	Photoimide	
Pad metal	3200nm AlSiCu	
Backside metal	Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond	Electrically conductive epoxy glue and soft solder	
Wire bond	Al, $\leq 500\mu\text{m}$	
Reject ink dot size	$\varnothing 0.65\text{mm}$; max. 1.2mm	
Storage environment (<6 months)	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
	for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment.

¹ Nominal collector current at $T_C=100^\circ\text{C}$ for chip packaged in TO packages, see application example cited on page 5.

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}=25^{\circ}\text{C}$	V_{CE}	1200	V
DC collector current, limited by $T_{vj \text{ max}}^2$	I_C	-	A
Pulsed collector current, t_p limited by $T_{vj \text{ max}}^3$	$I_{C,\text{puls}}$	45	A
Gate-emitter voltage	V_{GE}	± 20	V
Virtual junction operating temperature	T_{vj}	-40 ... +175	$^{\circ}\text{C}$
Short circuit data ^{3/4} $V_{GE}=15\text{V}$, $V_{CC}=800\text{V}$, $T_{vj}=150^{\circ}\text{C}$	t_{sc}	10	μs

Static Characteristics (tested on wafer), $T_{vj}=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$, $I_C=0.5\text{mA}$	1200	-	-	V
Collector-emitter saturation voltage	V_{CESat}	$V_{GE}=15\text{V}$, $I_C=15\text{A}$	1.78	2.05	2.42	
Gate-emitter threshold voltage	$V_{GE(\text{th})}$	$I_C=0.5\text{mA}$, $V_{GE}=V_{CE}$	5.3	5.8	6.3	
Zero gate voltage collector current	I_{CES}	$V_{CE}=1200\text{V}$, $V_{GE}=0\text{V}$	-	-	2	
Gate-emitter leakage current	I_{GES}	$V_{CE}=0\text{V}$, $V_{GE}=20\text{V}$	-	-	120	nA
Integrated gate resistor	r_G		none			Ω

Electrical Characteristics ³

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter saturation voltage	V_{CESat}	$V_{GE}=15\text{V}$, $I_C=15\text{A}$, $T_{vj}=175^{\circ}\text{C}$	-	2.70	-	V
Input capacitance	C_{ies}	$V_{CE}=25\text{V}$, $V_{GE}=0\text{V}$, $f=1\text{MHz}$ $T_{vj}=25^{\circ}\text{C}$	-	875	-	pF
Reverse transfer capacitance	C_{res}		-	45	-	

² Depending on thermal properties of assembly.

³ Not subject to production test - verified by design/characterization.

⁴ Allowed number of short circuits: <1000; time between short circuits: >1s.

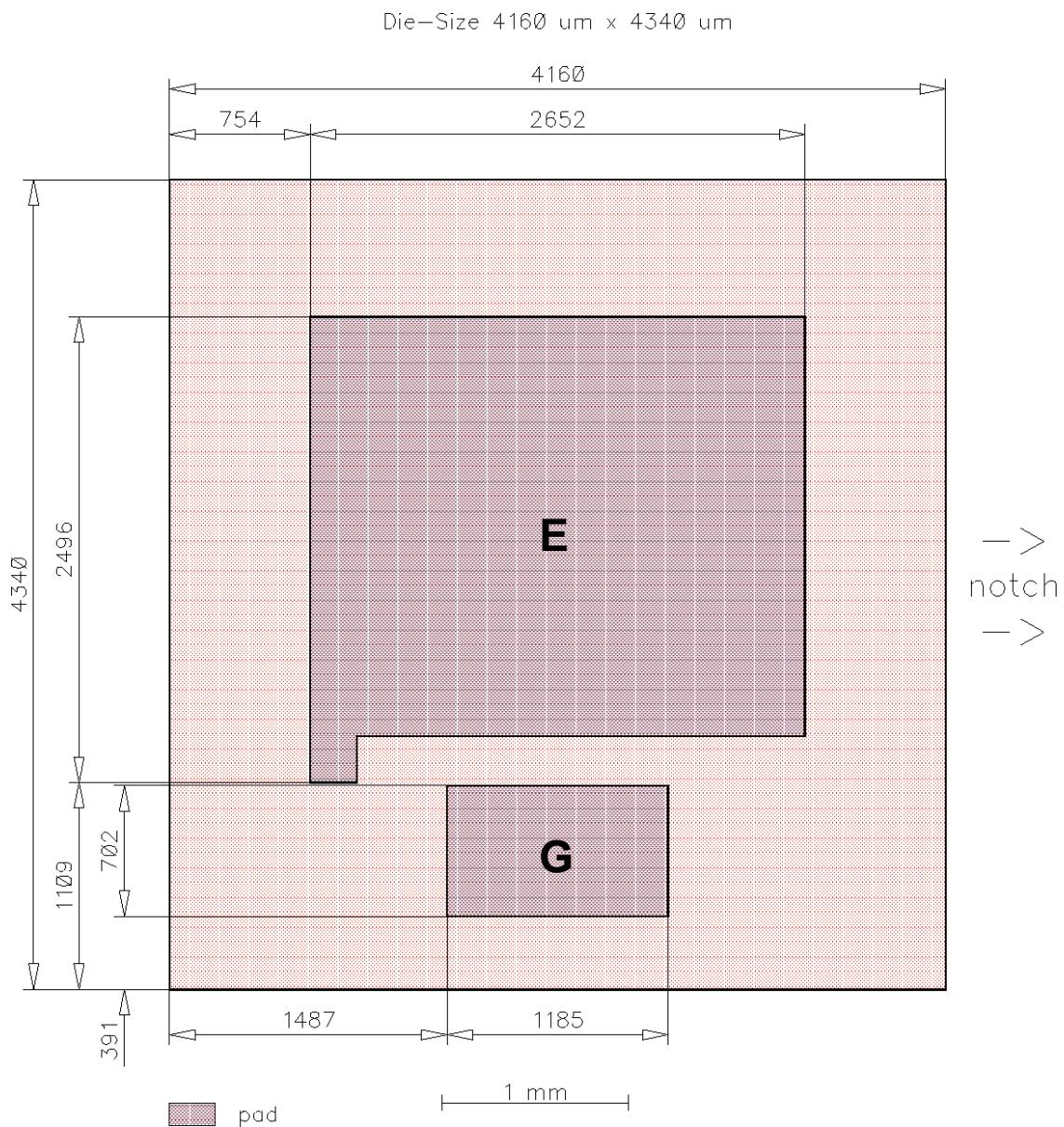


IGC18T120T8Q

Further Electrical Characteristics

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

Application example	IKW15N120H3	Rev. 1.2
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Chip Drawing

E = Emitter
G = Gate



IGC18T120T8Q

Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Description

AQL 0.65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Revision	Subjects (major changes since last revision)	Date
2.0	Final data sheet	13.10.2015

Relevant Application Notes

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