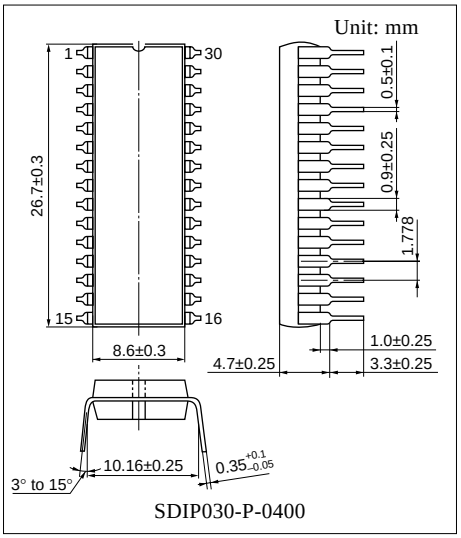
AN5295NK

3-ch. sound signal processing single chip IC for TV (with I²C bus)

■ Overview

The AN5295NK is a television-use 3-ch. sound signal processing IC which incorporates volume, tone control (L/R/C 3-ch.), and surround sound, sound AGC, lower sound enforce (L/R 2-ch.) functions. All of the functions (including changeover switch) including external I/O port can be controlled by I²C bus.



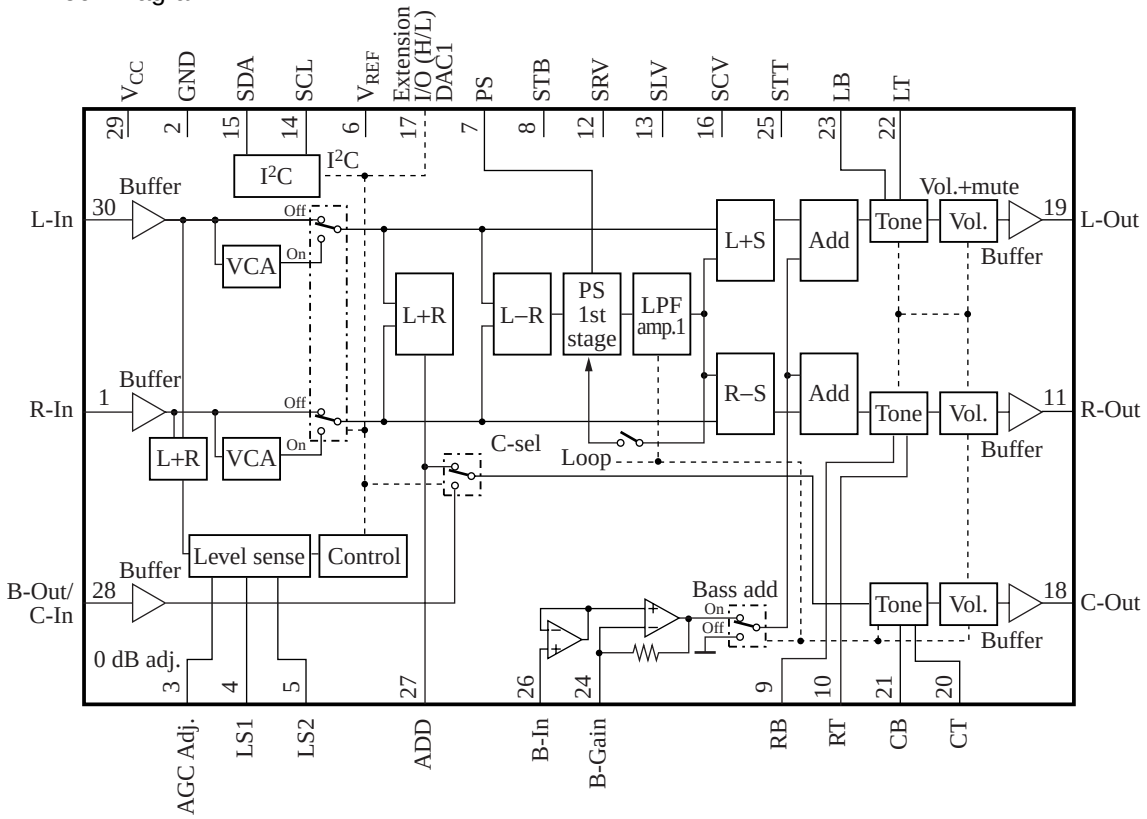
■ Features

- 3-ch. of volumes can be controlled independently (max. attenuation is 75 dB or more)
- Center output can be switched, ether center input or inside L+R signal (for HDTV)
- Lower sound enforce effect (frequency and gain) can be adjusted with external parts
- With L+R output

■ Applications

- Television

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	R-ch. input pin	16	C-ch. volume DAC output pin
2	Ground pin	17	Extension DAC pin 1
3	AGC 0 dB adjustment pin	18	C-ch. output pin
4	AGC level sensor-1 pin	19	L-ch. output pin
5	AGC level sensor-2 pin	20	C-ch. treble f_C setting pin
6	1/2 V_{CC} pin	21	C-ch. bass f_C setting pin
7	Phase shift pin	22	L-ch. treble f_C setting pin
8	L/R/C-ch. bass DAC output pin	23	L-ch. bass f_C setting pin
9	R-ch. bass f_C setting pin	24	Bass mix. gain adjustment pin
10	R-ch. treble f_C setting pin	25	L/R/C-ch. treble DAC output pin
11	R-ch. output pin	26	Bass detection LPF ope.-amp. input pin
12	R-ch. volume DAC output pin	27	L+R add after AGC output pin
13	L-ch. volume DAC output pin	28	C-ch. input pin
14	I^2C communication clock pin	29	Power supply pin (12 V)
15	I^2C communication data pin	30	L-ch. input pin

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	13.5	V
Supply current	I_{CC}	80	mA
Power dissipation *2	P_D	1 143	mW
Operating ambient temperature *1	T_{opr}	–20 to +75	°C
Storage temperature *1	T_{stg}	–55 to +150	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
∗2: T_a = 70 °C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	10.8 to 13.2	V

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Tone control						
Volume max. level *	$V_{VO\ (max)}$	V_{IN} = 1 V[rms], f = 1 kHz	–2.3	– 0.3	1.7	dB
Volume typ. level *	$V_{VO\ (typ)}$	V_{IN} = 1 V[rms], f = 1 kHz	–16.2	–13.2	–10.2	dB
Volume min. level *	$V_{VO\ (min)}$	V_{IN} = 1 V[rms], f = 1 kHz	—	—	–75	dB
Bass: boost level	V_{BB}	V_{IN} = 400 mV[rms], f = 50 Hz	9.2	11.2	13.2	dB
Bass: cut level	V_{BC}	V_{IN} = 400 mV[rms], f = 50 Hz	–11.7	–9.7	–7.7	dB
Treble: boost level	V_{TB}	V_{IN} = 400 mV[rms], f = 20 kHz	9.7	11.7	13.7	dB
Treble: cut level	V_{TC}	V_{IN} = 400 mV[rms], f = 20 kHz	–12.1	–10.1	–8.1	dB
AGC						
Input/output level 1 *	V_{AGC1}	V_{IN} = 1 mV[rms], f = 1 kHz	0.7	1.7	2.7	mV[rms]
Input/output level 2 *	V_{AGC2}	V_{IN} = 50 mV[rms], f = 1 kHz	70	110	150	mV[rms]
Input/output level 3 *	V_{AGC3}	V_{IN} = 1 V[rms], f = 1 kHz	275	345	415	mV[rms]
Circuit current *	I_{CC}	V_{IN} = 0 mV	25	45	65	mA
Total harmonics distortion *	THD	V_{IN} = 1 V[rms], f = 1 kHz	—	0.1	0.5	%
Max. input voltage *	$V_{IN\ (max)}$	THD = 1%	2.8	—	—	V[rms]
Mute level *	V_{MUTE}	V_{IN} = 1 V[rms], f = 1 kHz	—	—	–80	dB
Noise level at volume max. *	$V_{NO\ (max)}$	V_{IN} = 0 mV, R_g = 0 Ω	—	115	200	μV[rms]
Noise level at volume min. *	$V_{NO\ (min)}$	V_{IN} = 0 mV, R_g = 0 Ω	—	45	100	μV[rms]
Surround level (max.) *	$V_{SU\ (max)}$	V_{IN} = 100 mV[rms], f = 1 kHz	12.4	14.4	16.4	dB
Surround level (min.) *	$V_{SU\ (min)}$	V_{IN} = 100 mV[rms], f = 1 kHz	2.9	4.9	6.9	dB
Surround level at loop on *	V_{LPSUL}	V_{IN} = 100 mV[rms], f = 1 kHz	4.9	6.9	8.9	dB
Level at bass add on *	V_{BAONL}	V_{IN} = 400 mV[rms], f = 50 Hz	3.95	5.95	7.95	dB
Cross talk *	CT	V_{IN} = 1 V[rms], f = 1 kHz	—	–70	–68.5	dB
Channel balance *	CB	V_{IN} = 1 V[rms], f = 1 kHz	–1.5	0	1.5	dB
L–R volume tracking (1/4) *	V_{TR}	V_{IN} = 1 V[rms], f = 1 kHz	–2.0	0	2.0	dB
I^2C interface						
Sink current at ACK	I_{ACK}	Maximum value of pin 15 sink current at ACK	2.0	10	—	mA
SCL, SDA signal high-level input	V_{IHI}		3.5	—	5.0	V
SCL, SDA signal low-level input	V_{ILO}		0	—	0.9	V
Max. allowable input frequency	f_{Imax}		—	—	100	kbit/s

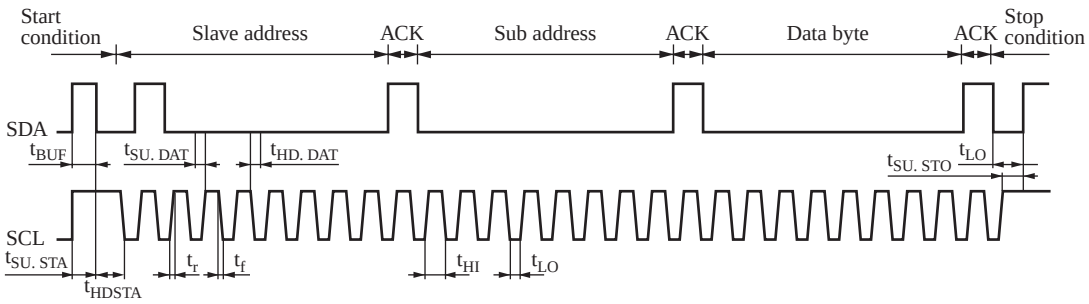
Note) * : Uses DIN audio filter.

■ Electrical Characteristics at T_a = 25°C (continued)

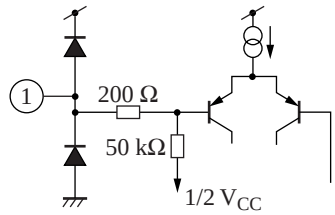
• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

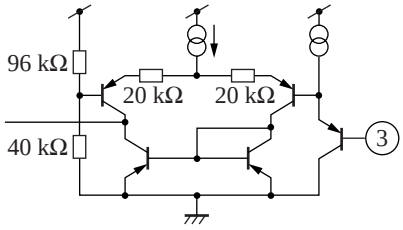
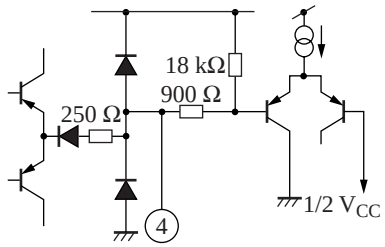
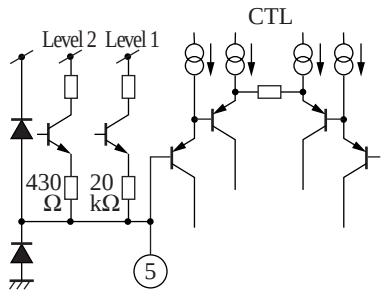
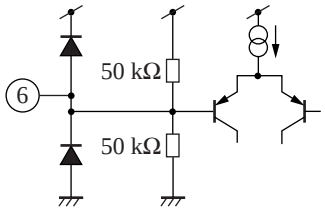
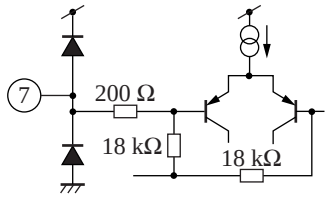
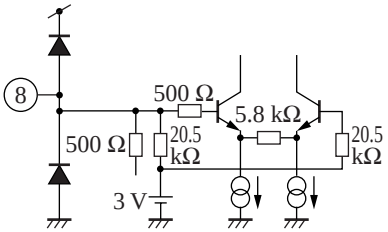
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C interface						
Bus free before start	t_{BUS}		4.0	—	—	µs
Start condition setup time	$t_{SU.\ STA}$		4.0	—	—	µs
Start condition hold time	$t_{HD.\ STA}$		4.0	—	—	µs
Low period SCL, SDA	t_{LO}		4.0	—	—	µs
High period SCL	t_{HI}		4.0	—	—	µs
Rise time SCL, SDA	t_r		—	—	1.0	µs
Fall time SCL, SDA	t_f		—	—	0.35	µs
Data setup time (write)	$t_{SU.\ DAT}$		0.25	—	—	µs
Data hold time (write)	$t_{HD.\ DAT}$		0	—	—	µs
Acknowledge setup time	$t_{SU.\ ACK}$		—	—	3.5	µs
Acknowledge hold time	$t_{HD.\ ACK}$		0	—	—	µs
Stop condition setup time	$t_{SU.\ STO}$		4.0	—	—	µs
DAC						
6-bit DAC DNLE	L_6	1 LSB = (data (max.) − data (00))/63	0.1	1.0	1.9	LSB/step



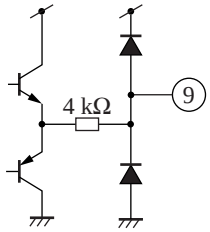
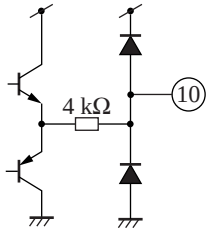
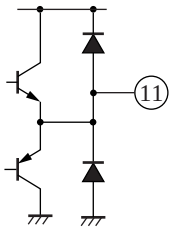
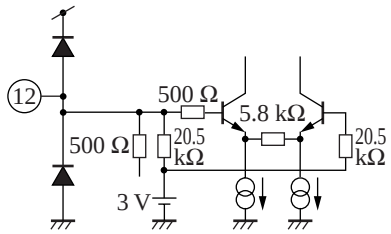
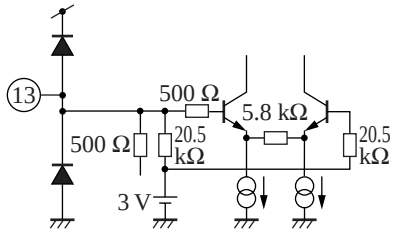
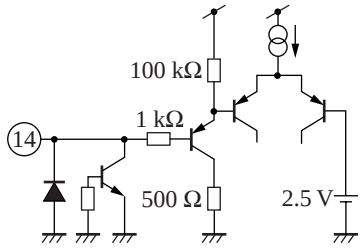
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage (V)
1		R-In: R-ch. Input pin	6
2	—	GND: GND pin	0

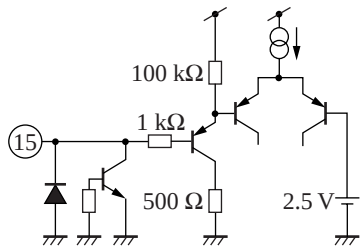
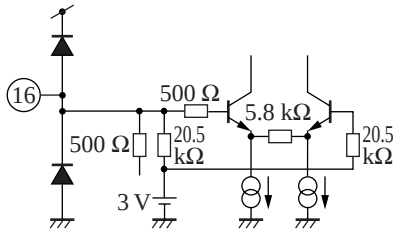
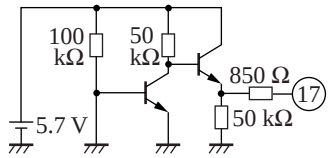
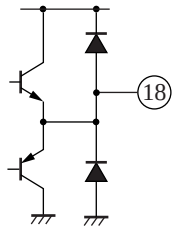
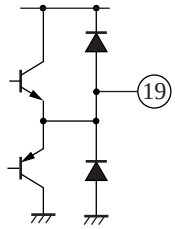
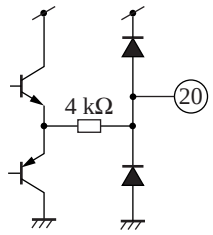
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
3		AGC Adj.: AGC on/off changeover AGC off at 1.2 V or less.	—
4		LS1: AGC level sensor 1	7
5		LS2: AGC level sensor 1, 2	0.5 to 1.5
6		V_{REF} : Reference voltage to be stabilized	6
7		PS: Phase shift pin	6
8		STB: L/R/C-ch. bass DAC output pin	3±1

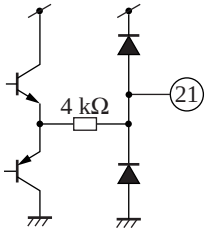
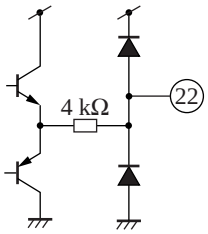
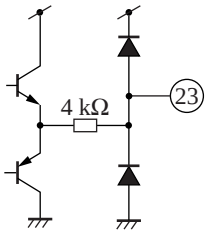
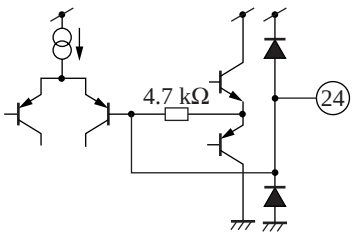
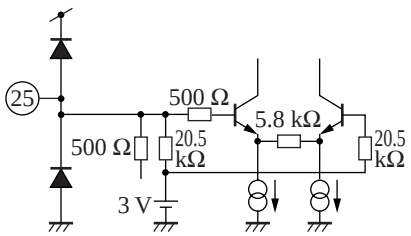
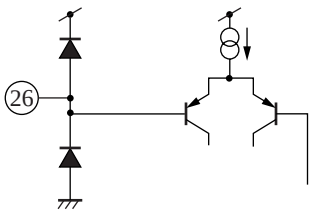
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
9		RB: R-ch. bass f_C setting pin	6
10		RT: R-ch. treble f_C setting pin	6
11		R-Out: R-ch. output pin	6
12		SRV: R-ch. volume DAC output pin	3±1
13		SLV: L-ch. volume DAC output pin	3±1
14		SCL: I^2C bus clock input pin	V_{CC}

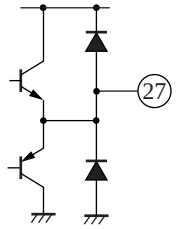
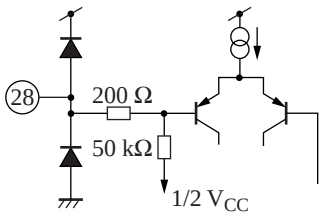
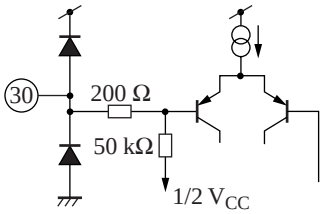
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
15		SDA: I²C bus data input pin	V_{CC}
16		SCV: C-ch. volume DAC output pin	3±1
17		DAC1: Extension DAC output pin	0 or 5
18		C-Out: C-ch. output pin	6
19		L-Out: L-ch. output pin	6
20		CT: C-ch. treble f_C setting pin	6

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
21		CB: C-ch. bass f_C setting pin	6
22		LT: L-ch. treble f_C setting pin	6
23		LB: L-ch. bass f_C setting pin	6
24		B-Gain: Bass mix. gain adjustment pin	6
25		STT: L/R/C-ch. treble DAC output pin	3±1
26		B-In: Bass detection LPF ope.-amp. input pin	6

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
27		ADD: L+R (after AGC) output pin	6
28		C-In: C-ch. input pin	6
29	—	V_{CC} : Power supply pin	12
30		L-In: L-ch. input pin	6

■ Technical Information

- I²C bus

1. DAC
   1) Built-in 5 DAC controls and 8 switches
   2) Incorporating auto-increment functions
      (1) Sub address 0* : Auto-increment mode
      (Data are inputted by the change of sub-address according to the transfer when data are sequentially transferred.)
      (2) Sub address 8* : Data renewal mode
      (Data are inputted with the same sub-address when data are sequentially transferred.)
   3) I²C bus protocol
      (1) Slave address: 10000000 (80H)
      (2) Format (normal)

S	Slave address	A	Sub address	A	Data byte	A	P

Start condition ↑ Acknowledge bit ↑ Stop condition ↑

      (3) Auto-increment mode/data renewal mode

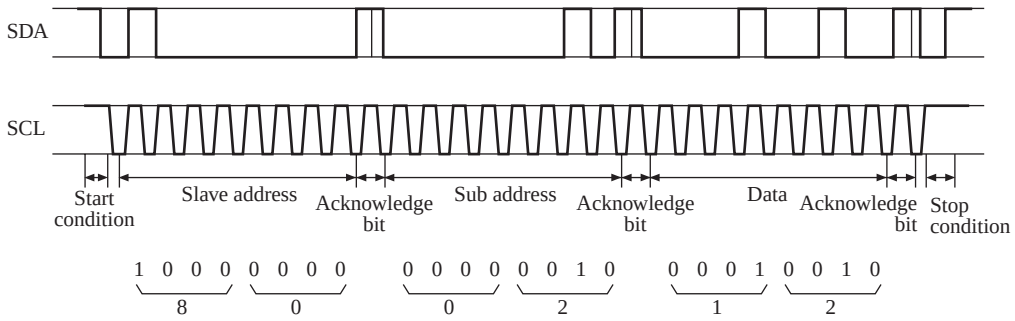
S	Slave address	A	Sub address	A	Data 1	A	Data 2	A	Data n	A	P

   4) Typical data should be inputted at power on because initial state of DAC is not guaranteed.

■ Technical Information (continued)

- I²C bus (continued)

2. I²C bus transfer sequence



Transfer message example

Two type of transfer messages of SCL and SDA are sent by synchronous serial transfer. SCL is a clock of constant frequency and SDA indicates address data to control receiving side and is sent in parallel by synchronizing with SCL. Data are transferred in principle with 8-bit 3 octet (byte) and acknowledge bit exists every one octet. Frame organization are described as follows:

1) Start condition — When SDA becomes low from high at SCA = high, receiver is on a data receiving mode.
2) Stop condition — When SDA becomes high from low at SCA = high, receiver stops receiving data.
3) Slave address — Address determined by device. Receiving is stopped when address of another device is sent.
4) Sub address — Address determined by function
5) Data — Data to control
6) Acknowledge bit — To let the master acknowledge that data has been received for each octet in such manner that the master sends a high signal and the receiver sends back a low signal as shown by above transfer sequence.

SDA is not changed when SCL is high except start and stop conditions.

3. Sub address byte and data byte format

Sub address	Upper MSB Data byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00	L-ch. vol.						Mute on/off	AGC on/off
01	R-ch. vol.						C-ch. mute on/off	Surround on/off
02	C-ch. vol.						Bass mix. on/off	C-In select
03	L/R/C treble				L/R/C bass			
04	0	0	0	0	0	0	0	0
05	Surround effect				Surround loop on/off	0	0	DAC1 L/H

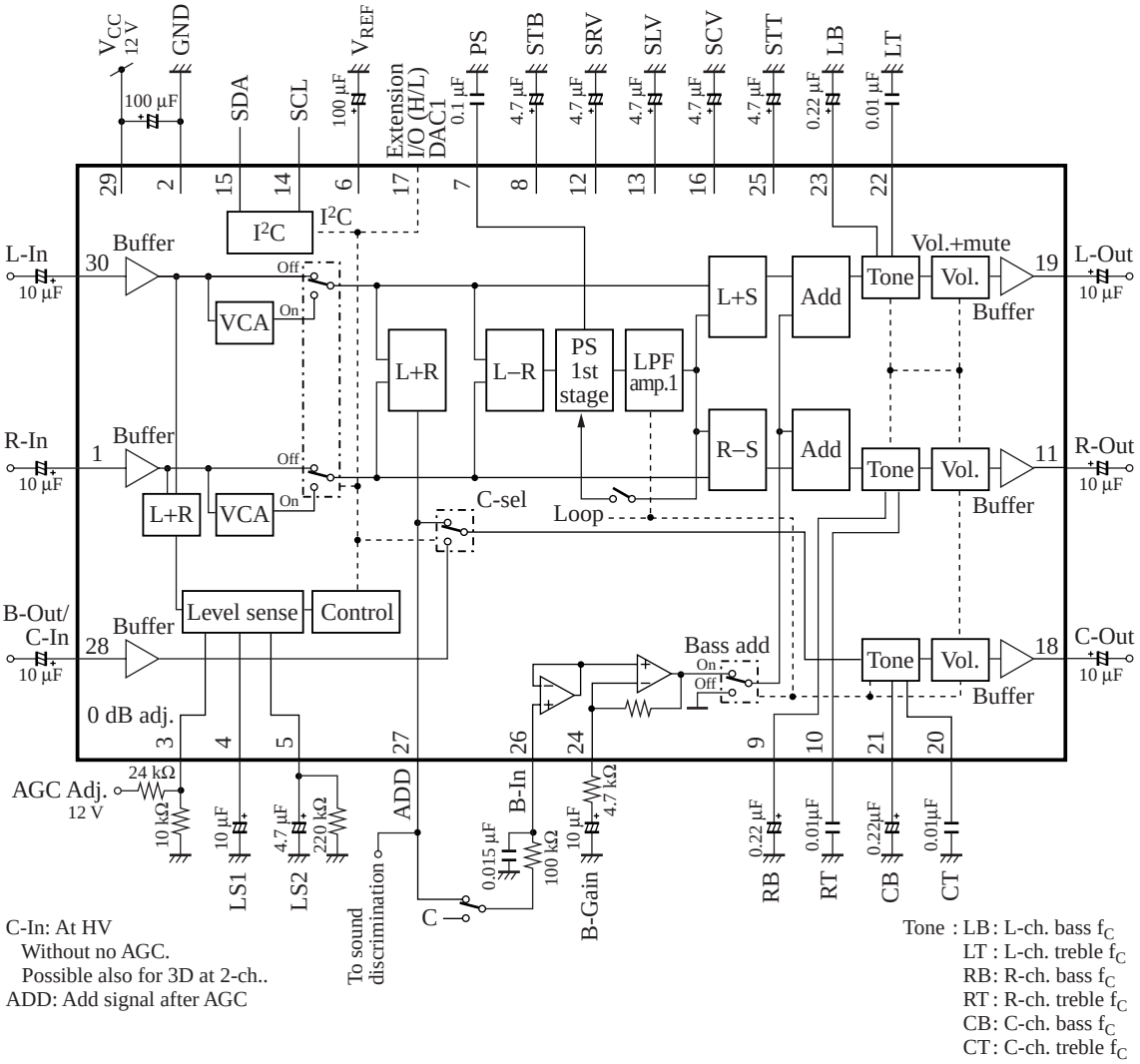
■ Technical Information (continued)

- I²C bus (continued)

3. Sub address byte and data byte format (continued)

1) L-ch. Vol., R-ch. Vol., C-ch. Vol.
   Min. at data = 00
   Max. at data = 3F
2) L/R/C treble, L/R/C bass
   Min. at data = 0
   Max. at data = F
3) Surround effect
   Min. at data = 0
   Max. at data = F
4) Switches (except C-ch. mute SW)
   Off at data = 0
   On at data = 1
5) DAC1
   Low (0 V) at data = 0
   High (5 V) at data = 1
6) C-In select
   L+R in at data = 0
   C-In at data = 1
7) C-ch. mute
   Off at data = 0
   On at data = 1

■ Application Circuit Example



C-In: At HV
Without no AGC.
Possible also for 3D at 2-ch..
ADD: Add signal after AGC

Tone : LB : L-ch. bass f_C
LT : L-ch. treble f_C
RB : R-ch. bass f_C
RT : R-ch. treble f_C
CB : C-ch. bass f_C
CT : C-ch. treble f_C

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