AsahiKASEI
ASAHI KASEI EMD

AK7742

24bit 2ch ADC + 24bit 4ch DAC with Audio DSP

GENERAL DESCRIPTION

The AK7742 is a highly integrated audio digital processor, including two stereo 24bit DAC's and one stereo ADC with input selector. The stereo DAC and ADC feature high performance, archiving 106dB and 96dB dynamic range respectively, 8kHz to 96kHz sampling rate are supported. The audio DSP has 1536step/fs parallel processing power, and 74k-bit delay memory allows surround processing, acoustic effect and parametric equalizers. As the AK7742 is a RAM based DSP, it is programmable for user requirements. The AK7742 is available in a space saving small 48pin LQFP package.

FEATURES

■ **DSP:**
- **Word length: 24bit (Data RAM 24bit floating point)**
- **Instruction cycle: 13.6 ns (1536step/fs fs=48kHz; 9216step/fs fs=8kHz)**
- **Multiplier 20 x 16 → 36bit (double precision available)**
- **Divider 20 / 20 → 20bit**
- **ALU: 40bit arithmetic operation (overflow margin 4bit) 24bit floating point arithmetic and logic operation**
- **Program RAM: 1536 x 36bit**
- **Coefficient RAM: 1536 x 16bit**
- **Data RAM: 1536 x 24-bit (24bit floating point)**
- **Delay RAM: 74kbit (3072 x 24bit)**
- **Sampling frequency: 8kHz ~ 96kHz**
- **Master / Slave operation**
- **Serial signal input port (4ch) MSB justified 24bit / LSB justified 24 / 20 / 16bit and I^2S**
- **Serial signal output port (6ch) MSB justified 24bit / LSB justified 24 / 16bit and I^2S**

■ **ADC: 2ch (stereo)**
- **24bit 64 x Over-sampling delta sigma (fs=8kHz~48kHz)**
- **DR, S/N: 96dB (fs=48kHz, fully differential input)**
- **S/(N+D): 84dB (fs=48kHz)**
- **Differential, Single-end Inputs**
- **Digital HPF (fc=1Hz)**
- **3:1 Analog input selector**
- **Digital Volume (24dB~-103dB, 0.5dB Step, Mute)**

■ **DAC: 4ch (two stereo pairs)**
- **24bit 128 x Over-sampling advanced multi-bit (fs=8kHz~96kHz)**
- **DR, S/N: 106dB**
- **S/(N+D): 92dB**
- **Differential output**
- **Digital Volume (12dB~-115dB, 0.5dB Step, Mute)**

■ **DSP Through Mode**

■ **I^2C BUS interface for micro-controller**

■ **Power supply: +3.3V ±0.3V, internal regulator for 1.8V**

■ **Operating temperature range: -20°C~70°C (AK7742EQ), -20°C~85°C (AK7742EN)**

■ **Package: 48pin LQFP, 0.5mm pitch (AK7742EQ)**
48pin QFN, 0.4mm pitch (AK7742EN)

■ Block Diagram

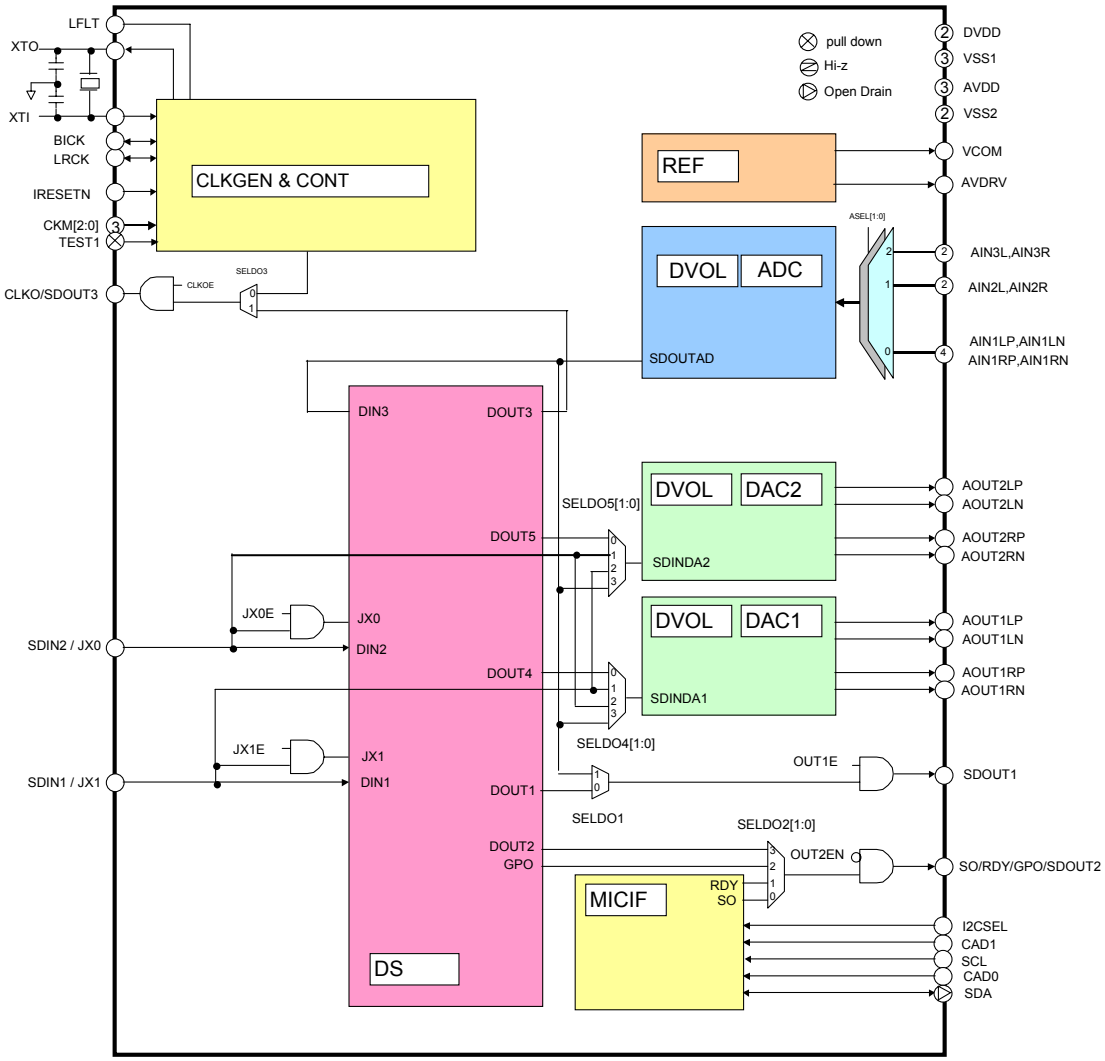


Figure 1. Block Diagram

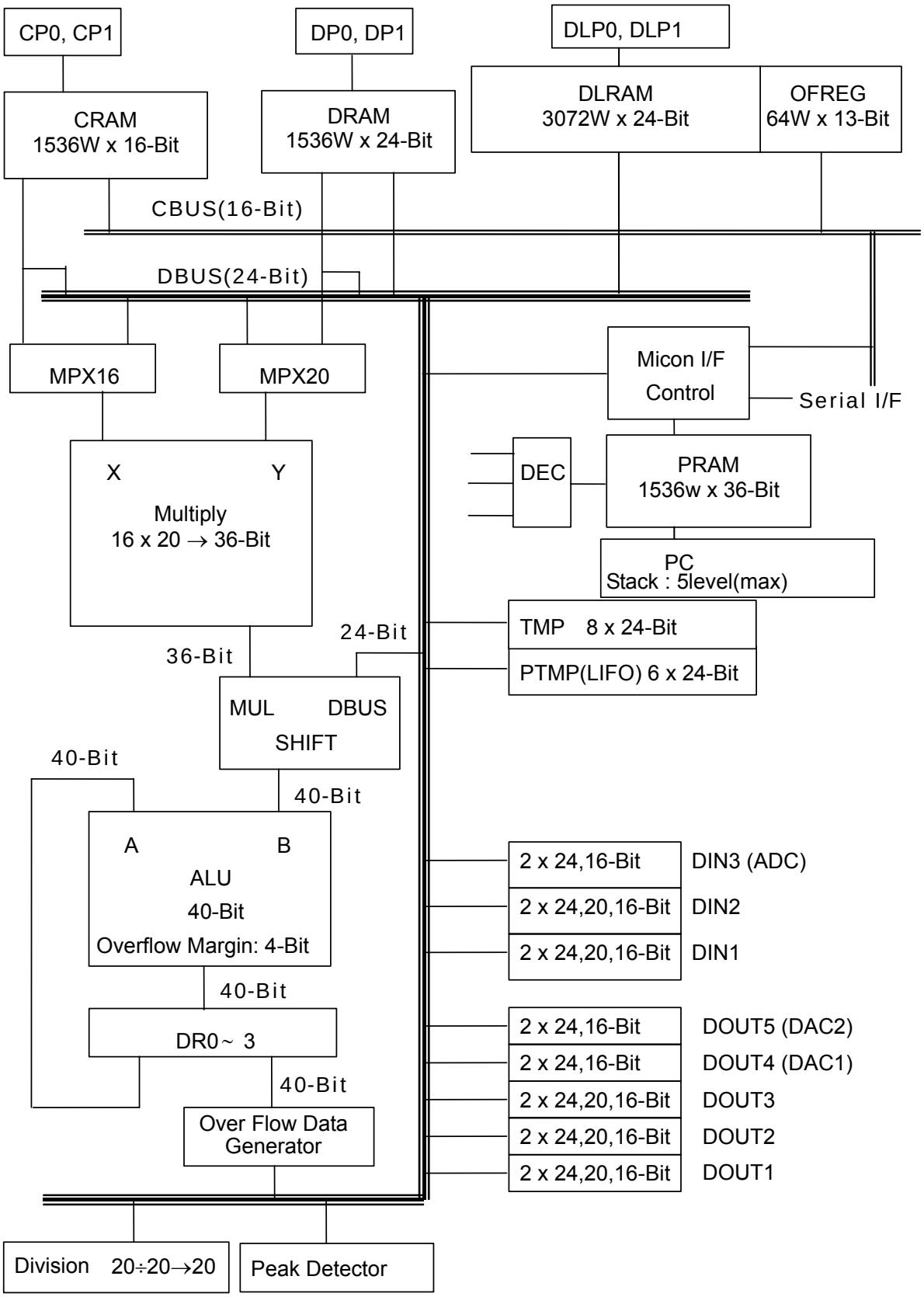


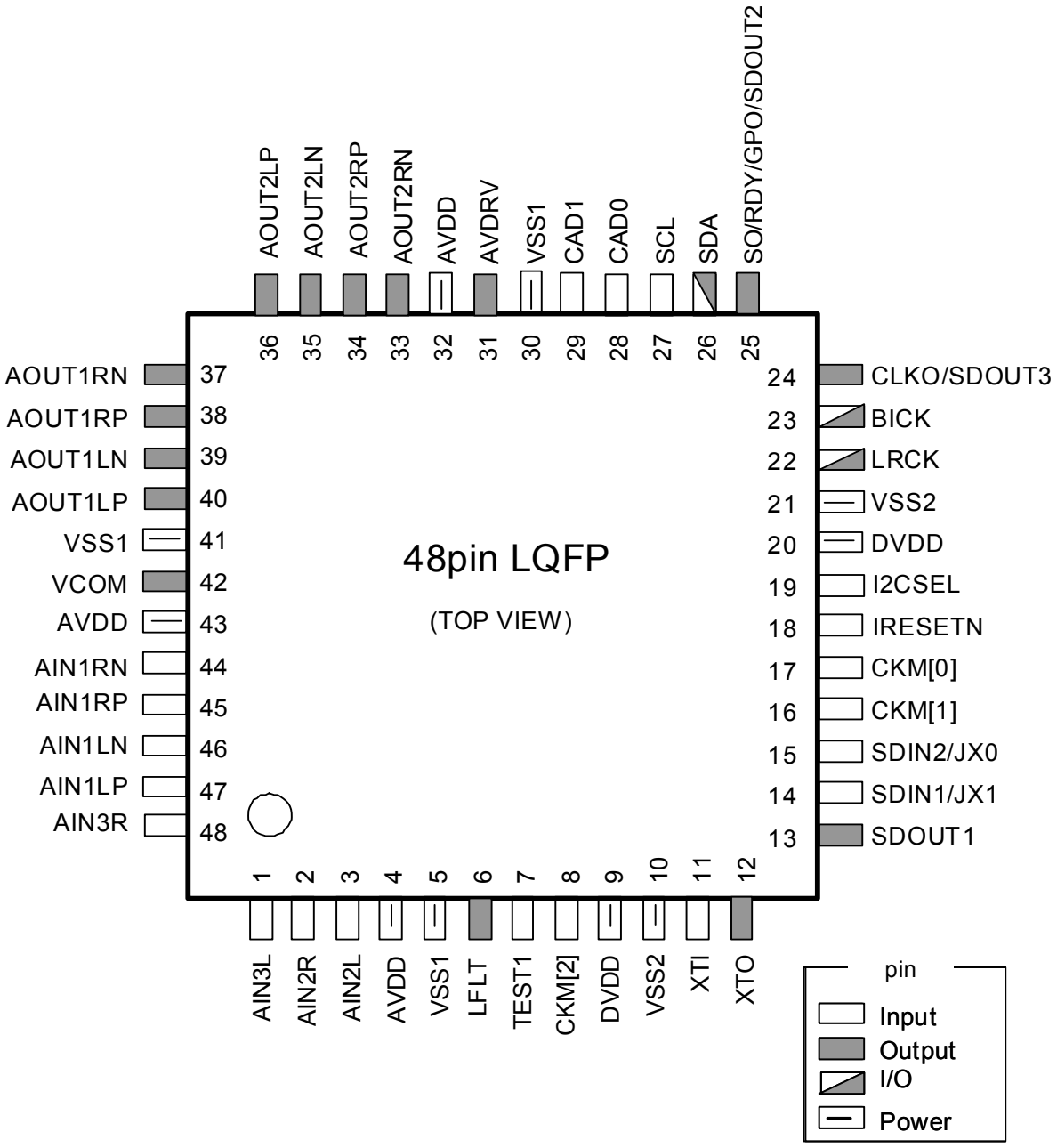
Figure 2. AK7742 DSP Block

■ Ordering Guide

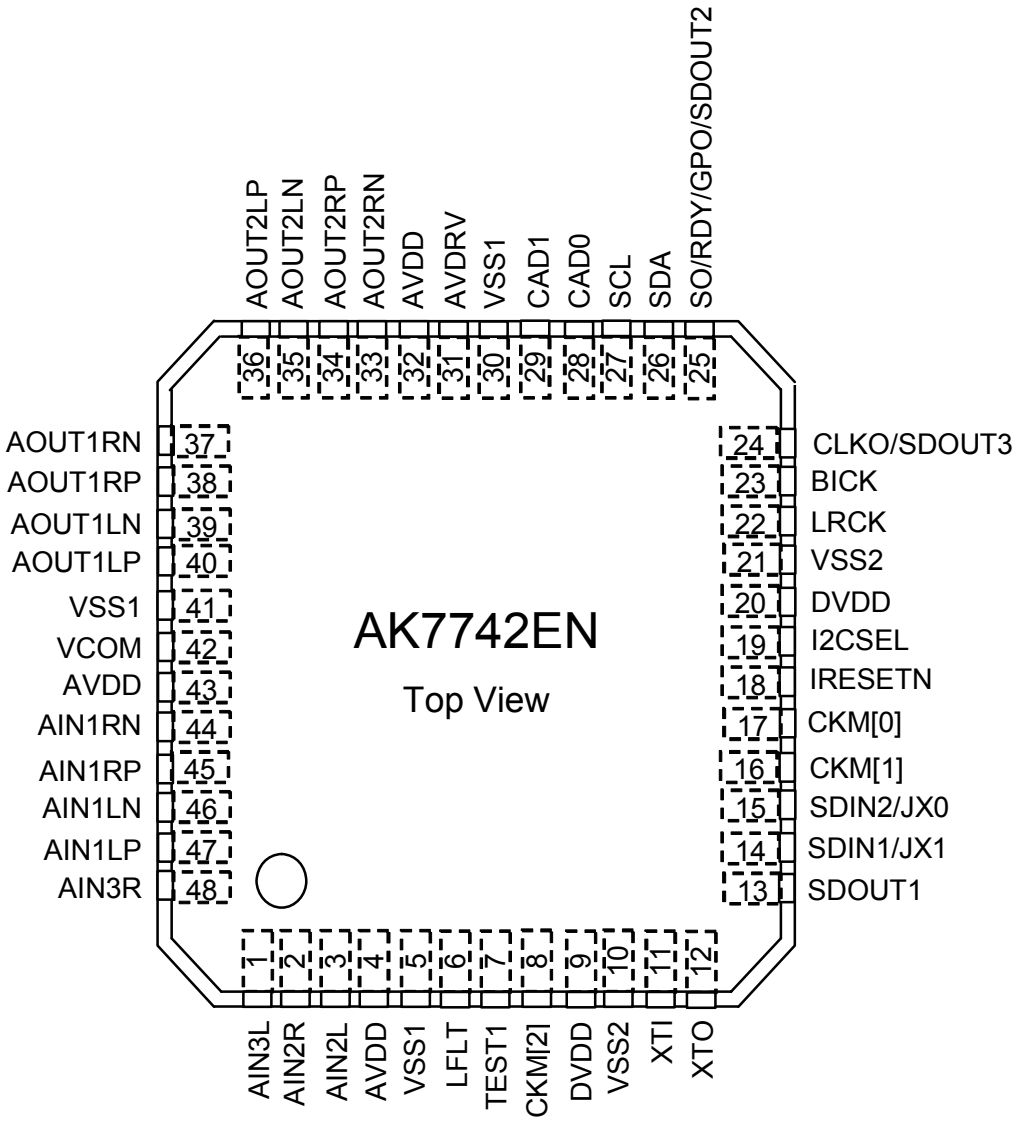
AK7742EQ	-20 ~ +70°C	48pin LQFP (0.5mm pitch)
AK7742EN	-20 ~ +85°C	48pin QFN (0.4mm pitch)
AKD7742	Evaluation board for the AK7742	

■ Pin Layout

AK7742EQ



AK7742EN


AK7742EN
Top View
1 AIN3L
2 AIN2R
3 AIN2L
4 AVDD
5 VSS1
6 LFLT
7 TEST1
8 CKM[2]
9 DVDD
10 VSS2
11 XTI
12 XTO
13 SDOUT1
14 SDIN1/JX1
15 SDIN2/JX0
16 CKM[1]
17 CKM[0]
18 IRESETN
19 I2CSEL
20 DVDD
21 VSS2
22 LRCK
23 BICK
24 CLKO/SDOUT3
25 SO/RDY/GPO/SDOUT2
26 SDA
27 SCL
28 CAD0
29 CAD1
30 VSS1
31 AVDRV
32 AVDD
33 AOUT2RN
34 AOUT2RP
35 AOUT2LN
36 AOUT2LP
37 AOUT1RN
38 AOUT1RP
39 AOUT1LN
40 AOUT1LP
41 VSS1
42 VCOM
43 AVDD
44 AIN1RN
45 AIN1RP
46 AIN1LN
47 AIN1LP
48 AIN3R

PIN FUNCTION

No.	Pin name	I/O	Function	Classification
1	AIN3L	I	ADC Lch Single-end input 3 pin	Analog input
2	AIN2R	I	ADC Rch Single-end input 2 pin	Analog input
3	AIN2L	I	ADC Lch Single-end input 2 pin	Analog input
4	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
5	VSS1		Analog ground 0V	Analog power supply
6	LFLT	O	Filter connection pin for PLL Connect C=12nF to VSS1. "L" output during initial reset.	Analog output
7	TEST1	I	Test pin (internal pull-down resistor) Connect to VSS2	Test
8	CKM[2]	I	Clock mode select pin 2	Mode select
9	DVDD		Power supply pin for digital section 3.0V ~ 3.6V	Digital power supply
10	VSS2		Digital ground 0V	Digital power supply
11	XTI	I	Master clock input pin When using a crystal oscillator, connect it between this pin and XTO. When using external main clock, input to this pin with CMOS level.	Clock
12	XTO	O	Crystal oscillator output pin When using a crystal oscillator, connect it between this pin and XTI. When not using crystal oscillator, leave open. Output during initial reset is not determined.	Clock
13	SDOUT1	O	DSP serial data output pin "L" output during initial reset	Data interface
14	SDIN1/JX1	I	Serial data input pin 1 / JX1	Data interface
15	SDIN2/JX0	I	Serial data input pin 2 / JX0	Data interface
16	CKM[1]	I	Clock mode select pin 1	Mode select
17	CKM[0]	I	Clock mode select pin 0	Mode select
18	IRESETN	I	Reset pin (for initialization)	Reset
19	I2CSEL	I	I^2CBUS select pin Connect to DVDD	Microcomputer I/F
20	DVDD		Power supply pin for digital section 3.0V ~ 3.6V	Digital power supply
21	VSS2		Digital ground 0V	Digital power supply
22	LRCK	I/O	LR channel select clock pin "L" output during initial reset with master mode.	Data interface
23	BICK	I/O	Serial bit clock pin "L" output during initial reset with master mode.	Data interface
24	CLKO/SDOUT3	O	Clock output / DSP serial data output pin "L" output during initial reset	Clock
25	SO/RDY/GPO/ SDOUT2	O	Serial data output pin / Data write ready output pin / General purpose output / DSP serial data output pin "L" output during initial reset	Microcomputer I/F
26	SDA	I/O	SDA I^2C bus interface	Microcomputer I/F
27	SCL	I	SCL I^2C bus interface	Microcomputer I/F
28	CAD0	I	I^2C bus address pin 0	Microcomputer I/F
29	CAD1	I	I^2C bus address pin 1	Microcomputer I/F
30	VSS1		Analog ground 0V	Analog power supply

31	AVDRV	O	AVDRV Pin Connect 1μF to VSS1. Never to use for external circuit. “L” output during initial reset	Analog power supply
32	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
33	AOUT2RN	O	DAC2 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
34	AOUT2RP	O	DAC2 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
35	AOUT2LN	O	DAC2 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
36	AOUT2LP	O	DAC2 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
37	AOUT1RN	O	DAC1 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
38	AOUT1RP	O	DAC1 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
39	AOUT1LN	O	DAC1 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
40	AOUT1LP	O	DAC1 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
41	VSS1		Analog ground 0V	Analog power supply
42	VCOM	O	Analog common voltage Connect 0.1μF and 2.2μF in parallel to VSS1. Never to use for external circuit. “L” output during initial reset	Analog output
43	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
44	AIN1RN	I	ADC Rch differential inverted analog input pin	Analog input
45	AIN1RP	I	ADC Rch differential non-inverted analog input pin	Analog input
46	AIN1LN	I	ADC Lch differential inverted analog input pin	Analog input
47	AIN1LP	I	ADC Lch differential non-inverted analog input pin	Analog input
48	AIN3R	I	ADC Rch Single-end input 3 pin	Analog input

Note:

Digital input pins are never to be left open.

If analog input pins (AIN1LP, AIN1LN, AIN1RP, AIN1RN, AIN2L, AIN2R, AIN3L, AIN3R) are not used, leave them open.

ABSOLUTE MAXMUM RATING

(VSS1=VSS2=0V: Note 1)

Item		Symbol	min	max	Unit
Power supply voltage (AVDD= DVDD)					
Analog		AVDD	-0.3	4.3	V
Digital		DVDD	-0.3	4.3	V
Input current (except for power supply pin)		IIN	-	±10	mA
Analog input voltage (Note 2) AIN1LP, AINL1N, AIN1RP, AINR1N, AIN2L, AIN2R, AIN3L, AIN3R		VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital input voltage (Note 3)		VIND	-0.3	(DVDD+0.3) or 4.3	V
Operating ambient temperature	AK7742EQ	Ta	-20	70	ºC
	AK7742EN	Ta	-20	70	ºC
Storage temperature		Tstg	-65	150	ºC

Note 1. All indicated voltages are with respect to ground. VSS1 and VSS2 must be the same voltage.
Note 2. The maximum value of analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 3. The maximum value of digital input voltage is smaller value between (DVDD+ 0.3)V and 4.3V.

WARNING: Operating at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these critical conditions.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V: Note 1)

Item	Symbol	min	typ	max	Unit
Power supply voltage					
Analog	AVDD	3.0	3.3	3.6	V
Digital	DVDD	3.0	3.3	3.6	V

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in the datasheet.

Note) Do not turn off the power of the AK7742 during the power supplies of surrounding devices are turned on. DVDD must not exceed the pull-up of SDA and SCL of I^2C BUS. (The diode exists for DVDD in the SDA and SCL pins.)

ANALOG CHARACTERISTICS

■ ADC Characteristics

(Ta=25ºC; AVDD=DVDD=3.3V; BICK=64fs; signal frequency 1kHz; Measurement bandwidth=20Hz~20kHz, fs=48kHz, ADC differential input, CKM mode 0 (CKM[2:0]=000), unless otherwise specified)

	Parameter	min	typ	max	Unit
Stereo ADC	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (-1dBFS) (Note 4)	76	84		dB
	Dynamic range (A-weighted) (Note 4)	88	96		dB
	S/N (A-weighted) (Note 4)	88	96		dB
	Inter-channel isolation (f=1kHz) (Note 5)	90	105		dB
	DC accuracy				
	Channel gain mismatch		0.1	0.3	dB
	Analog input				
	Input voltage (differential input) (Note 6)	±1.85	±2.00	±2.15	Vp-p
	Input voltage (single-end input) (Note 7)	1.85	2.00	2.15	Vp-p
	Input impedance (Note 8)	41	62		kΩ

Note 4. This value is not guaranteed for single-ended inputs.
Note 5. Indicates isolation between L and R when -1dBFS signal is applied.
Note 6. Target input pins are AIN1LP, AIN1LN, AIN1RP, AIN1RN.
Note 7. Target input pins are AIN2L, AIN2R, AIN3L, AIN3R.
Note 8. Target input pins are AIN1LP, AIN1LN, AIN1RP, AIN1RN, AIN2L, AIN2R, AIN3L, AIN3R.

■ DAC Characteristics

(Ta=25ºC; AVDD=DVDD=3.3V; BICK=64fs; signal frequency 1kHz; Measurement bandwidth=20Hz~20kHz, fs=48kHz, R_L=5KΩ, C_L= 15pF; CKM mode 0 (CKM[2:0]=000), unless otherwise specified)

	Parameter	min	typ	max	Unit
Stereo DAC	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (0dBFS)	80	92		dB
	Dynamic range (A-weighted)	90	106		dB
	S/N (A-weighted)	90	106		dB
	Inter-channel isolation (f=1kHz)(Note 9)	90	100		dB
	DC accuracy				
	Channel gain mismatch		0.2	0.5	dB
	Analog output				
	Output voltage (Note 10)	3.36	3.66	3.96	Vp-p
	Load resistance	5			kΩ
	Load capacitance			30	pF

Note 9. Indicates isolation between each DAC's of Lch and Rch when -1dBFS signal is applied.
Note 10. Full scale output voltage. The output voltage scales with AVDD.

DC CHARACTERISTICS

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
High level input voltage (Note 11)	VIH	80%DVDD			V
Low level input voltage (Note 11)	VIL			20%DVDD	V
SCL, SDA High level input voltage	VIH	70%DVDD			V
SCL, SDA Low level input voltage	VIL			30%DVDD	V
High level output voltage Iout=-100μA	VOH	DVDD-0.5			V
Low level output voltage Iout=100μA (Note 12)	VOL			0.5	V
SDA Low level output voltage Iout=3mA	VOL			0.4	V
Input leak current (Note 13)	Iin			±10	μA
Input leak current (pull-down) (Note 14)	Iid		22		μA
Input leak current XTI pin	Iix		26		μA

Note 11. Except for the SCL, SDA pin.
Note 12. Except for the SDA pin.
Note 13. Except for the TEST1 pin, XTI pin.
Note 14. The TEST1 pin has an internal pull-down device, nominally 150kΩ.

POWER CONSUMPTION

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V(typ=3.3V, max=3.6V))

Parameter	min	typ	max	Unit
Power supply current (Note 15)				
Normal Operation AVDD+DVDD		75	122	mA
Reset (IRESETN= "L" reference data) AVDD+DVDD (Note 16)		2		mA

Note 15. Depends on the system frequency and contents of DSP program.
Note 16. This is a reference value when using a crystal oscillator. Since most of the supply current at the initial reset state is in the oscillator section, the value may vary according to the crystal type and the external circuit. This value is just reference.

DIGITAL FILTER CHARACTERISTICS

■ ADC

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN), AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Pass band (±0.005dB) (Note 18)	PB	0		21.5	kHz
(-0.02dB)			21.768		kHz
(-6.0dB)			24.00		kHz
Stop band	SB	26.5			kHz
Pass band ripple (Note 18)	PR			±0.005	dB
Stop band attenuation (Note 19, Note 20)	SA	80			dB
Group delay distortion	ΔGD			0	μs
Group delay (Ts=1/fs)	GD		30		Ts
Digital filter + Analog filter characteristics					
Amplitude characteristic 20Hz~20.0kHz			±0.01		dB

Note 17. Each parameter is related to the sampling frequency (fs). HPF response is not included.
Note 18. Pass band is from DC to 21.5kHz when fs=48kHz.
Note 19. Stop band is from 26.5kHz to 3.0455MHz when fs=48kHz.
Note 20. When fs=48kHz, the analog modulator samples the analog input at 3.072MHz. Therefore the input signal is not attenuated by the digital filter in multiple bands (n x 3.072MHz ±21.99kHz; n=0, 1, 2, 3 …) of the sampling frequency.

■ DAC

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN), AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Digital filter					
Pass band ±0.07dB (Note 21)	PB	0		21.7	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 21)	SB	26.2			kHz
Pass band ripple	PR			±0.01	dB
Stop band attenuation	SA	64			dB
Group delay (Ts=1/fs) (Note 22)	GD	-	24		Ts
Digital filter + Analog filter					
Amplitude characteristic 0~20.0kHz			±0.5		dB

Note 21. Pass band and Stop band parameter is related to sampling frequency(fs). PB=0.4535fs (at-0.05dB), SB=0.5465fs.
Note 22. The digital filter's delay is calculated as the time from setting 24-bit data into the input register until an analog signal is output.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter		Symbol	min	typ	max	Unit
XTI						
a)with a crystal oscillator						
Frequency(256fs) CKM[2:0]= 000	fs=44.1KHz fs=48KHz	fXTI	-	11.2896 12.288	-	MHz
b)with an external clock						
Duty cycle		Duty	40	50	60	%
Frequency(256fs) CKM[2:0]= 000, 010	fs=44.1KHz fs=48KHz	fXTI	11.0	11.2896 12.288	12.4	MHz
Frequency (384fs) CKM[2:0]= 001	fs=44.1KHz fs=48KHz	fXTI	16.5	16.9344 18.432	18.6	MHz
LRCK frequency (Note 23)		Fs	7.35	48	96	kHz
BICK frequency						
a) CKM[2:0]= 001, 010			32	64		fs
High level width		tBCLKH	64			ns
Low level width		tBCLKL	64			ns
Frequency		fBCLK	0.46	3.072	6.144	MHz
b) CKM[2:0]= 011 (Note 25)				64		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	2.75	3.072	3.1	MHz
c) CKM[2:0]= 100 (Note 26)				32		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	230	256	258	kHz
d) CKM[2:0]= 101 (Note 27)				64		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	460	512	516	kHz

Note 23. LRCK frequency and sampling rate (fs) should be the same.
Note 24. The BICK must be divided 32, 48 or 64 clocks correctly. (BICK can be selected from 32fs, 48fs or 64fs)
Note 25. When BICK is resource of internal MCLK. The BICK must be divided 64 clocks correctly. 64fs fixed.
Note 26. When BICK is resource of internal MCLK. The BICK must be divided 32 clocks correctly. 32fs fixed.
Note 27. When BICK is resource of internal MCLK. The BICK must be divided 64 clocks correctly. 64fs fixed.

■ Reset

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
IRESET (Note 28)	tRST	600			ns

Note 28. It is necessity that the power is supplied and master clock is input when the IRESET pin goes to "H".

■ Audio Interface

1) SDIN1, SDIN2, SDOUT1, SDOUT2, SDOUT3

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BICK frequency	fBCLK	32	64		fs
BICK low level width	tBCLKL	150			ns
BICK high level width	tBCLKH	150			ns
Delay time from BICK "↑" to LRCK (Note 29)	tBLRD	40			ns
Delay time from LRCK to BICK "↑" (Note 29)	tLRBD	40			ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Delay time from LRCK to serial data output	tLRD	-10		40	ns
Delay time from BICK "↓" to serial data output (Note 30)	tBSOD	-10		40	ns
Master mode					
BICK frequency	fBCLK		64		fs
BICK duty cycle			50		%
Delay time from BICK "↑" to LRCK	tBLRD	40			ns
Delay time from LRCK to BICK "↑"	tLRBD	40			ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Delay time from BICK "↓" to serial data output (Note 30)	tBSOD	-30		40	ns

Note 29. BICK rising edge must not occur at the same time as LRCK edge.

Note 30. The serial data output is synchronized to BICK falling edge, and held until next BICK falling (spec -10ns) in Slave mode. In case of the LRCK edge comes before BICK edge, data will be held until LRCK edge (spec -10ns). In Master mode, serial data is held until 30ns before falling edge of BICK. Therefore, please use BICK rising edge in both slave and master modes for a safety latch.

■ I²CBUS Interface

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
I²C Timing					
SCL clock frequency	fSCL			400	KHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 31. I²C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

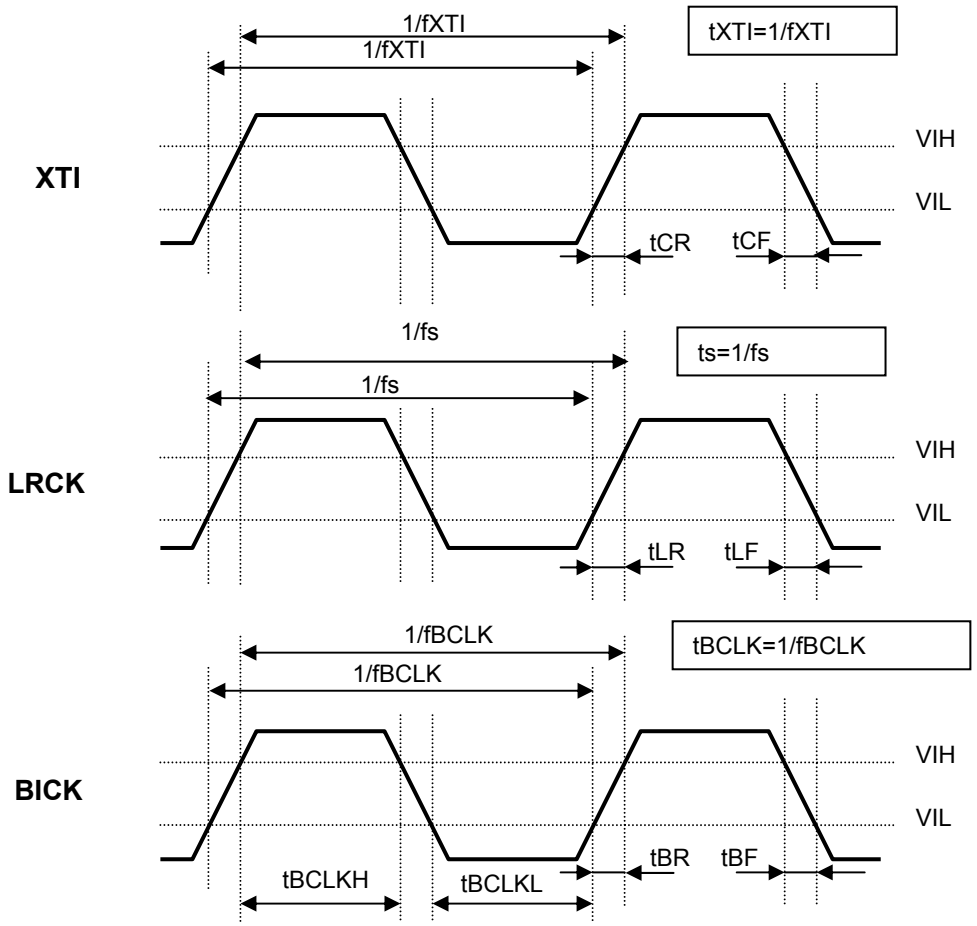


Figure 3. System Clock

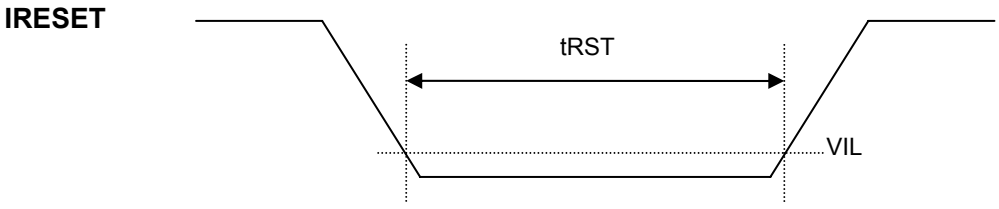


Figure 4. Reset

Audio Interface

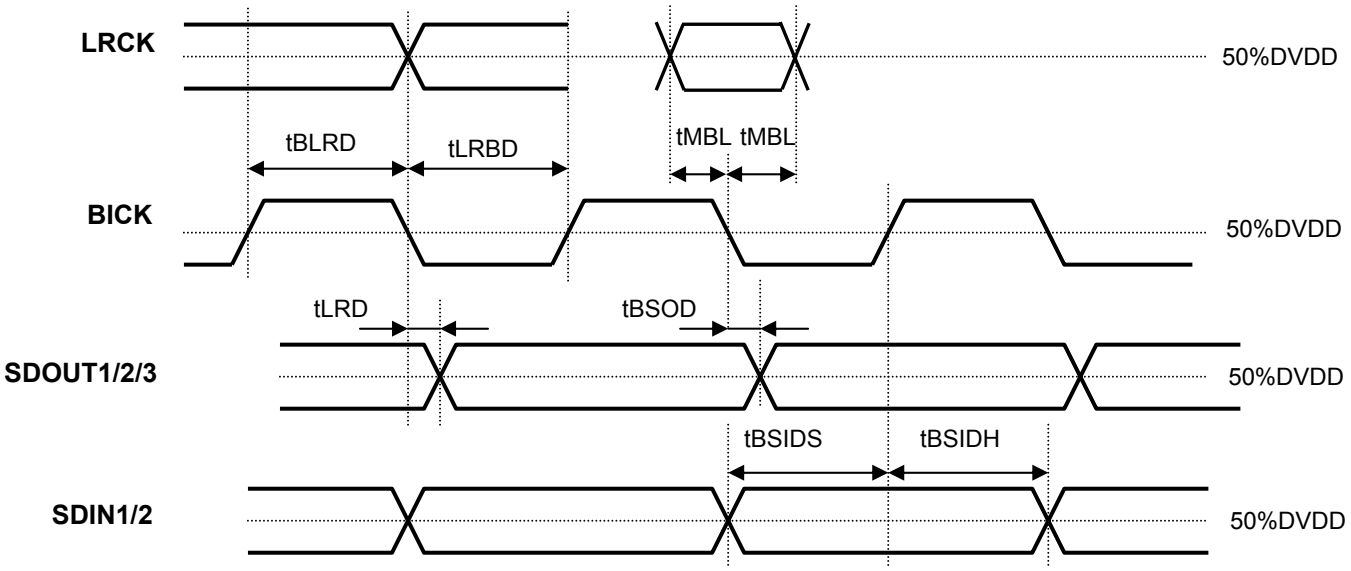


Figure 5. Audio Interface

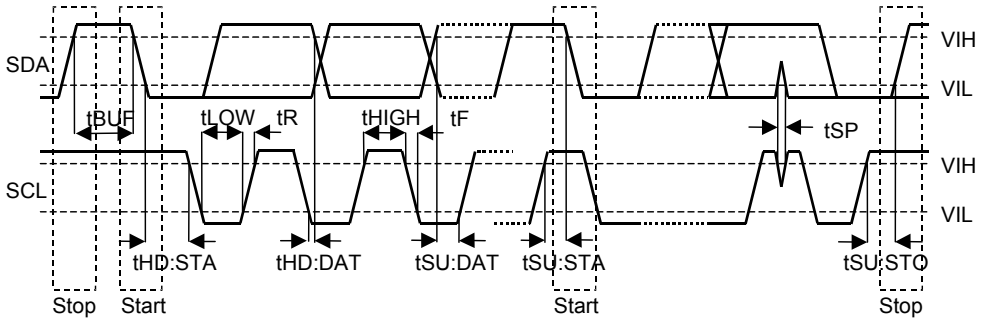


Figure 6. I^2C Bus Interface

OPERATION OVERVIEW

■ CKM[2:0] Clock Mode Select Pin

Master/Slave mode switching, MCLK/ICLK (internal master clock/generating clock) clock source pin select, and ICLK frequency change are controlled by CKM [2:0] clock mode select pins. CKM[2:0] pins can only be set during initial reset.

CKM Mode	CKM [2:0]	Master Slave	MCLK source	Input frequency for MCLK	Input pin(s) required for system clock	use the oscillator permitted
0	000	Master	XTI	12.288MHz (Note 32)	XTI (256fs)	YES
1	001	Slave	XTI	18.432MHz (Note 32)	XTI (384fs), BICK (32fs, 48fs, 64fs) LRCK (fs)	-
2	010	Slave	XTI	12.288MHz (Note 32, Note 35)	XTI(256fs), BICK (32fs, 48fs, 64fs), LRCK (fs)	-
3	011	Slave	BICK	64fs (fs=48kHz fixed)	BICK, LRCK	-
4	100	Slave	BICK	32fs (fs=8kHz fixed)	BICK, LRCK	-
5	101	Slave	BICK	64fs (fs=8kHz fixed)	BICK, LRCK	-
6	110	TEST	N/A	N/A	N/A	-
7	111	TEST	N/A	N/A	N/A	-

(N/A: Not available)

Note 32. On operating fs=44.1kHz series, multiply 44.1/48.
Note 33. CKM mode 6/7 are for testing purpose only. Cannot be used.
Note 34. The sampling frequency is set by control register CONT0 in CKM mode 0.
Note 35. In case of CKM mode 1/2, XTI and LRCK must be synchronized. The phase is not critical.
Note 36. The sampling frequency on CKM mode 3-5 is fixed. The setting of control register CONT0 is ignored.
Note 37. In case of CKM mode 3-5, BICK must be divided exactly from LRCK. BICK and LRCK must be synchronized.

[Description rule]
Regarding the input / output levels in this Datasheet, the low level is represented as "L" and the high level is represented as "H". The registers or bus pins (such as CKM[2:0] is represented "0" and "1".
##h means hexadecimal code. (# = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F)

■ Relationship of Clock Source (ICLK) and MCLK

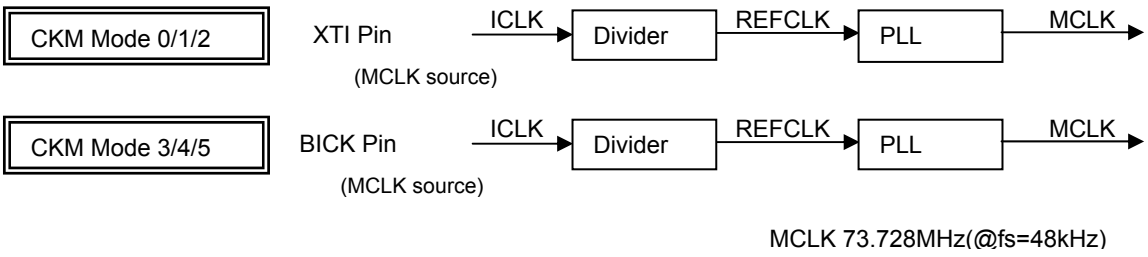


Figure 7. The Relationship of Clock Source (ICLK) and MCLK

1. Master Mode (CKM Mode 0)

fs: Sampling frequency

CKM Mode	CKM [2:0]	XTI		Input frequency range (MHz)	Use of crystal permitted
		fs:48kHz series	fs:44.1kHz series		
0	000	12.288MHz	11.2896MHz	11.0~12.4	YES

Input system clock to the XTI pin. The internal counter which is synchronized to XTI generates LRCK (1fs) and BICK (64fs). LRCK and BICK is not output during initial reset state (IRESETN pin= "L") and system reset state. (Refer to ■ Reset)

The system clock for the AK7742 can be supplied to the XTI pin by the following way. In case of CKM mode 0, connect proper crystal oscillator XTI and XTO pin, or supply appropriate system clock to the XTI pin.

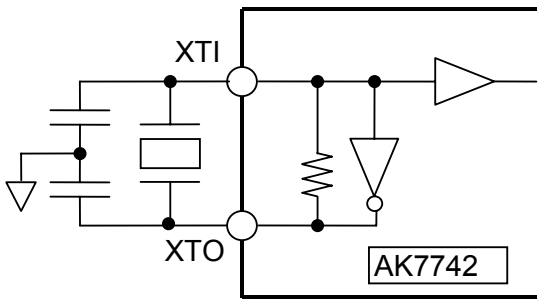


Figure 8. Using Crystal Oscillator (CKM Mode 0)

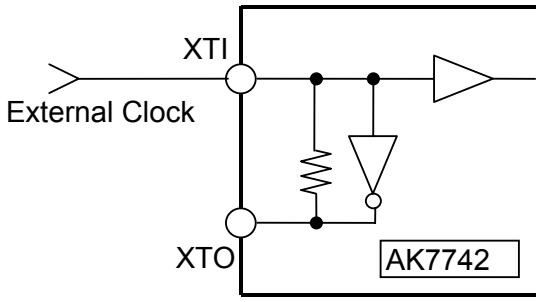


Figure 9. Using External System Clock(CKM Mode 0)

The sampling frequency is determined by control register CONT0 DFS[2:0] (D3, D2, D1).

2. Slave Mode (XTI Input Clock) (CKM Mode 1/2)

fs: sampling frequency

CKM Mode	CKM [2:0]	XTI		Input frequency range (MHz)	Use of crystal permitted
		fs:48kHz series	fs:44.1kHz series		
1	001	18.432MHz	16.9344MHz	16.5~18.6	Not Permitted
2	010	12.288MHz	11.2896MHz	11.0~12.4	Not Permitted

The required system clocks are XTI, LRCK and BICK. XTI and LRCK must be synchronized but the phase is not critical.

3. Slave Mode (BICK input) (CKM Mode 3/4/5)

In the CKM mode 3/4/5, BICK is used for clock source. This clock is multiplied by a PLL directly, therefore burst clock or the clock with two different frequencies can not be used.

fs: sampling frequency

CKM Mode	CKM [2:0]	BICK			Input frequency range
		BICK	fs:48kHz series	fs:44.1kHz series	
3	011	64fs(fs=48,44.1kHz)	3.072MHz	2.8224MHz	2.75~3.1MHz
4	100	32fs(fs=8kHz)	256kHz		230~258kHz
5	101	64fs(fs=8kHz)	512kHz	-	460~516kHz

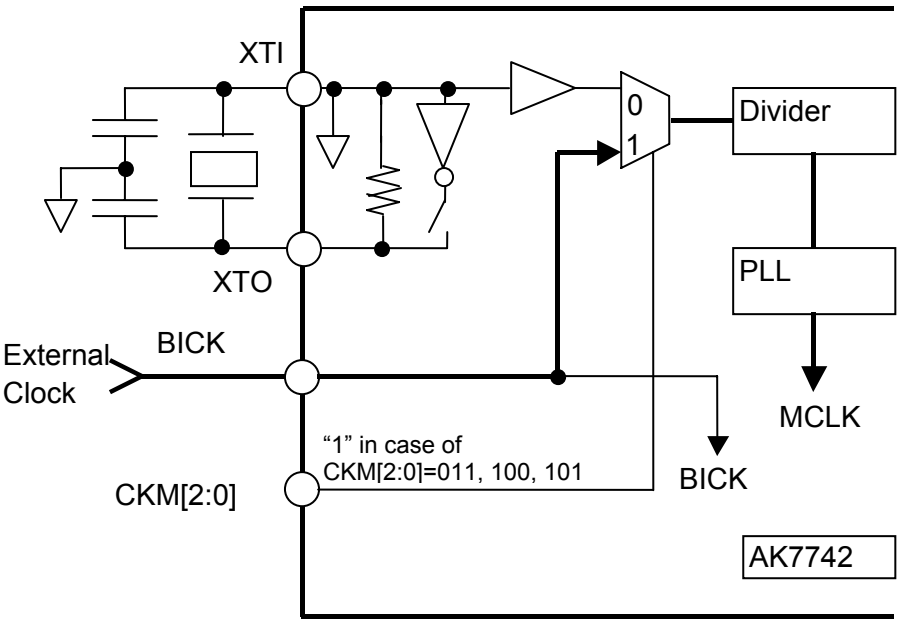


Figure 10. Internal Connection Image

Sampling rate is fixed by CKM[2:0] pin setting. The control register CONT0 DFS mode setting is ignored. In applications which do not need the XTI pin of the AK7742, set the XTI pin= "L"(VSS2).

4. CKM[2:0] Pin Setting Changing

CKM[2:0] pin setting must be made during initial reset after the AK7742 is powered-up or clock reset.

5. CKM[2:0] Pin Setting / IO Interface

Slave/ Master	CKM Mode	CKM [2:0]	DFS Mode	DFS [2:0]	fs(kHz)	BICK	
						MSB/LSB justified	I^2S compatible
M	0	000	0	000(default)	48/44.1	64fs	64fs
M	0	000	1	001	32/29.4	64fs	64fs
M	0	000	2	010	16/14.7	64fs	64fs
M	0	000	3	011	8	64fs	64fs
M	0	000	4	100	96/88.2	64fs	64fs
S	1	001	0	000(default)	48/44.1	64fs,48fs,32fs	64fs,48fs
S	1	001	1	001	32/29.4	64fs,48fs,32fs	64fs,48fs
S	1	001	2	010	16/14.7	64fs,48fs,32fs	64fs,48fs
S	1	001	3	011	8	64fs,48fs,32fs	64fs,48fs
S	1	001	4	100	96/88.2	64fs,48fs,32fs	64fs,48fs
S	2	010	0	000(default)	48/44.1	64fs,48fs,32fs	64fs,48fs
S	2	010	1	001	32/29.4	64fs,48fs,32fs	64fs,48fs
S	2	010	2	010	16/14.7	64fs,48fs,32fs	64fs,48fs
S	2	010	3	011	8	64fs,48fs,32fs	64fs,48fs
S	2	010	4	100	96/88.2	64fs,48fs,32fs	64fs,48fs
S	3	011	-	-	48/44.1	64fs	64fs
S	4	100	-	-	8	32fs	32fs
S	5	101	-	-	8	64fs	64fs

Note 38. DFS mode is assigned to control register CONT0 DFS[2:0] (D3, D2, D1).

■ Control Register Setting

The AK7742 control register settings are executed through a microcontroller interface. The AK7742 has 15 control registers, and each register has 8bit length. The LSB bit is always "0". Register configuration is shown below. The value of each control register becomes valid when LSB "0" is written.
All registers are initialized by IRESETN pin = "L". The system reset does not initialize the registers.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C0h	40h	CONT0	DIFPCM	DIFI2S	PCM[1]	PCM[0]	DFS[2]	DFS[1]	DFS[0]	0	00h
C1h	41h	CONT1	ATSPAD	ATSPDA	BANK[1]	BANK[0]	TEST	SS[1]	SS[0]	0	00h
C2h	42h	CONT2	POMODE	DATARAM	BIT32FS	WAVM	WAVP[1]	WAVP[0]	EEFN	0	00h
C3h	43h	CONT3	DIF[1]	DIF[0]	DOF[1]	DOF[0]	CLKS[2]	CLKS[1]	CLKS[0]	0	00h
C4h	44h	CONT4	CLKOE	BITCLKEN	LRCLKEN	OUT2EN	OUT1EN	JX1E	JX0E	0	00h
C5h	45h	CONT5	SELDO5 [0]	SELDO4 [0]	SELDO3	SELDO2[1]	SELDO2[0]	SELDO1	SELDO4 [1]	0	00h
C6h	46h	CONT6	ADMUTE	Reserved	ASEL[1]	ASEL[0]	SELDO5[1]	DA2MUTE	DA1MUTE	0	00h
C7h	47h	CONT7	DEM1[1]	DEM1[0]	DEM2[1]	DEM2[0]	TEST	TEST	TEST	0	00h
C8h	48h	CONT8	SRESETN	ADRST	DA2RST	DA1RST	DSPRST	TEST	CKRST	0	00h
D0h	50h	CONT10	VOLADL[7]	VOLADL[6]	VOLADL[5]	VOLADL[4]	VOLADL[3]	VOLADL[2]	VOLADL[1]	VOLADL[0]	30h
D1h	51h	CONT11	VOLADR[7]	VOLADR[6]	VOLADR[5]	VOLADR[4]	VOLADR[3]	VOLADR[2]	VOLADR[1]	VOLADR[0]	30h
D2h	52h	CONT12	VOLDA1L[7]	VOLDA1L[6]	VOLDA1L[5]	VOLDA1L[4]	VOLDA1L[3]	VOLDA1L[2]	VOLDA1L[1]	VOLDA1L[0]	18h
D3h	53h	CONT13	VOLDA1R[7]	VOLDA1R[6]	VOLDA1R[5]	VOLDA1R[4]	VOLDA1R[3]	VOLDA1R[2]	VOLDA1R[1]	VOLDA1R[0]	18h
D4h	54h	CONT14	VOLDA2L[7]	VOLDA2L[6]	VOLDA2L[5]	VOLDA2L[4]	VOLDA2L[3]	VOLDA2L[2]	VOLDA2L[1]	VOLDA2L[0]	18h
D5h	55h	CONT15	VOLDA2R[7]	VOLDA2R[6]	VOLDA2R[5]	VOLDA2R[4]	VOLDA2R[3]	VOLDA2R[2]	VOLDA2R[1]	VOLDA2R[0]	18h

Note 39. Do not access to not specified command codes or registers.
Note 40. "TEST" bit is for test purpose, "0" should be written.
Note 41. The default is initial value of when the IRESETN pin= "L".

1) CONT0: Sampling rate, I/O interface

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C0h	40h	CONT0	DIFPCM	DIFI2S	PCM[1]	PCM[0]	DFS[2]	DFS[1]	DFS[0]	0	00h

DIFPCM: Audio interface select

0: MSB justified, LSB justified, I²S (default)
1: PCM format

Note 42. When using PCM format, D6: DIFI2S must be set "0".

DIFI2S: Audio interface I²S select

0: Except I²S mode (default)
1: I²S mode

When using I2S mode for SDIN1-2, SDOUT1-3, set to DIFI2S bit = "1". All interface setting of DIF[1:0], DOF[1:0] should be set MSB justified (24bit). DIFI2S bit should be set to "0" when using DSP through mode, and all interface setting of DIF[1:0], DOF[1:0] should be set MSB justified (24bit).

Note 43. When using I²S format, D7: DIFPCM must be set "0".

PCM[1:0]: PCM format select (only slave mode available)

Select PCM interface at DIFPCM bit = "1".
PCM format is available for CKM mode 3/4/5.

PCM Mode	PCM[1:0]	LRCK (FRAME)	LRCK edge referenced to BICK edge	BIT32FS bit 0	BIT32FS bit 1	
0	00	short (SF)	rising (RE)	Figure 21	Figure 22	(default)
1	01	short (SF)	falling (FE)	Figure 23	Figure 24	
2	10	long (LF)	rising (RE)	Figure 25	Figure 26	
3	11	long (LF)	falling (FE)	Figure 27	Figure 28	

Please refer to "Audio Data Interface" section.

DFS[2:0]: Sampling frequency setting (CKM Mode 0/1/2)

fs: sampling frequency

CKM Mode	CKM [2:0]	DFS Mode	DFS [2:0]	fs(kHz) 48kHz series	fs(kHz) 44.1kHz series	
0-2	0XX	0	000	48	44.1	(default)
0-2	0XX	1	001	32	29.4	
0-2	0XX	2	010	16	14.7	
0-2	0XX	3	011	8	-	
0-2	0XX	4	100	96	88.2	
3	011	-	-	48	44.1	
4	100	-	-	8	-	
5	101	-	-	8	-	
6	110	-	-	N/A	N/A	
7	111	-	-	N/A	N/A	

(N/A: Not available)

Note 44. DFS mode is available for CKM mode 0/1/2.
No permission to set DFS mode 5-7.

Write "0" into the "0" register.

2) CONT1: RAM control

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C1h	41h	CONT1	ATSPAD	ATSPDA	BANK[1]	BANK[0]	TEST	SS[1]	SS[0]	0	00h

ATSPAD: ADC soft mute transition

0: 912LRCK(max) (19ms at fs=48kHz) (default)
1: 912LRCK x 4(max) (76ms at fs=48kHz)

ATSPDA: DAC1/2 Volume Transition Time Setting

0: 1/fs (default)
1: 4/fs

BANK[1:0]: DLRAM Mode setting

DLRAM Mode	BANK[1:0]	Ring 24bit limited range floating point	Ring 8.4f	Linear 24bit limited range floating point	
0	00	3072word			(default)
1	01	2048word	2048word		
2	10	1024word	2048word	1024word	
3	11	N/A	N/A	N/A	

(N/A: Not available)

SS[1:0]: DLRAM sampling setting

SS Mode	SS[1]	SS[0]	Sampling set time	
0	0	0	address is updated every sampling	(default)
1	0	1	address is updated every 2 samplings	
2	1	0	address is updated every 4 samplings	
3	1	1	address is updated every 8 samplings	

Note 45. When SS mode 1/2/3 is selected, aliasing noise may be generated.
Note 46. DLRAM mode 1/2 affects to the Ring 8.4f buffer only. DLRAM mode 0 affects to the Ring 20.4f buffer.

Write "0" into the TEST bits and "0" registers.

3) CONT2: RAM control

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C2h	42h	CONT2	POMODE	DATARAM	BIT32FS	WAVM	WAVP[1]	WAVP[0]	EEFN	0	00h

POMODE: DLRAM pointer0 select

0: OFREG (default)
1: DBUS direct

DATARAM: DATARAM addressing select

DATARAM Mode	A(000h-3FFh) 1024word	B(400h-5FFh) 512word	
0	Ring addressing	Ring addressing	(default)
1	Ring addressing	Linear addressing	
Pointer	DP0	DP1	

BIT32FS: BICK32fs setting (only slave mode available)

0: BICK64fs (default)
1: BICK32fs
Normally BICK is 64fs. At CKM mode 4, set BIT32FS bit = "1".

WAVM: CRAM WAV Mode select

0: 1/4 mode (default)
1: 1/2 mode
1/4 mode has an advantage of CRAM memory size but calculation precision drops down.

WAVP[1:0]: CRAM memory assignment

WAVP Mode	WAVP[1]	WAVP[0]	WAVM=0	WAVM=1	number of point	
0	0	0	33word	65word	128	(default)
1	0	1	65word	129word	256	
2	1	0	129word	257word	512	
3	1	1	257word	513word	1024	

EFEN: Extended Instruction enable

0: disable (default)
1: enable

Write "0" into the "0" registers.

4) CONT3: I/O interface / Clock select

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C3h	43h	CONT3	DIF[1]	DIF[0]	DOF[1]	DOF[0]	CLKS[2]	CLKS[1]	CLKS[0]	0	00h

DIF[1:0]: DSP DIN1, DIN2 input format select

DIF Mode	DIF[1]	DIF[0]	input format	
0	0	0	MSB justified (24bit)	(default)
1	0	1	LSB justified 24bit	
2	1	0	LSB justified 20bit	
3	1	1	LSB justified 16bit	

Note 47. In case of I^2S format (DIFI2S bit = "1"), set DIF mode 0.

DOF[1:0]: DSP DOUT1, DOUT2, DOUT3 output format select

DOF Mode	DOF[1]	DOF[0]	output format	
0	0	0	MSB justified (24bit)	(default)
1	0	1	LSB justified 24bit	
2	1	0	LSB justified 20bit	
3	1	1	LSB justified 16bit	

Note 48. In case of I^2S format (DIFI2S bit = "1") or BIT32FS bit = "1", set DOF mode 0.

CLKS[2:0]:CLKO clock select

CLKS Mode	CLKS[2:0]	fs=48kHz series	fs=44.1kHz series	
0	000	12.288MHz	11.2896MHz	(default)
1	001	6.144MHz	5.6448MHz	
2	010	3.072MHz	2.8224MHz	
3	011	8.192MHz	7.5264MHz	
4	100	4.096MHz	3.7632MHz	
5	101	2.048MHz	1.8816MHz	
6	110	18.432MHz	16.9344MHz	
7	111	N/A	N/A	

(N/A: Not available)

Write "0" into the "0" registers.

5) CONT4: Clock / Output setting

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C4h	44h	CONT4	CLKOE	BITCLKEN	LRCLKEN	OUT2EN	OUT1EN	JX1E	JX0E	0	00h

CLKOE: CLKO output enable

0: CLKO output disable (default)
1: CLKO output enable

BITCLKEN:

When the AK7742 is in master mode, BICK output can be stopped.
0: Enable (default)
1: Disable (Low output)
When CKM mode 1-5, AK7742 is in slave mode. Appropriate BICK clock is required.

LRCLKEN:

When the AK7742 is in master mode, LRCK output can be stopped.
0: Enable (default)
1: Disable (Low output)
When CKM mode 1-5, AK7742 is in slave mode. Appropriate LRCK clock is required.

OUT2EN: SO/RDY/GPO/SDOUT2 disable

0: SO/RDY/GPO/SDOUT2 output enable (default)
1: SO/RDY/GPO/SDOUT2 output disable

OUT1EN: SDOUT1 output enable

0: SDOUT1 output disable (default)
1: SDOUT1 output enable

JX1E:

0: Select SDIN1/JX1 pin for DSP input port SDIN1 (default)
1: Select SDIN1/JX1 pin for DSP input port JX1

JX0E:

0: Select SDIN2/JX0 pin for DSP input port DIN2 (default)
1: Select SDIN2/JX0 pin for DSP input port JX0

Write "0" into the "0" registers.

6) CONT5: DSP output select

Write during system reset state.

		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
C5h	45h	CONT5	SELDO5 [0]	SELDO4 [0]	SELDO3	SELDO2[1]	SELDO2[0]	SELDO1	SELDO4 [1]	0	00h

D7: SELDO5[0] DAC2 SDINDA2 input select

SELDO5 Mode	SELDO5[1] CONT6 D3	SELDO5[0] CONT5 D7	Input Data Select	
0	0	0	DSP Port: DOUT5	(default)
1	0	1	SDIN2 Pin	
2	1	0	SDIN1 Pin	
3	1	1	ADC Port: SDOUTAD	

D6: SELDO4[0] DAC1 SDINDA1 input select

SELDO4 Mode	SELDO4[1] CONT5 D1	SELDO4[0] CONT5 D6	Input Data Select	
0	0	0	DSP Port: DOUT4	(default)
1	0	1	SDIN1 Pin	
2	1	0	SDIN2 Pin	
3	1	1	ADC Port: SDOUTAD	

D5: SELDO3 CLKO/SDOUT3 output select

0: CLKO (default)
1: DSP port DOUT3

D4, D3: SELDO2[1:0] SO/RDY/GPO/SDOUT2 output select

SELDO2 Mode	SELDO2[1:0]	Output Function	
0	00	SO	(default)
1	01	RDY	
2	10	DSP GPO	
3	11	DSP DOUT2	

D2: SELDO1 SDOUT1 output select

0: DSP port DOUT1 (default)
1: ADC SDOUTAD

D1: SELDO4[1]

Refer to D6

Write "0" into the TEST bits and "0" registers.

7) CONT6: ADC setting

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C6h	46h	CONT6	ADMUTE	Reserved	ASEL[1]	ASEL[0]	SELDO5[1]	DA2MUTE	DA1MUTE	0	00h

D7: ADMUTE ADC SMUTE setting

0: ADC SMUTE release (default)
1: ADC SMUTE

D6: Reserved

0: normal operation (default)
Set to "0"

D5, D4: ASEL[1:0] ADC input select

ASEL Mode	ASEL1[1:0]	selected pin(s)	
0	00	AIN1LP, AIN1LN, AIN1RP, AIN1RN	(default)
1	01	AIN2L, AIN2R	
2	10	AIN3L, AIN3R	
3	11	N/A	

(N/A: Not available)

In case that this register is changed while an operation, take a measure of mute process to reduce switching noise.

D3: SELDO5[1] DAC2 SDINDA2 Input Setting

Refer to D7

D2: DA2MUTE DAC2 SMUTE Setting

0: DAC2 SMUTE disable (default)
1: DAC2 SMUTE enable

D1: DA1MUTE DAC1 SMUTE Setting

0: DAC1 SMUTE disable (default)
1: DAC1SMUTE enable

Write "0" into the TEST bit(s) and "0" register(s).

8) CONT7: TEST

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C7h	47h	CONT7	DEM1[1]	DEM1[0]	DEM2[1]	DEM2[0]	TEST	TEST	TEST	0	00h

D7, D6: DEM1[1:0] DAC1 De-emphasis Setting (50/15μs)

DEM Mode	DEM1[1:0]	Sampling Frequency (fs)	
0	00	Off	(default)
1	01	48KH	
2	10	44.1KHz	
3	11	32KHz	

D5, D4: EM2[10] DAC2 De-emphasis Setting (50/15μs)

DEM Mode	DEM1[1:0]	Sampling Frequency (fs)	
0	00	Off	(default)
1	01	48KH	
2	10	44.1KHz	
3	11	32KHz	

Write "0" into the TEST bit(s) and "0" register(s).

9) CONT8: Reset

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C8h	48h	CONT8	SRESETN	ADRST	DA2RST	DA1RST	DSPRST	TEST	CKRST	0	00h

D7: SRESETN

0: system reset state (default)
1: DSP / ADC / DAC operating

When SRESETN bit = "0", ADC, DSP, DAC1 and DAC2 are in reset state regard less of ADCRST, DA2RST, DA1RST and DSPRST bits settings. Control register and program writings should be made during this System reset period. ADCRST, DA2RST, DA1RST and DSPRST bits are effective for powere saving of each block.

ADRST:

0: ADC operating (default)
1: ADC powered down

DA2RST:

0: DAC2 operating (default)
1: DAC2 powered down

DA1RST:

0: DAC1 operating (default)
1: DAC1 powered down

DSPRST: DSP Reset

0: Normal use DSP Reset Exsit (default)
1: DSP Reset
For when using ADC and DAC without operating DSP. ADC and DAC data foramat is fixed to MSB justified.

CKRST:

0: Clock reset release (default)
1: Clock reset state

If the CKM mode or input frequency is changed without initial reset, this CKRST register has to be set "1". All other registers are not initialized by this reset register.

Write "0" into the TEST bit(s) and "0" register(s).

10) CONT10-11: ADC Volume Control

		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
D0h	50h	CONT 10	VOLADL [7]	VOLADL [6]	VOLADL [5]	VOLADL [4]	VOLADL [3]	VOLADL [2]	VOLADL [1]	VOLADL [0]	30h
D1h	51h	CONT 11	VOLADR [7]	VOLADR [6]	VOLADR [5]	VOLADR [4]	VOLADR [3]	VOLADR [2]	VOLADR [1]	VOLADR [0]	30h

VOLADL[7:0], VOLADR[7:0]: Input Digital Volume, L/R indipendent Setting available 0.5dB step 256 Level
(Page 58,Table 4)

11) CONT12-15: DAC1, DAC2 Volume Control

		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
D2h	52h	CONT12	VOLDA 1L[7]	VOLDA 1L[6]	VOLDA 1L[5]	VOLDA 1L[4]	VOLDA 1L[3]	VOLDA 1L[2]	VOLDA 1L[1]	VOLDA 1L[0]	18h
D3h	53h	CONT13	VOLDA 1R[7]	VOLDA 1R[6]	VOLDA 1R[5]	VOLDA 1R[4]	VOLDA 1R[3]	VOLDA 1R[2]	VOLDA 1R[1]	VOLDA 1R[0]	18h
D4h	54h	CONT14	VOLDA 2L[7]	VOLDA 2L[6]	VOLDA 2L[5]	VOLDA 2L[4]	VOLDA 2L[3]	VOLDA 2L[2]	VOLDA 2L[1]	VOLDA 2L[0]	18h
D5h	55h	CONT15	VOLDA 2R[7]	VOLDA 2R[6]	VOLDA 2R[5]	VOLDA 2R[4]	VOLDA 2R[3]	VOLDA 2R[2]	VOLDA 2R[1]	VOLDA 2R[0]	18h

VOLDA1L/R[7:0], VOLDA2L/R[7:0]: Input Digital Volume, L/R indipendent Setting available 0.5dB step 256 Level
(Page 59, Table 7)

■ Reset

1) Definition of reset state

The AK7742 has three types of reset function which are Initial reset, Clock reset and System reset. Operating condition (RUN state) is defined as when these reset are released. In the Initial reset condition, the IRESETN pin= "L" and all blocks DSP/PLL/ADC/DAC and etc. go sleep. The System reset condition is when the IRESETN pin= "H", SRESET bit= "0", PLL and VREF blocks are in operation and DSP/ADC/DAC are not in operation. Clock reset is one of the System reset but CKRST bit = "1". This mode can be used for changing a main clock or clock source when PLL and internal clock are stopped. After the Initial reset is released, during System reset, each register settings and program writings are made. Program down-loading to the DSP is prohibited until PLL oscillation is stabilized.

2) Initial reset

Initial reset is required to initialize all AK7742 blocks. As IRESETN pin= "L", all control registers are initialized, internal counters, ADC, DAC, DSP, PLL, etc. are stopped. When changing the IRESETN pin to "H", VREF circuit (Analog reference voltage) and PLL for master clock starts operating and control register writing become valid.

CKM[2:0] pin setting or main clock source must be changed during this initial reset. CKM[2:0] pins are related to main PLL circuit and internal counter control, therefore these pin sate changing on another state of the device may cause erroneous operation.

3) System reset

DSP Program download is executed in system reset. It is recommended that set all control registers except for SRESETN in this state. In system reset, ADC / DAC / DSP are stopped. VREF circuit and PLL are in operation. LRCK and BICK output is stopped if the AK7742 is in master mode. System reset state will be released when set SRESETN register to "1" and the AK7742 switches to RUN.

4) Clock Reset

CKM[2:0] pin settings and Input clock ICLK (XTI@CKM Mode 0/1/2 or BICK@CKM Mode 3/4/5) can be also changed during the clock reset as well as during initial reset.

By this reset, both the PLL and the internal clocks stop and clock selection can be safely done during System Reset. After System Reset, the AK7742 enters Clock Reset condition by setting the CKRST bit = "1" (CONT8 D1). Change pin settings and input clock frequency during Clock Reset. The PLL re-starts by exiting the clock reset condition (CKRST bit = "1" to "0") after those changes are made and the input clock settles to its final setting. Transmission of DSP program, Coefficient Data and other data from an external microcontroller is prohibited until the PLL reaches stable oscillation (50ms). After transferring DSP program, Coefficient Data and other data, the AK7742 returns to normal operation by bringing SRESETN bit to "1".

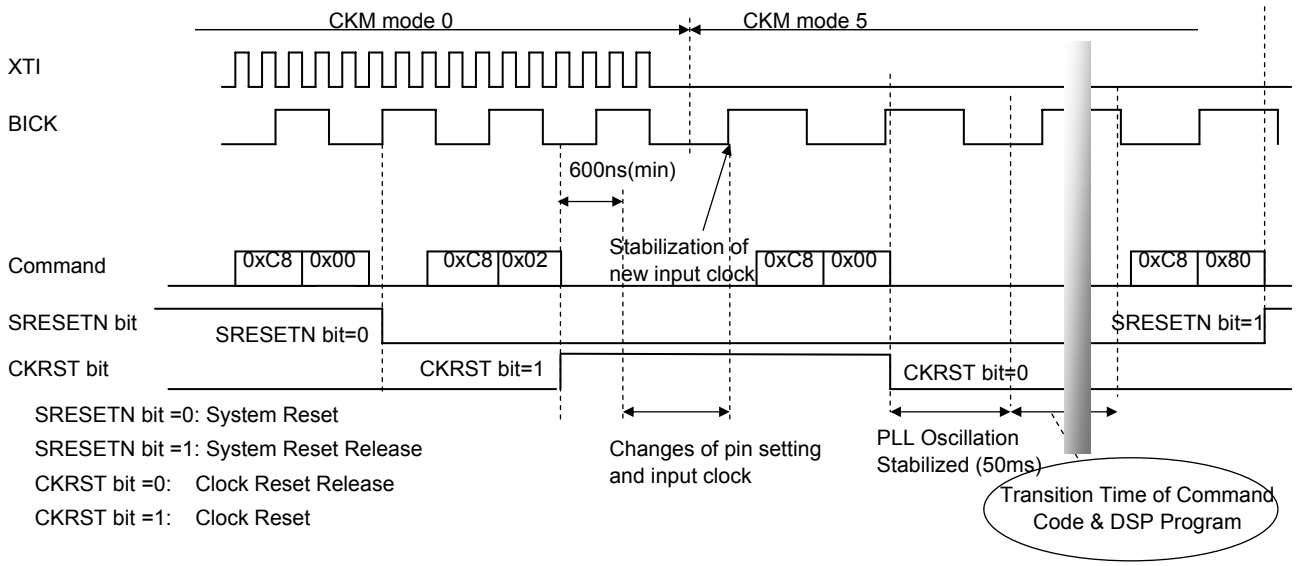


Figure 11. Clock Set Sequence (Ex: CKM Mode 0 → CKM Mode 5)

5) Operation state (RUN)

When system reset is released, DSP / ADC / DAC start operating. In this state, CRAM write process is required special procedure instead of normal download.

When the AK7742 is in slave mode (especially CKM mode 2), the main clock and LRCK / BICK have to be synchronized. In Run sate, the AK7742 generates internal LRCK reference clock by internal counter, and this clock adjusts the phase of LRCK inputs just after when the AK7742 switched to RUN. If the phase differences between internal LRCK reference and LRCK input clock becomes large (this may be caused by pulse noise for main clock), the data transition for outside block may be interfered. To avoid this, the DSP will be stopped to restart the phase adjustment process in this error state. In this time the data output will be unstable. This phase adjustment function is to prevent continuous error by noise, not to allow using asynchronous clocks.

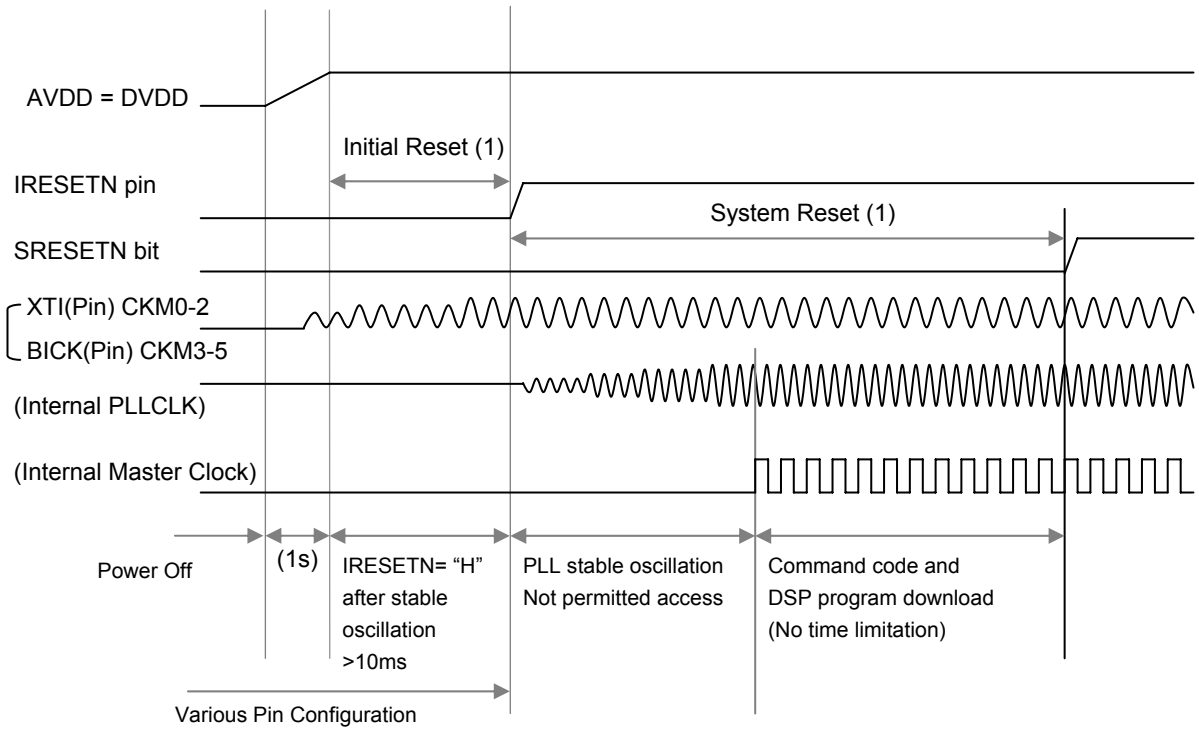
Phase adjustment function requires 4LRCK(max) time in slave mode and 1LRCK(max) time in master mode. ADC output will be available after 130LRCK(max) once the phase are adjusted. (2.75ms@fs=48kHz, 16.5ms@fs=8kHz).

■ Power Up/Down Sequence

1. Initial Reset Sequence

The AK7742 should be powered up at the IRESETN pin= "L". This initial reset initializes control resisters. AVDD and DVDD should be powered up at same time. When the IRESETN pin= "H", VREF circuit and main PLL start operating and the PLL generates internal main clock (MCLK). The interface with the AK7742 should be made after the PLL oscillation is stabilized. Normally the IRESETN pin initialization is required at powered up only.

Note 49. For a certain initialization, power must be completely up and master clock source must be supplied.
Note 50. In case of using crystal oscillator, set the IRESETN pin= "H" after stable oscillation. The time until stable oscillation depends on its characteristics and external circuits.
Note 51. External system clock (XTI) and bit clock (BICK) should not be stopped, except at Initial Reset or at Clock Reset. AVDD and DVDD should be powered-up at the same time and supplied from the same system power supply.



(1) System clock (XTI) and bit clock (BICK) should not be stopped, except at Initial Reset (IRESETN pin = "L") or at System Reset. The start-up order of AVDD and DVDD is not critical. However, all power supplies should be powered-up within 1sec.

Figure 12. Powered Up Sequence

2. Power Down Sequence

When power down the AK7742, AVDD and DVDD must be OFF at the same time and IRESERN pin must be “L”. Never supply any clocks to the AK7742 when powered down.

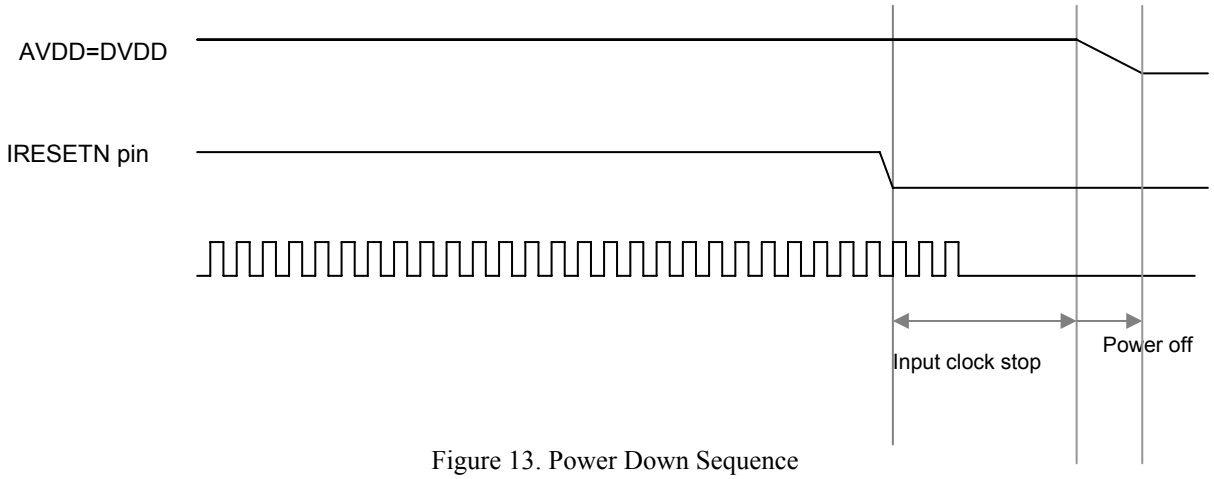


Figure 13. Power Down Sequence

■ RAM Clear

The AK7742 has RAM clear function. After the system reset release (RUN state), DRAM and DLRAM are cleared by “0”. The internal PLL must have stable oscillation before System reset. (Refer to ■ Power Up Sequence)The required time to clear RAM is about 200µs.
In the RAM clear sequence, it is possible to order command to DSP. (DSP is stopped during RAM clear sequence. The ordered command is accepted automatically after this sequence is completed.)

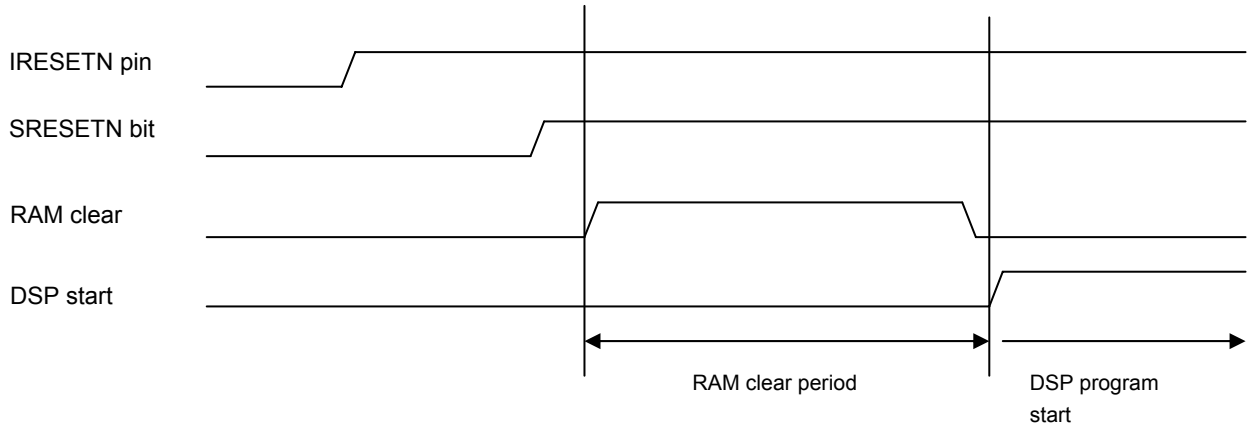


Figure 14. RAM Clear Sequence

■ Audio Data Interface

Serial audio data pins SDIN1-2, SDOUT1-3 are interfaced with external system, using LRCK / BICK clock. The data format is 2's compliment MSB first. I/O format supports MSB justified, LSB justified and I^2S compatible. (In case of using I^2S format, all interface become I^2S.) In CKM mode 4/5, PCM format is also supported.

The Input format of SDIN1-2 is MSB justified 24bit as default. LSB justified 24bit/20bit/16bit and I^2S are selectable by control register. The Output format of SDOUT1-3 is MSB justified 24bit as default. LSB justified 24bit/16bit and I^2S are selectable by control register.

1. MSB Justified (24bit), BICK64fs (DIFI2S= "0")

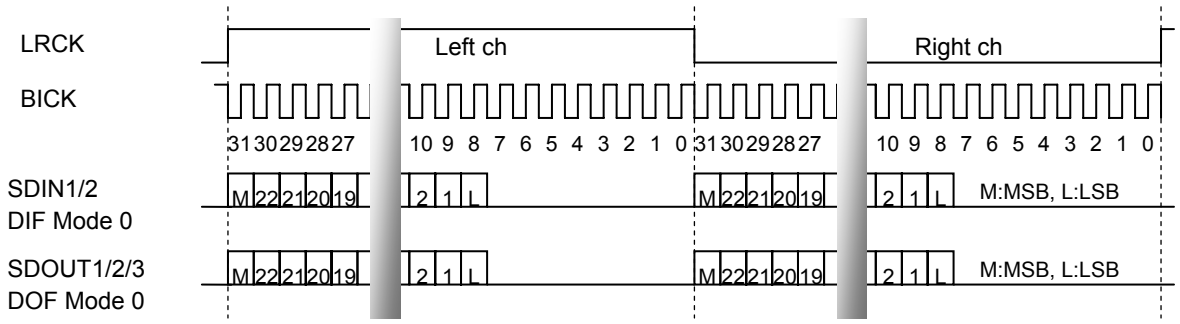


Figure 15. MSB justified (24bit), BICK64fs (DIFI2S= "0")

2. MSB Justified (24bit), BICK48fs (DIFI2S= "0")

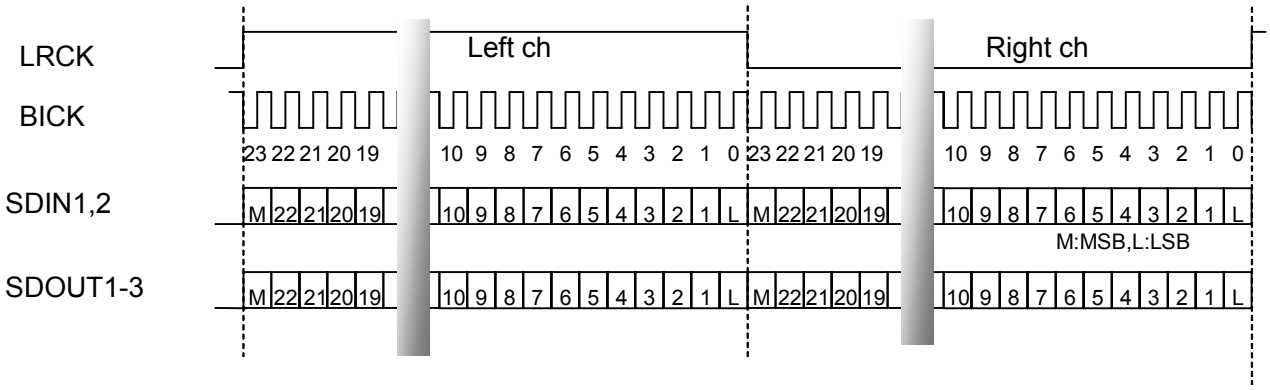


Figure 16. MSB justified (24bit), BICK48fs (DIFI2S= "0")

3. LSB Justified (24bit/20bit/16bit), BICK64fs (DIFI2S= “0”)

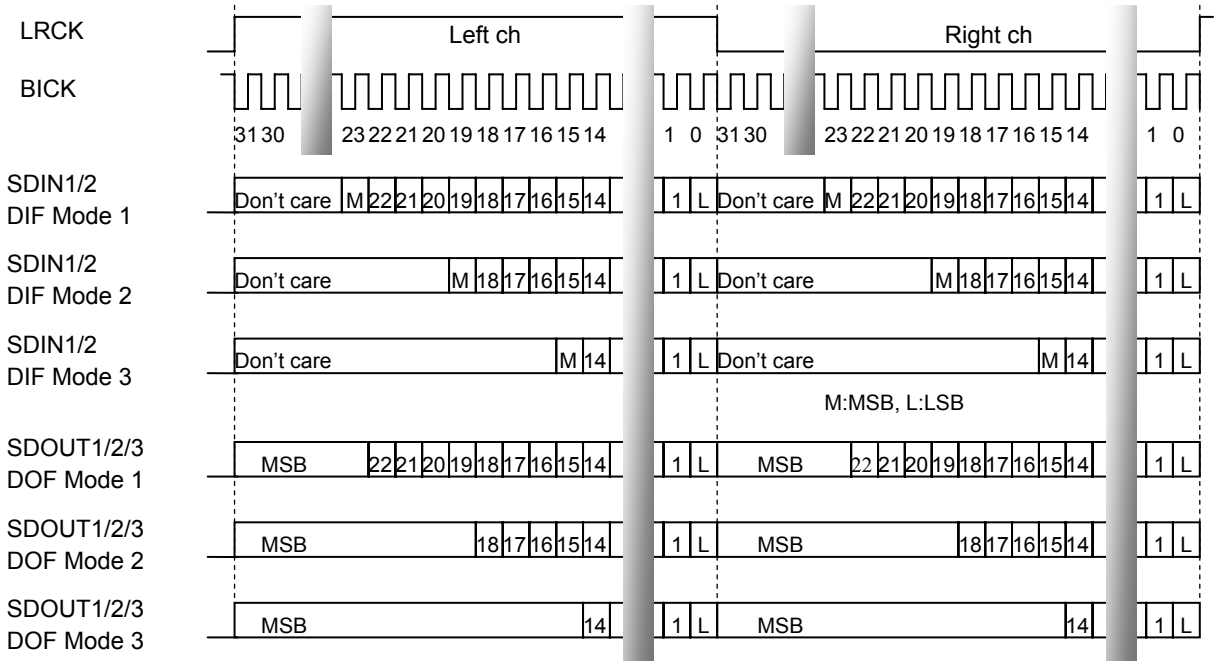
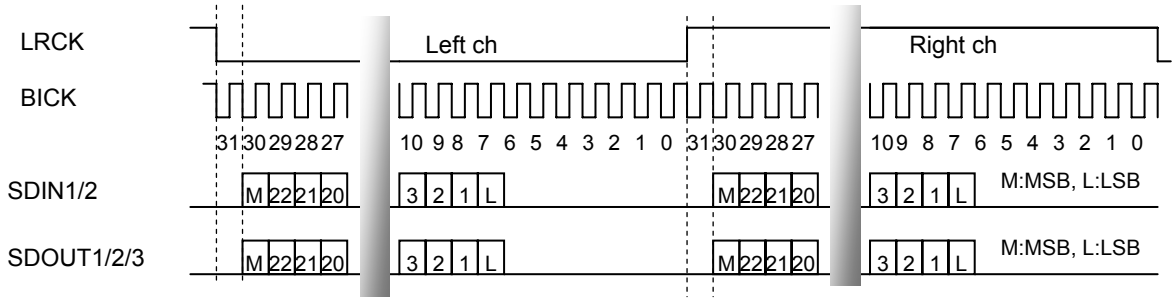


Figure 17. LSB justified (24bit/20bit/16bit), BICK64fs (DIFI2S= “0”)

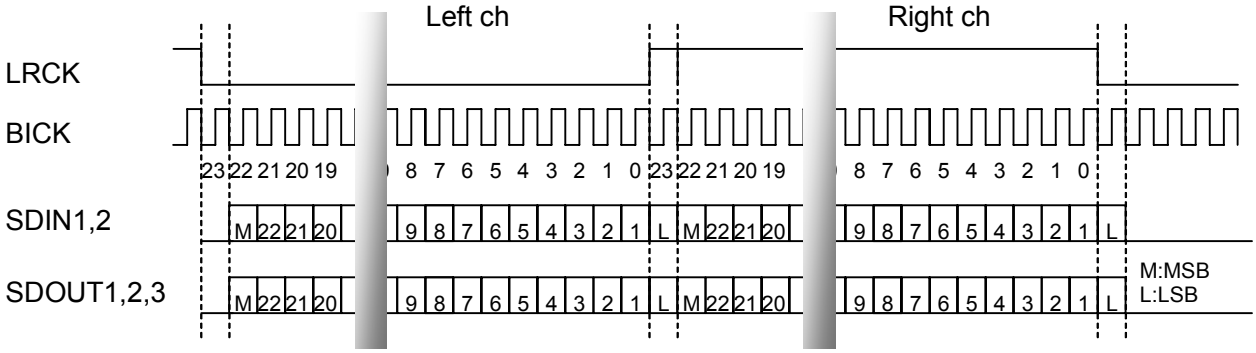
4. I²S Compatible (BICK=64fs)



In this mode, all I/O format is set to MSB justified (24bit).

Figure 18. I²S Compatible

5. I²S Compatible (BICK=48fs)



In this mode, all I/O format is set to MSB justified (24bit).

Figure 19. I²S Compatible

6. BICK 32fs (CKM Mode 4)

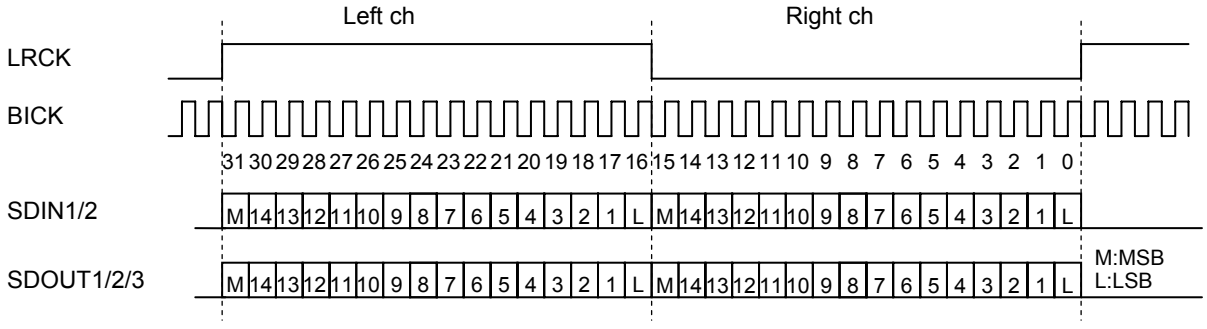


Figure 20. BICK 32fs (CKM Mode 4)

5. PCM Format

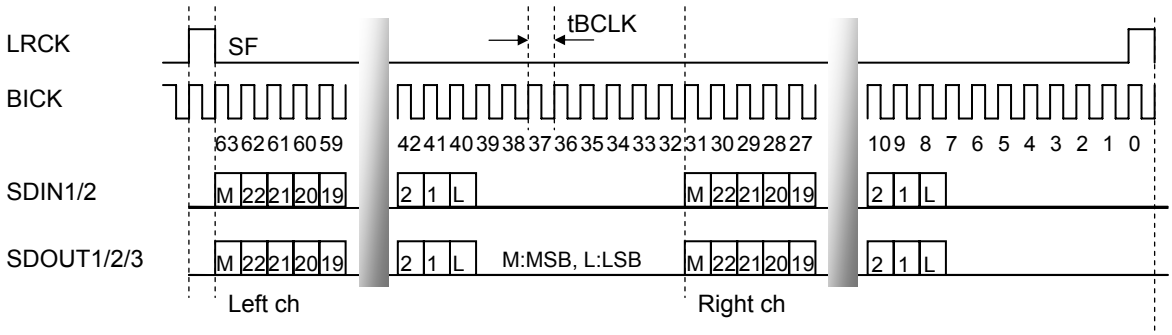


Figure 21. 64fs Short-frame, Rising-edge (CKM Mode 5)

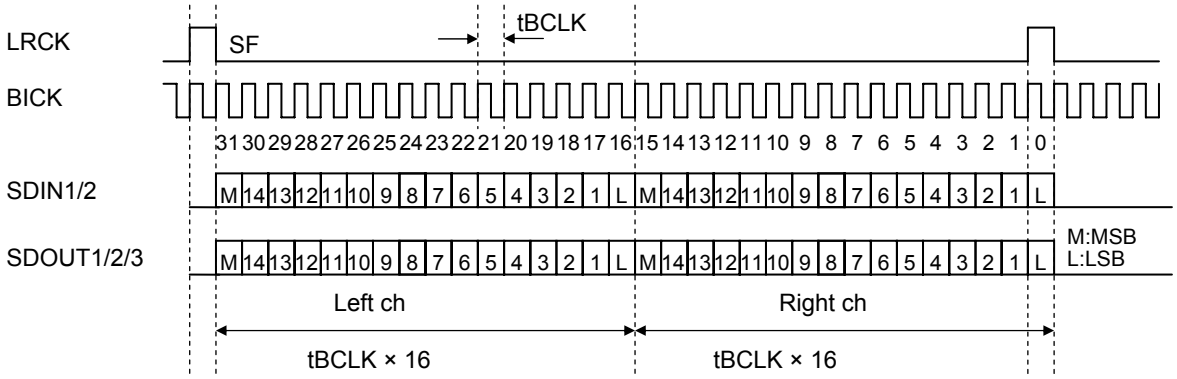


Figure 22. 32fs Short-frame, Rising-edge (CKM Mode 4)

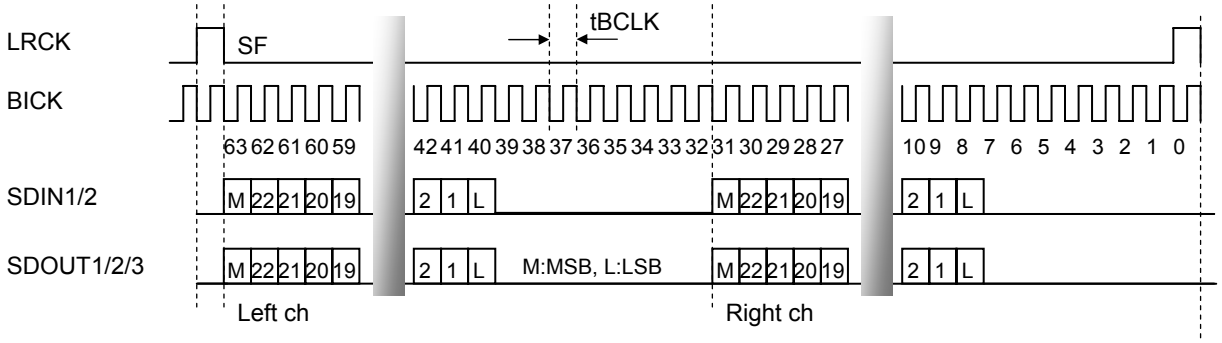


Figure 23. 64fs Short-frame, Falling-edge (CKM Mode 5)

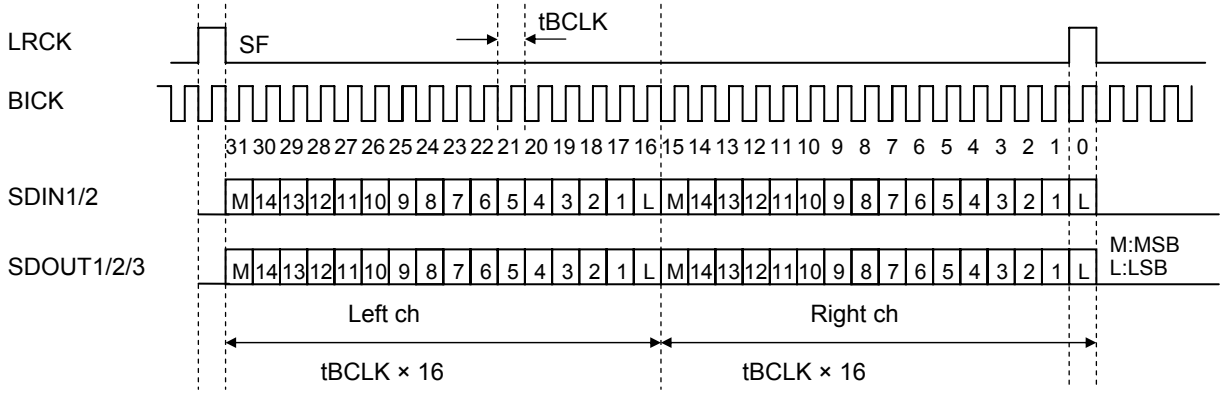


Figure 24. 32fs Short-frame, Falling-edge (CKM Mode 4)

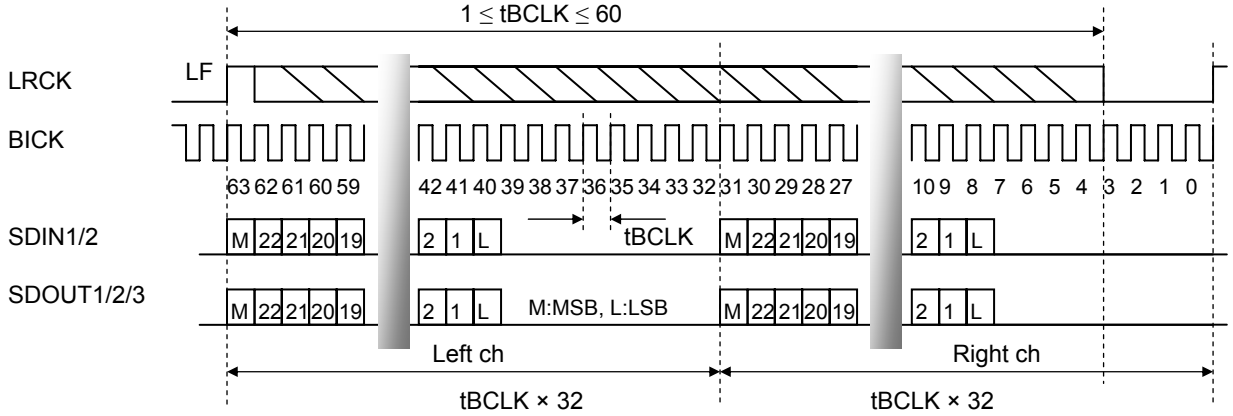


Figure 25. 64fs Long-frame, Rising-edge

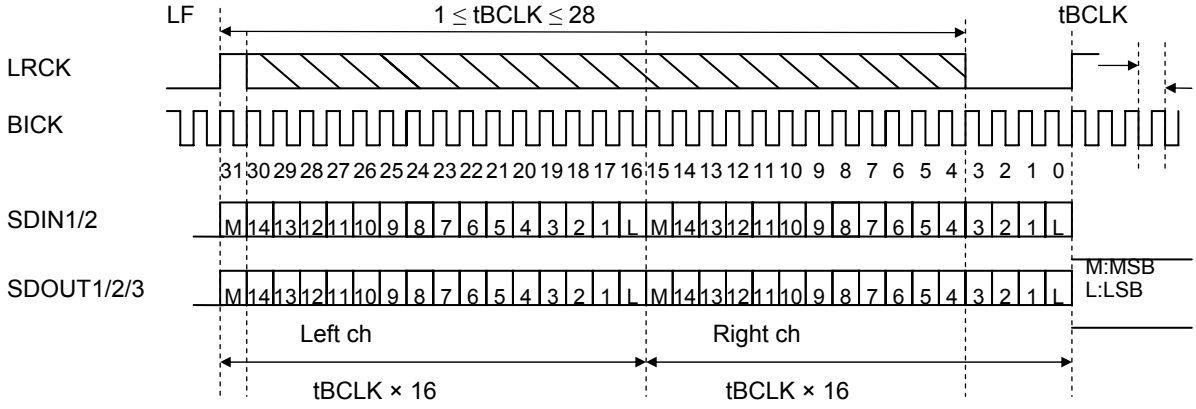


Figure 26. 32fs Long-frame, Rising-edge

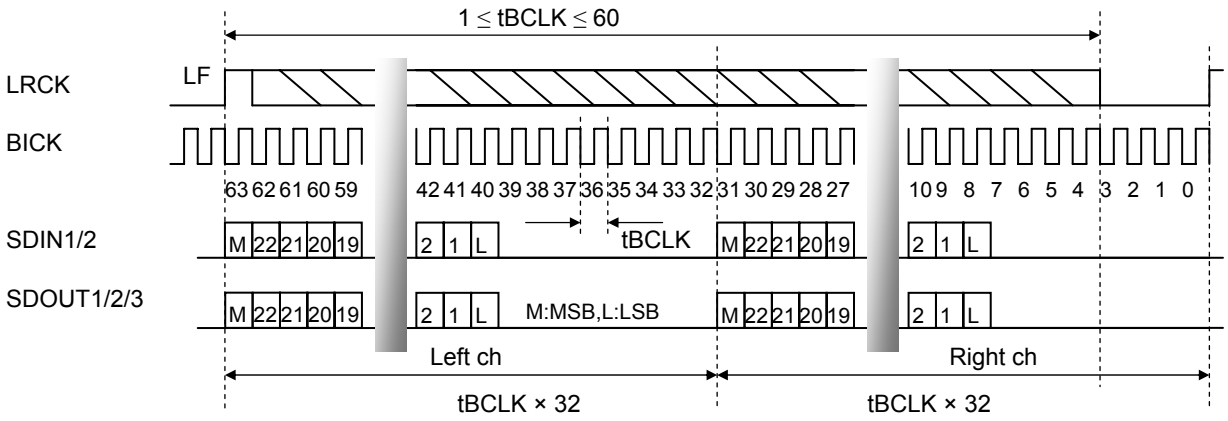


Figure 27. 64fs Long-frame, Falling-edge

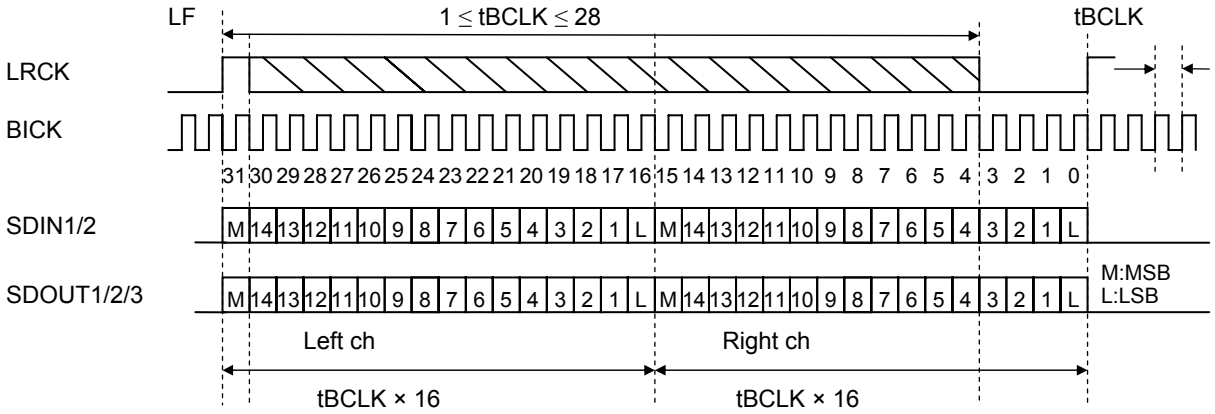


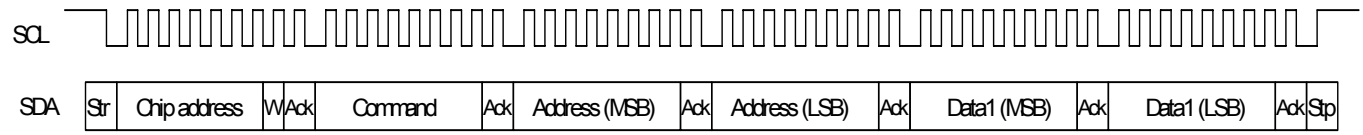
Figure 28. 32fs Long-frame, Falling-edge

■ Microcontroller Interface

1. Configuration

The access format is: Chip address (7bit) + Command code(8bit) + Address + Data

	Bit length	
Chip Address	7	fixed address as CAD[1:0] pin CAD[1:0]= "00": read 31h write 30h CAD[1:0]= "01": read 33h write 32h CAD[1:0]= "10": read 35h write 34h CAD[1:0]= "11": read 37h write 36h
Command	8	MSB bit is R/W flag. The followed 7bit indicates access area such as PRAM / CRAM / registers.
Address	16 / 0	Valid only for those cases where accessed areas have addresses such as PRAM / CRAM. When no address is assigned, there is no data.
Data	later section	Write data or Read data



ex) data access which has Address 16bit and Data 16bit.

2. Command Code

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R/W flag	Area to be accessed			Accompanying data to the access area			

R/W flag

Write at "1", Read at "0".

Access data and Accompanying data

BIT6	BIT5	BIT4	BIT3~0	
0	0	0	number of write	Prepare to write into CRAM on operation state
0	0	1	number of write	Prepare to write into OFRAM on operation state
0	1	0	0100/0010	execute writing into CRAM/OFRAM on operation state
0	1	1	1000/0100/0010	Write into PRAM/CRAM/OFRAM on system reset state
1	0	0	Register address	Registers to 0-15
1	1	0	0000	Device identify (Read only)
1	1	1	BIT0 is always 0 0100 0110 1000	special access JX write @MICR read @MIR2 read

3. Address

Address description is always LSB justified.
Accessing command code BIT[6:4]= “000” to “011” requires 16bit address.
Accessing command code BIT[6:4]= “100” to “111” requires no address.

4. Data

Length of write data is depending on the write area size. When accessing RAM, write data to sequential address locations by writing data continuously.

■Write command and data

command code	address	data length	content
80h~8Fh	16bit	16bit×(n+1) n: lower address	Write preparation while CRAM is running. BIT3 ~ BIT0 of the command code assign # of write operation (80h:1, 81h:2,…, 8Fh:16). Write operation exceeding the assigned # of write, abandons the data.
90h~9Fh	16bit	16bit×(n+1) n: lower address	Write preparation while OFRAM is running. BIT3 ~ BIT0 of the command code assign # of write operation (90h:1, 91h:2,…, 9Fh:16). Write operation exceeding the assigned # of write, abandons the data.
A2h	16bit	none	Execution of OFRAM writing in operation state. Address is ignored.
A4h	16bit	none	Execution of CRAM writing in operation state. Address is ignored.
B2h	16bit	16bit x n	Writing to OFRAM (in system reset state)
B4h	16bit	16bit x n	Writing to CRAM (in system reset state)
B8h	16bit	40bit x n	Writing to PRAM (in system reset state)
C0h~CFh	none	8bit	Writing to Register 0-15
F4h	none	8bit	Writing to JX code

Length of the read data is depending on the read area size. When accessing RAM, read data to sequential address locations by reading data continuously.

■Read

command code	address	data length	content
32h	16bit	16bit×n	Reading from OFRAM (in system reset state)
34h	16bit	16bit×n	Reading from CRAM (in system reset state)
38h	16bit	40bit×n	Reading from PRAM (in system reset state)
40h~4Fh	none	8bit	Reading from Register 0-15
60h	none	8bit	Device identification
76h	none	32bit	Read @MICR. 24-bit is upper-bit justified. Lower 4-bits are for validity flags. Valid at 0000.
78h	none	32bit	Read @MIR2. 24-bit is upper-bit justified. Lower 4-bits are for validity flags. Valid at 0000.

5. Data Format

[1] Write in system reset state

1. Program RAM (PRAM) write (during System Reset)

(1) COMMAND	B8h
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8
(3) ADDRESS2	A7-A0
(4) DATA1	0 0 0 0 D35 D34 D33 D32
(5) DATA2	D31-D24
(6) DATA3	D23-D16
(7) DATA4	D15-D8
(8) DATA5	D7-D0
	(It is possible to write data to sequential address by 1word:5byte unit)

2. Coefficient RAM (CRAM) write (during System Reset)

(1) COMMAND	B4h
(2) ADDRESS1	0 0 0 0 0 0 A9 A8
(3) ADDRESS2	A7-A0
(4) DATA1	D15-D8
(5) DATA2	D7-D0
	(It is possible to write data to sequential address by 1word:2byte unit)

3. Offset RAM (OFRAM) write (during System Reset)

(1) COMMAND	B2h
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 D12 D11 D10 D9 D8
(5) DATA2	D7-D0
	(It is possible to write data to sequential address by 1word:2byte unit)

[2] Write in system reset state and in operation state

1. Control register write (during System Reset and RUN)

(1) COMMAND	C0h-DFh
(2) DATA	D7-D0

Note 52. Some registers have limitation in operation state.

2.External jump code (JX) write (during System Reset and RUN)

(1) COMMAND	F4h
(2) DATA	D7-D0

[3] Write in operation state

1. Coefficient RAM (CRAM) write (during RUN)

Preparation	Input
(1) COMMAND	80h-8Fh (80h means number of data is one, 8Fh means number of data is 16)
(2) ADDRESS1	0 0 0 0 0 0 A9 A8
(3) ADDRESS2	A7-A0
(4) DATA1	D15-D8
(5) DATA2	D7-D0
	(It is possible to write data to sequential address by 1word:2byte unit)

Note 53. The COMMAND determines the length of the data. If the written data exceeds the allotted amount, the excess data is ignored.

Execute	Input
(1) COMMAND	A4h
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0

2. Offset RAM (OFRAM) write (during RUN)

Preparation	Input
(1) COMMAND	90h-9Fh (90h means number of data is one, 9Fh means number of data is 16)
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 D12 D11 D10 D9 D8
(5) DATA2	D7-D0
	(It is possible to write data to sequential address by 1word:2byte unit)

Note 53. The COMMAND determines the length of the data. If the written data exceeds the allotted amount, the excess data is ignored.

Execute	Input
(1) COMMAND	A2h
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0

[4] Read in system reset

1. Program RAM (PRAM) read (during System Reset)

	Input	Output
(1) COMMAND	38h	
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8	
(3) ADDRESS2	A7-A0	
(4) DATA1		0 0 0 0 D35 D34 D33 D32
(5) DATA2		D31-D24
(6) DATA3		D23-D16
(7) DATA4		D15-D8
(8) DATA5		D7-D0
	(It is possible to read data from sequential address by 1word:5byte unit)	

2. Coefficient RAM (CRAM) read (during System Reset)

	Input	Output
(1) COMMAND	34h	
(2) ADDRESS1	0 0 0 0 0 0 A9 A8	
(3) ADDRESS2	A7-A0	
(4) DATA1		D15-D8
(5) DATA2		D7-D0
	(It is possible to read data from sequential address by 1word:2byte unit)	

3. Offset RAM (OFRAM) read (during System Reset)

	Input	Output
(1) COMMAND	32h	
(2) ADDRESS1	0 0 0 0 0 0 0 0	
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0	
(4) DATA1		0 0 0 D12 D11 D10 D9 D8
(5) DATA2		D7-D0
	(It is possible to read data from sequential address by 1word:2byte unit)	

[5] Read in system reset state and in operation state

1. Control register read (during System Reset and RUN)

	Input	Output
(1) COMMAND	40h-5Fh	
(2) DATA		D7-D0

2. Device identification (during System Reset and RUN)

	Input	Output							
(1) COMMAND	60h								
(2) DATA		D7	D6	D5	D4	D3	D2	D1	D0
		0	1	0	0	0	0	1	0
		4				2			

[6] Read in operation state

1. @MICR read (during RUN)

	Input	Output
(1) COMMAND	76h	
(2) DATA1		D27-D20
(3) DATA2		D19-D12
(4) DATA3		D11-D4
(5) DATA4		D3 D2 D1 D0 (flag) (flag) (flag) (flag)

Note 54. Flag bit all “0” shows that data is valid.

2. @MIR2 read (during RUN)

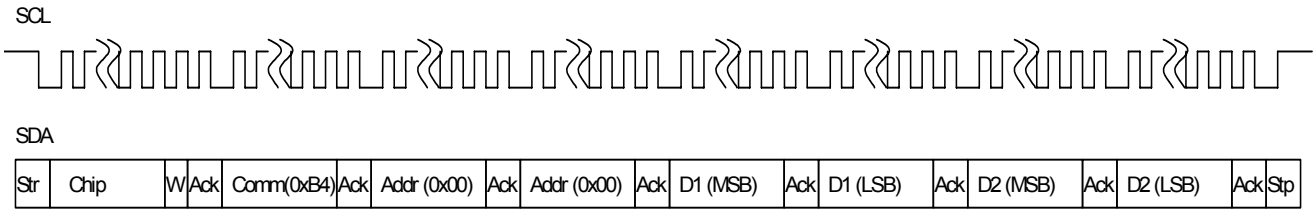
	Input	Output
(1) COMMAND	78h	
(2) DATA1		D27-D20
(3) DATA2		D19-D12
(4) DATA3		D11-D4
(5) DATA4		D3 D2 D1 D0 (flag) (flag) (flag) (flag)

Note 54. Flag bit all “0” shows that data is valid.

6. Timing

[1] RAM writing timing during System Reset.

Write to Program RAM (PRAM), Coefficient RAM (CRAM) and Offset RAM (OFRAM) during System Reset in the order of Command code, Address and Data. When writing Data to consecutive address locations, continue to input data only.



In this example, command code is B4h which shows CRAM write in system reset state. Address is 0000h.
Data are 2word D1 and D2, it is possible to write continuously if there were more data.

[2] RAM writing timing during RUN

Use this operation to rewrite Coefficient RAM (CRAM) during RUN. After inputting the assigned command code (8-bit) to select the number of data from 1 to 16, input the Starting Address of write and the number of data assigned by command code in this order (write preparation). Upon completion of this operation, execute RAM write during RUN by inputting the corresponding command code and address (16-bit all 0) in this order (write execution).

Write modification of RAM contents is executed whenever the RAM address for modification is assigned. For example, when 5 Data are written from RAM address “10”, it is executed as shown below.

CRAM pointer renew	7	8	9	10	11	13	16	11	12	13	14	15
				↓	↓				↓	↓	↓	
Changing timing				○	○	↑			○	○	○	

Note: Address “13” is not executed until rewriting address “12”.

Note 55. Execute Write preparation before a write execution. When writing to RAM without write preparation sequence, a malfunction occurs.

Note 56. In case that the DSP program is designed to refer all coefficient which may be changed by an external microcontroller, this write operation will finish within 2LRCK after a writing command. No further access to DSP is permitted until this write operation is completed.

[3] External Conditional Jump (JX)

External Conditional Jump code writing (during Reset and RUN)

(1) COMMAND	F4h
(2) DATA	D7~D0

Write the External Conditional Jump code after all necessary operations such as program downloading are finished. It can be input during both system Reset and RUN. Input data is set to the designated register with synchronizing to LRCK. When any data in a 10-bit External Jump code, which consists of an 8-bit code and external input pin information JX0 and JX1, matches any single bit of "1" in the IFCON field, a Jump instruction is executed. Write data during Reset before the release of Reset after transfer of all data. IFCON field is the area where the external conditions are written. This Jump code is reset to 00h by setting the IRESETN pin to "L", but it is not reset by System reset.

	7	6	5	4	3	2	1	0	JX 0	JX 1
External jump code	■	■	■	■	■	■	■	■	□	□
				↑						
Checking on each bit equal to "1"										
	16			↓				9	8	7
IFCON bit field	♦	♦	♦	♦	♦	♦	♦	♦	♦	♦

Note 57. Jump code transition will be finished within two LRCK clock cycles after the command is established.

[4] RAM reading timing during System Reset

Reading from Program RAM (PRAM), Coefficient RAM (CRAM) and Offset RAM (OFRAM) are possible during system reset. Establish command code and address, and then read. Reading from sequential address is possible by reading continuously.

[5] Control register reading during System Reset and RUN

Reading from Control register and device identification code are valid in system reset and RUN. Input command code. The reading data after inputting command code will be register values or device identifying coeds.

■ I²C BUS INTERFACE (I2CSEL= "H")

Access to the AK7742 registers and RAM is processed by I²C bus. The format of the I²C is complement with fast mode (max: 400kHz). The AK7742 does not support HS mode. (max: 3.4MHz).

1. Data Transfer

In order to access any IC devices on the I²C BUS, input a start condition first, followed by a single Slave address which includes the Device Address. IC devices on the BUS compare this Slave address with their own addresses and the IC device which has an identical address with the Slave-address generates an acknowledgement. An IC device with the identical address then executes either a read or write operation. After the command execution, input a Stop condition.

1-1. Data Change

Change the data on the SDA line while SCL line is "L". SDA line condition must be stable and fixed while the clock is "H". Change the Data line condition between "H" and "L" only when the clock signal on the SCL line is "L". Change the SDA line condition while SCL line is "H" only when the start condition or stop condition is input.

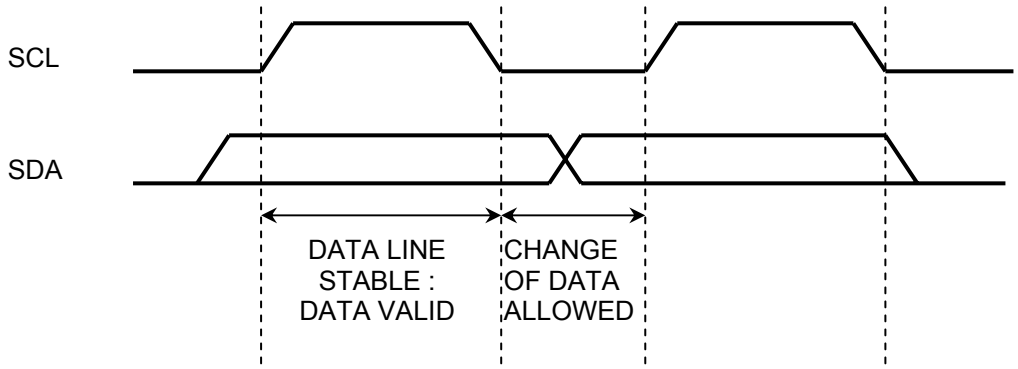


Figure 29. Data Transition

1-2. Start condition and Stop condition

Start condition is generated by the transition of "H" to "L" on the SDA line while the SCL line is "H". All instructions are initiated by Start condition. Stop condition is generated by the transition of "L" to "H" on SDA line while SCL line is "H". All instructions end by Stop condition.

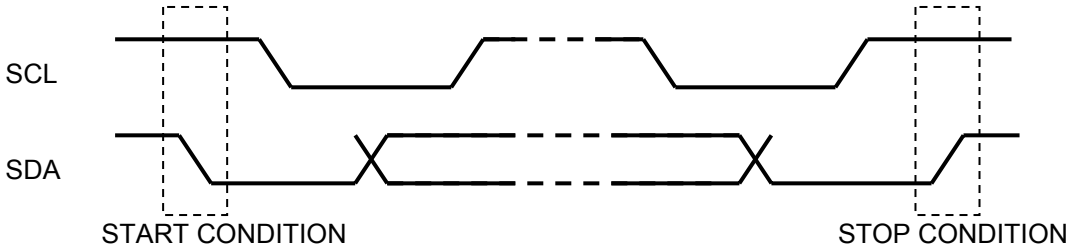


Figure 30. Start Condition and Stop Condition

1-3. Repeated Start Condition

When Start condition is received again instead of Stop condition, the bus changes to Repeated Start condition. Repeated Start condition is functionally the same as Start condition.

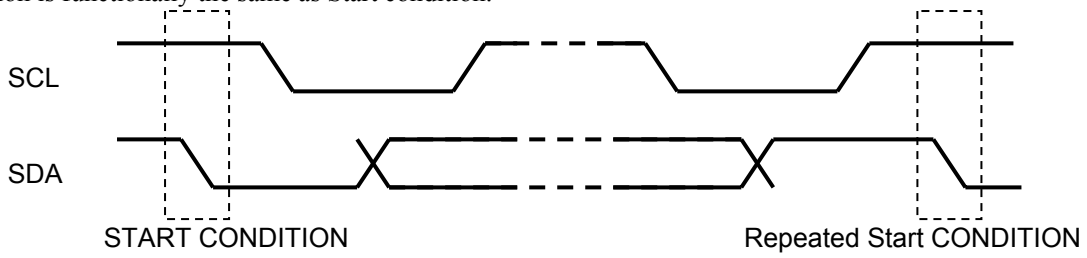


Figure 31. Repeated Start Condition

1-4. Acknowledge

An external device that is sending data to the AK7742 releases the SDA line ("Hi-Z") after receiving one-byte of data. An external device that receives data from the AK7742 then sets the SDA line to "L" at the next clock. This operation is called "acknowledgement" and it enables verification that the data transfer has been properly executed. The AK7742 generates an acknowledgement upon receipt of Start condition and Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK7742 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the Master side generates an acknowledgement without sending Stop condition, the AK7742 outputs data at the next address location. When no acknowledgement is generated, the AK7742 ends data output (not acknowledged).

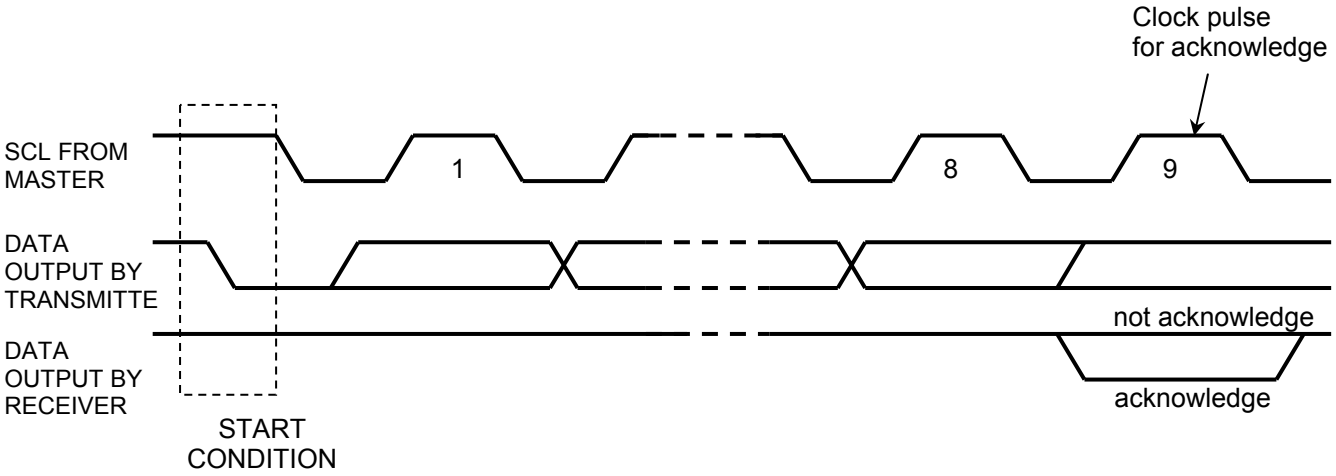


Figure 32. Acknowledge

1-5. The First byte

The First Byte, which includes the Slave-address that is input after Start condition, and a target IC device that will be accessed on the bus is selected by the Slave-address. The Slave-address is configured with the upper 7-bits. Data of the upper 5 bits is "00110". The next 2 bits are address bits that select the desired IC, which are set by the CAD1 and CAD0 pins. When the Slave-address is input, an external device that has the identical device address generates an acknowledgement and instructions are then executed. The 8th bit of the First Byte (lowest bit) is allocated as the R/W bit. When the R/W bit is "1", a read instruction is executed, and when it is "0", a write instruction is executed.

In this document, there is a case that describes a "Write Slave-address assignment" when both address bits match and a Slave-address at R/W bit = "0" is received. There is a case that describes "Read Slave-address assignment" when both address bits matches and a Slave-address at R/W Bit = "1" is received.

0	0	1	1	0	CAD1	CAD0	R/W

(CAD1 and CAD0 are set by pin settings)

Figure 33. The First Byte Structure

1-6. The Second and Succeeding byte

The data format of the second and succeeding bytes of the AK7742 Transfer / Receive Serial data (command code, address and data in microcontroller interface format) on the I2C BUS are all configured with a multiple of 8-bits. When transferring or receiving those data on the I2C BUS, they are divided into an 8-bit data stream segment and they are transferred / received with the MSB side data first with an acknowledgement in-between. A divided example is shown here.

Example) When transferring / receiving A1B2C3 (hex) 24-bit serial data in microcontroller interface format :

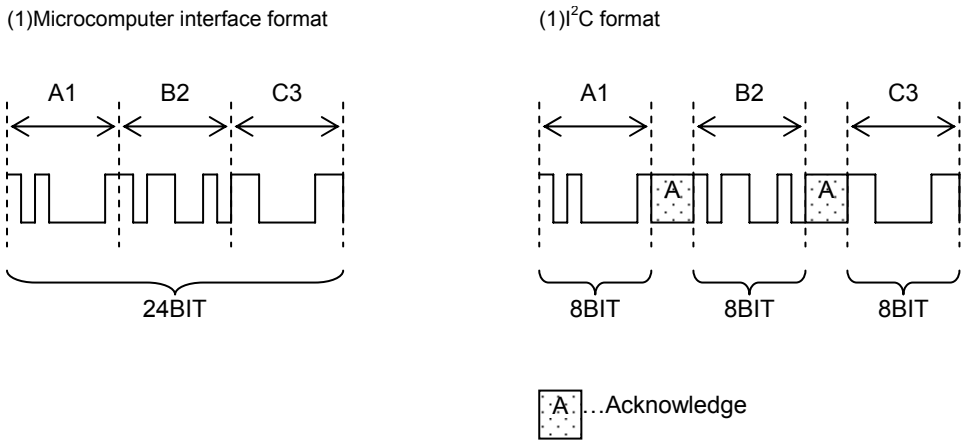


Figure 34. Division of data

In this document, there is a case that describes a write instruction command code which is received at the second byte as "Write Command". There is a case that describes a read instruction command code which is received at the second byte as "Read Command"

2. Write Sequence

In the AK7742, when a "Write-Slave-address assignment" is received at the first byte, the write command at the second byte and data at the third and succeeding bytes are received. At the data block, address and write data are received in a single-byte unit each in accordance with a command code. The number of write data bytes (*1 in Figure 35) is fixed by the received command code.

Usable command codes in write sequence are listed below as "(Table 1) Write Command".

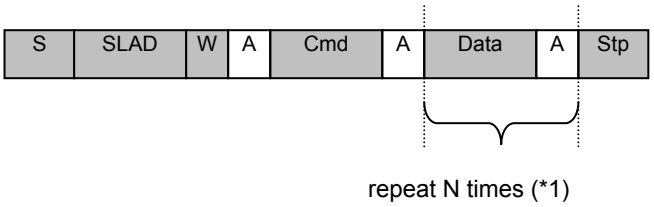


Figure 35. Write Sequence

Command Code	Address	Data length	Content
80h-8Fh	2byte	2byte×(n+1) n: Lowest address	Write preparation while CRAM is running. BIT3 ~ BIT0 of the command code assign # of write operation (80h:1, 81h:2,…, 8Fh: 16). Write operation exceeding the assigned # of write, abandons the data.
90h-9Fh	2byte	2byte×(n+1) n: Lowest address	Write preparation while OFRAM is running. BIT3 ~ BIT0 of the command code assign # of write operation (80h:1, 81h:2,…, 8Fh: 16). Write operation exceeding the assigned # of write, abandons the data.
A2h	2byte	none	Execution of OFRAM write in operation state. Address is ignored.
A4h	2byte	none	Execution of CRAM write in operation state. Address is ignored.
B2h	2byte	2byte×n	Write to OFRAM (in system reset state)
B4h	2byte	2byte×n	Write to CRAM (in system reset state)
B8h	2byte	5byte×n	Write to PRAM (in system reset state)
C0h-CFh	none	1byte	Write to Register 0-15
F4h	none	1byte	Write to JX code

Note 58. Length of write data is variable with the area to be written. When accessing RAM for writing, it is possible to write data at sequential address locations by writing data continuously.

Table 1. Write Command

3. Read Sequence

In the AK7742, when a "write- slave-address assignment" is received at the first byte, the read command at the second byte and the data at the third and succeeding bytes are received. At the data block, the address is received in a single byte unit in accordance with a read command code. In a command code without an address assignment, the sequence does not have to be repeated (*2 in Figure 36).

When the last address byte (or command code if no address assignment is specified) is received and an acknowledgement is transferred, the read command waits for the next restart condition. When a "read- slave-address assignment" is received in the first byte, data is transferred at the second and succeeding bytes. The number of readable data bytes (*3 in Figure 36) is fixed by the received read command.

After reading the last byte, assure that a "not acknowledged" signal is received. If this "not acknowledged" signal is not received, the AK7742 continues to send data regardless whether data is present or not, and since it did not release the BUS, the stop condition cannot be properly received.

Usable command codes in the read sequence are listed in the following "(Table 2) Read Command".

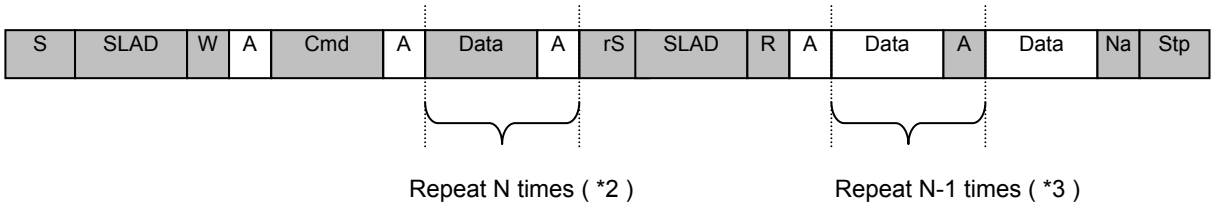


Figure 36. Read Sequence

Command Code	Address	Data length	Content
32h	2byte	2byte×n	Read from OFRAM (in system reset state)
34h	2byte	2byte×n	Read from CRAM (in system reset state)
38h	2byte	5byte×n	Read from PRAM (in system reset state)
40h-4Fh	none	1byte	Read from Register 0-15
60h	none	1byte	Device identification
76h	none	4byte	Read @MICR. 28-bit data is upper-bit-justified. Lower 4-bits are for validity flags. Valid at 0000.
78h	none	4byte	Read @MIR2. 28-bit data is upper-bit-justified. Lower 4-bits are for validity flags. Valid at 0000.

Note 59. Length of data is variable with the area to be read. As for access to RAM, it is possible to read data at sequential address locations by reading data continuously.

Table 2. Read Command

When Read Slave-address assignment is received without receiving Read command code.

Data read in the AK7742 can be made only in the previously documented Read sequence. Data cannot be read out without receiving a read command code. In the AK7742, a "Not Acknowledged" is generated when a "Read Slave-address Assignment" without proper receipt of read command. Under this condition, which occurs when RDY pin shifts from low level to high level after a "Write Slave-address assignment" in the read sequence and before a "Read Slave-address assignment", "Not Acknowledged" is generated in return.

This condition may be avoided by assigning a read Slave-address only when the acknowledgement is confirmed, by utilizing the acknowledge-polling feature.

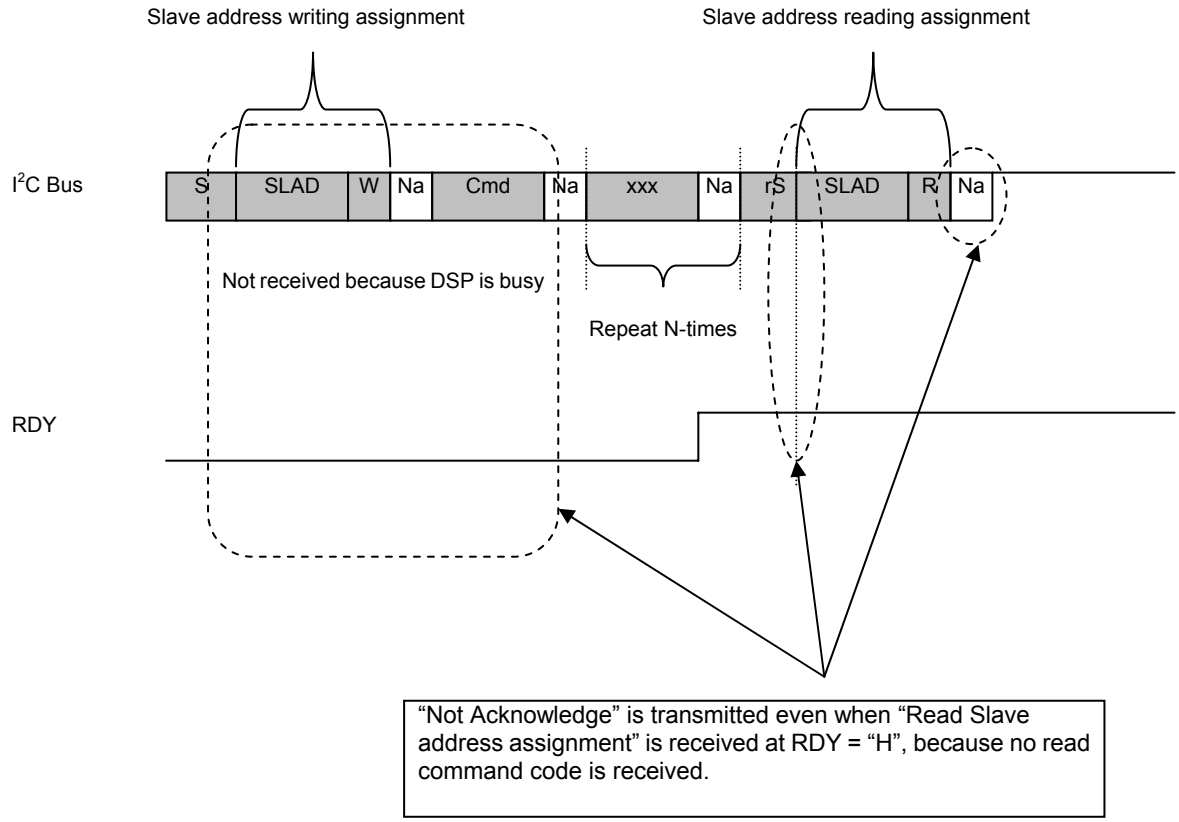


Figure 37. Not acknowledge response in read sequence

Note: The meaning of symbols in the I^2C format figures

SLAD	•••SlaveAddress (7 bits)
Cmd	•••Command Code (8 bits)
S	•••StartCondition
rS	•••Repeated StartCondition
Stp	•••StopCondition
W	•••R / W bit, the lowest bit of the first byte is at write (= 0) condition, Write (1 bit)
R	•••R / W bit, the lowest bit of the first byte is at read (= 1) condition, Read (1 bit)
A	•••Acknowledge (1 bit)
Na	•••NotAcknowledge (1 bit)
(Gray)	••• (Gray) where it is controlled by Master device.
(White)	••• (White) where it is controlled by Slave device. It is done by the AK7742.

■ ADC block

1. ADC High-pass filter

The AK7742 ADC has digital High Pass Filter (HPF) for DC offset cancellation. The cut-off frequency of the HPF is approximately 1Hz (at fs=48kHz). This cut-off frequency is proportional to the sampling frequency.

Sampling frequency (fs)	48kHz	44.1kHz	8kHz
Cut-off frequency	0.93Hz	0.86Hz	0.16Hz

Table 3. Cut-off Frequency of the High Pass Filter

2. Soft mute

The ADC block has digital soft mute circuit. When the ADSMUTE bit goes to "1", the output signal is attenuated by -∞ during ATT_DATA x ATT transition time from the current ATT level. When the ADSMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level in ATT_DATA x ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission. The transition time is 912 LRCK clock (depends on DATT register setting).

The soft mute function works when the ADC is in operation.
ATT_DATA is initialized by the INITRSTN pin = "L".

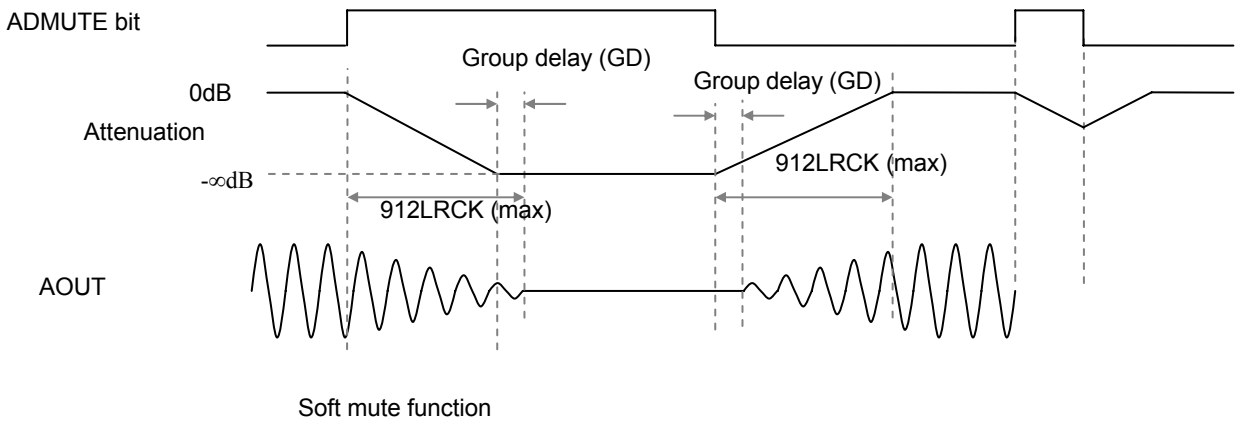


Figure 38. Soft Mute

3. Changing input selector

When changing the ADC input selector, execute soft mute first to reduce pop noise. Selector switching must be made during period (2). It requires about 200ms (3) to release the soft mute.

ADC input selector change sequence
- Execute soft mute
- Change selector
- Release soft mute

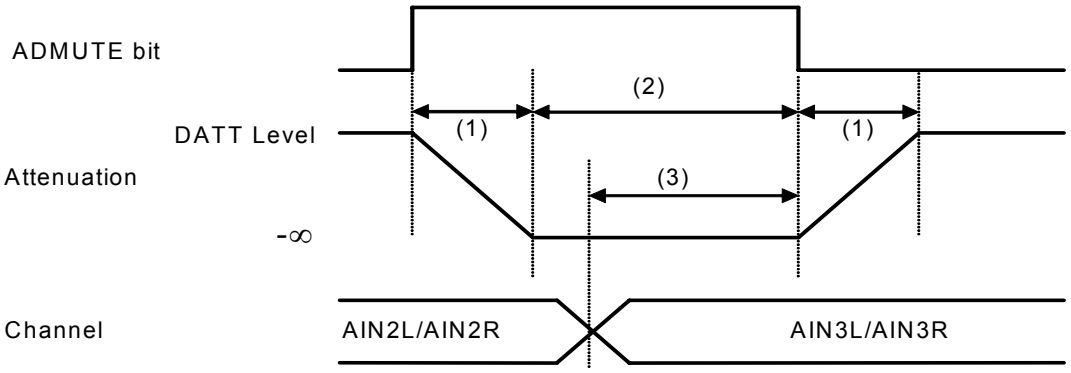


Figure 39. Input Selector Change

The transition time period (1) is depended on ATSPAD bit register setting.

ATSPAD bit (CONT1 D7)	Period (1) (max)			
	LRCK cycle	fs=48kHz	fs=44.1kHz	fs=8kHz
0	912LRCK	19ms	20.68ms	114ms
1	912LRCK x 4	76ms	82.72ms	456ms

Figure 40. Soft Mute Transition Time

4. ADC Digital Volume

The AK7742 has channel-independent digital volume control (256 levels, 0.5dB step).
The VOLADL[7:0] and VOLADR[7:0] bit set the volume level of each ADC channel.

ADC Lch VOLADL [7:0]	ADC Rch VOLADR [7:0]	Attenuation Level	
00h	00h	+24.0dB	
01h	01h	+23.5dB	
02h	02h	+23.0dB	
:	:	:	
2Fh	2Fh	+0.5dB	
30h	30h	0.0dB	(default)
31h	31h	-0.5dB	
:	:	:	
FDh	FDh	-102.5dB	
FEh	FEh	-103.0dB	
FFh	FFh	Mute (-∞)	

Table 4. ADC Digital Volume Level Setting

Transition time between set values of VOLADL[7:0] and VOLADR[7:0] bits can be selected by ATSPAD bit.

Mode	ATSPAD bit	Attenuation speed	
0	0	1/fs	(default)
1	1	4/fs	

Table 5 Transition Time between set values of VOLADL[7:0], VOLADR[7:0] bits

The transition between set values is soft transition of 1021 levels in Mode 0. It takes 1021/fs (21.3ms@fs=48kHz) from 00H to FFH(MUTE) in Mode 0. If the INITRSTN pin goes to “L”, the VOLADL[7:0] and VOLADR[7:0] bits are initialized to 30h.

■ DAC block

1. De-emphasis Filter Control

The AK47742 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter corresponding to f 48kHz sampling frequency. DEM1[1:0] bits control the de-emphasis filter for DAC1 and DEM2[1:0] bits control the de-emphasis filter for DAC2.

DEM Mode	DEM[1:0] bit	fs	
0	00	Off	(default)
1	01	48KHz	
2	10	44.1KHz	
3	11	32KHz	

Table 6. De-emphasis Control

2. DAC Digital Volume control

The DACs of the AK7742 have channel-independent digital volume control (256 levels, 0.5dB step). The VOLDA1L[7:0] and VOLDA1R[7:0] (DAC1), VOLDA2L[7:0] and VOLDA2R[7:0] (DAC2) bits set the volume level of each DAC channel.

VOLDA2L[7:0] byte VOLDA2R[7:0] byte VOLDA1L[7:0] byte VOLDA1R[7:0] byte	Attenuation Level	
00h	+12dB	
01h	+11.5dB	
02h	+11.0dB	
17h	+0.5dB	
18h	0.0dB	(default)
19h	-0.5dB	
FDh	-114.5dB	
FEh	-115dB	
FFh	Mute	

Table 7. DAC1 and DAC2 Digital Volume Level Setting

Transition time between set values can be selected independently by ATSPDA bit.

Mode	ATSPDA bit	Attenuation speed	
0	0	1/fs	(default)
1	1	4/fs	

Table 8. DAC1 and DAC2 Volume Transition Time

The transition between set values is soft transition of 1021 levels in Mode 0. It takes 1021/fs (21.3ms@fs=48kHz) from 00H to FFH(MUTE) in Mode 0. If the INITRSTN pin goes to “L”, the VOLDA2L[7:0], VOLDA2R[7:0], VOLDA1L[7:0] and VOLDA1R[7:0] bits are initialized to 18H.

3. DAC Soft mute control

The DACs have a soft mute function. The soft mute operation is performed at digital domain. When the DA1MUTE and DA2MUTE bits go to "1", the output signal is attenuated by -∞ during ATT_DATA x ATT transition time from the current ATT level. When the DA1MUTE and DA2MUTE bits are returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level in ATT_DATA x ATT transition time. If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The soft mute function works when the DAC section is in operation. After the output signal is attenuated by -∞, DA1RST bit = "0", DA2RST bit = "0" or SRESETN bit= "0" resets the DAC block. As some click noise occurs at the edge of RSTN signal, the analog output should be muted externally if click noise aversely affect system performance. An attenuation value is initialized by the INITRSTN pin = "L"

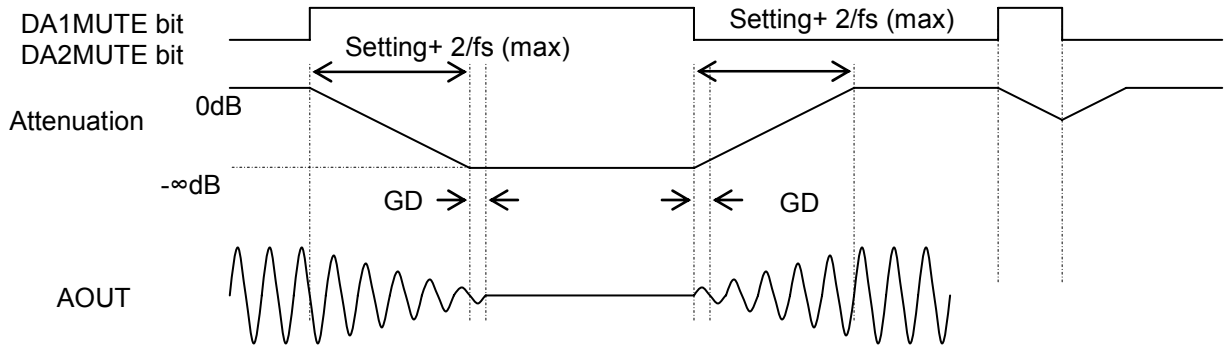
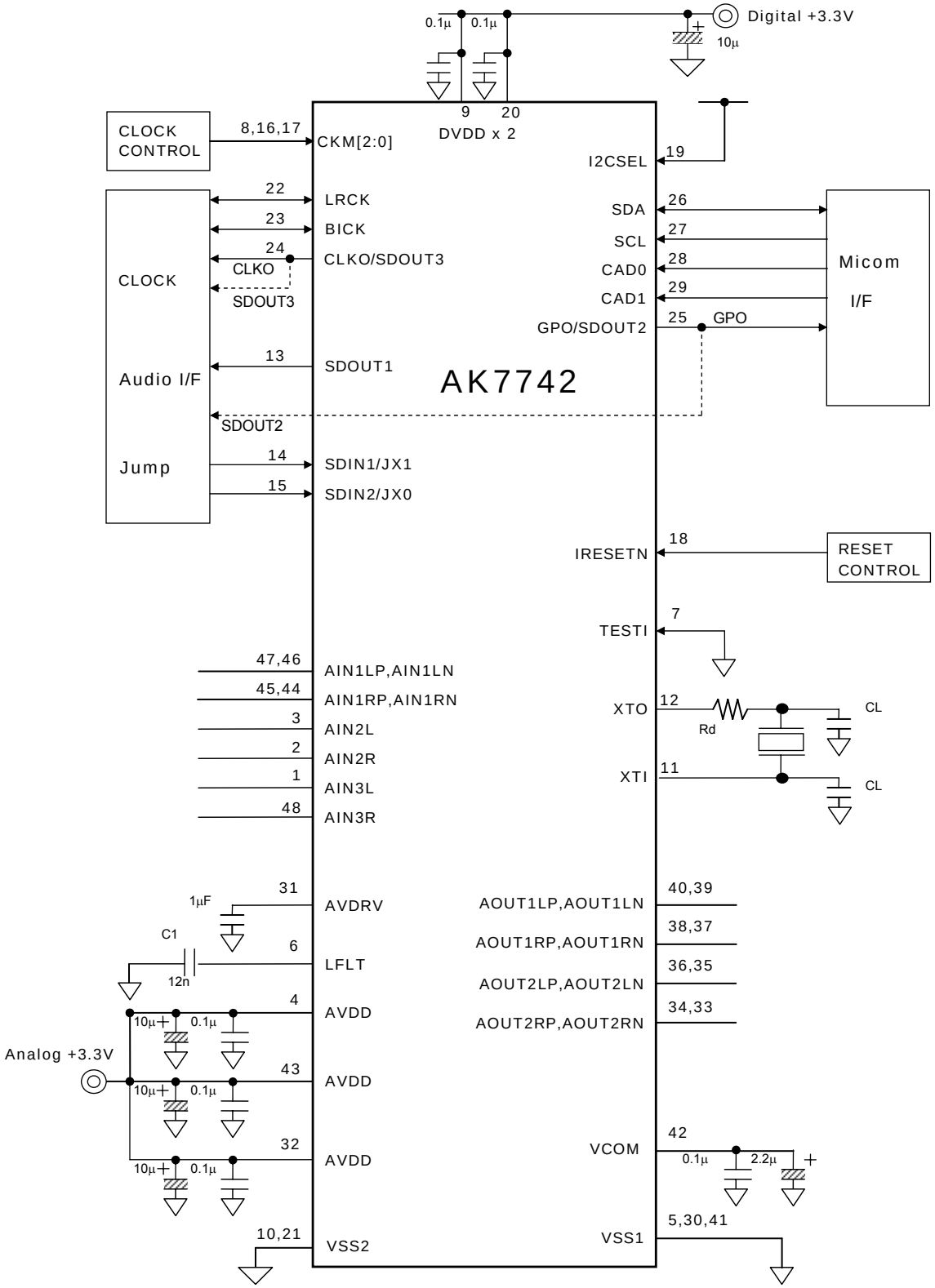


Figure 41. DAC Soft Mute Control

SYSTEM DESIGN

Figure 42 shows the system connection diagram. The evaluation board (AKD7742) demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



The Rd value is dependent on X'tal oscillator.

Figure 42. Typical connection

(2) Peripheral Circuits

1) Ground and Power Supply

To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK7742. System analog power is supplied to AVDD. VSS1 and VSS2 must be connected to the same ground plane. Power supply should be wired separately and connected as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be connected at positions as close as possible to the AK7742.

2) Reference Voltage

The AVDD voltage controls analog signal range. VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor attached between the VCOM pin and VSS1 eliminates the effects of high frequency noise. Especially a ceramic capacitor should be connected as close as possible to the pin.

Do not draw load current from the VCOM pin. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the AK7742.

3) Analog Input

Analog input signals are applied to the modulator through the input pin of each channel. Input voltage is ±FS=±(AVDD)x2.0/3.3 for differential pin and FS=(AVDD)x2.0/3.3 for single-end pin. When AVDD = 3.3V, the differential input range is ±2.00Vpp (typ) and for single-end is 2.00Vpp (typ). The output code format is given in terms of 2's complements.

The AK7742 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK7742 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

The analog source voltage to the AK7742 is +3.3V typical. Voltage of AVDD + 0.3V or more, voltage of VSS1 - 0.3V or less, and current of 10mA or more must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ±15V, the analog input pins must be protected from signals with the absolute maximum rating or more.

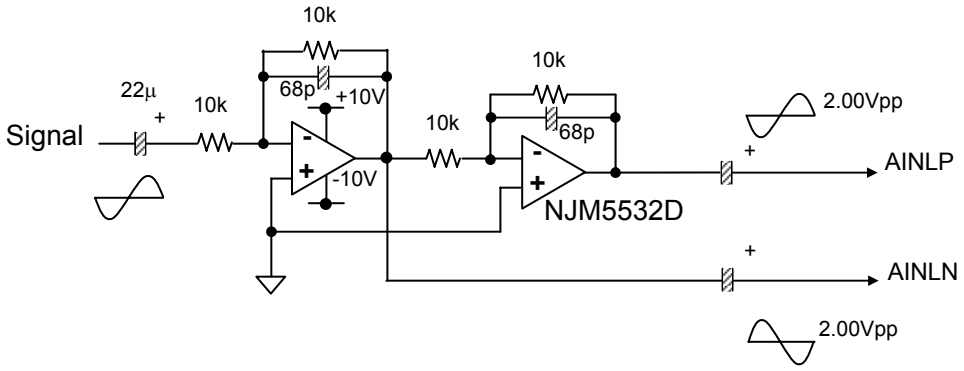


Figure 43. Input Buffer Circuit (differential)

4) Analog Output

The analog output is full differential. The output range is ±1.83Vpp (typ.) centered on VCOM voltage of AVDD/2(typ). The input code format is in 2's complement. Positive full-scale output corresponds to 7FFFFFh(@24bit) input code, Negative full scale is 800000h(@24bit) and VCOM voltage ideally is 000000h(@24bit)
The differential output has AVDD/2 + few mV DC offset. A capacitor to cut DC component should be connected. Figure 44 is an example of output buffer circuit.

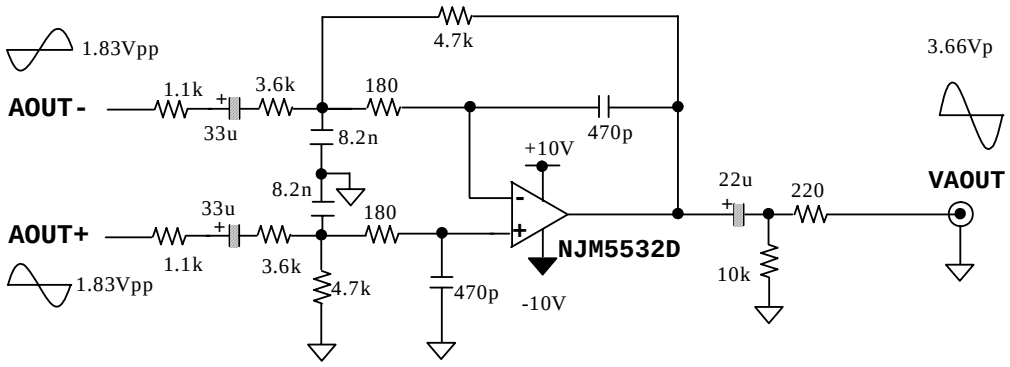


Figure 44. Output buffer circuit

1.1kΩ resisters should be connected as near as possible to the pin.

5) Cristal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown in Table 9.

CKM Mode	Equivalent Circuit Parameter		XTI, XTO pin external (CL)
	R1 (max)	C0 (max)	
0	70Ω	5pF	22pF

Table 9. Cristal Oscillator

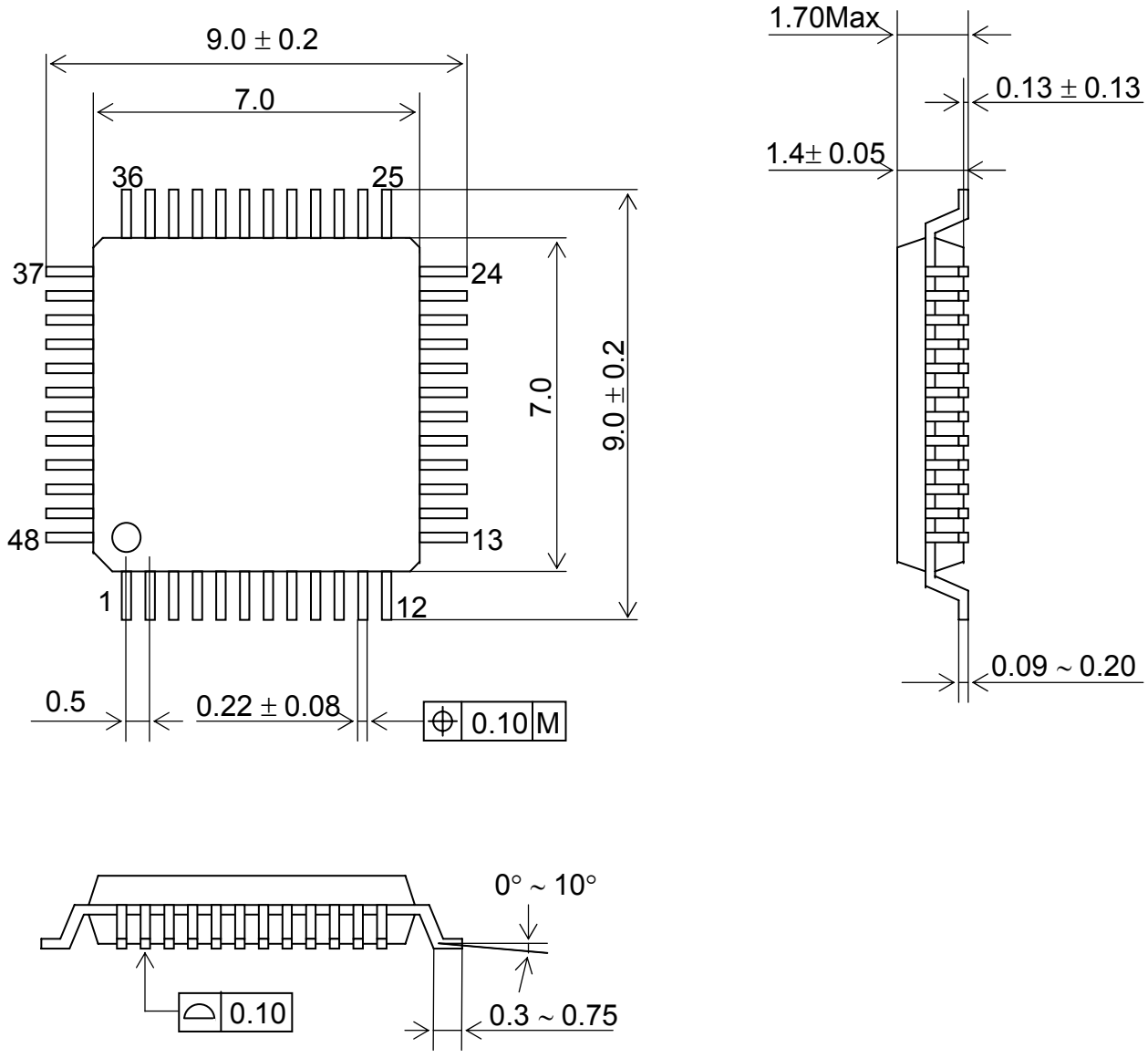
6) LFLT Pin External

The LFLT pin should be connected a capacitor with the following specification.

C1
12 nF ± 30%

PACKAGE (AK7742EQ)

48pin LQFP (Unit: mm)

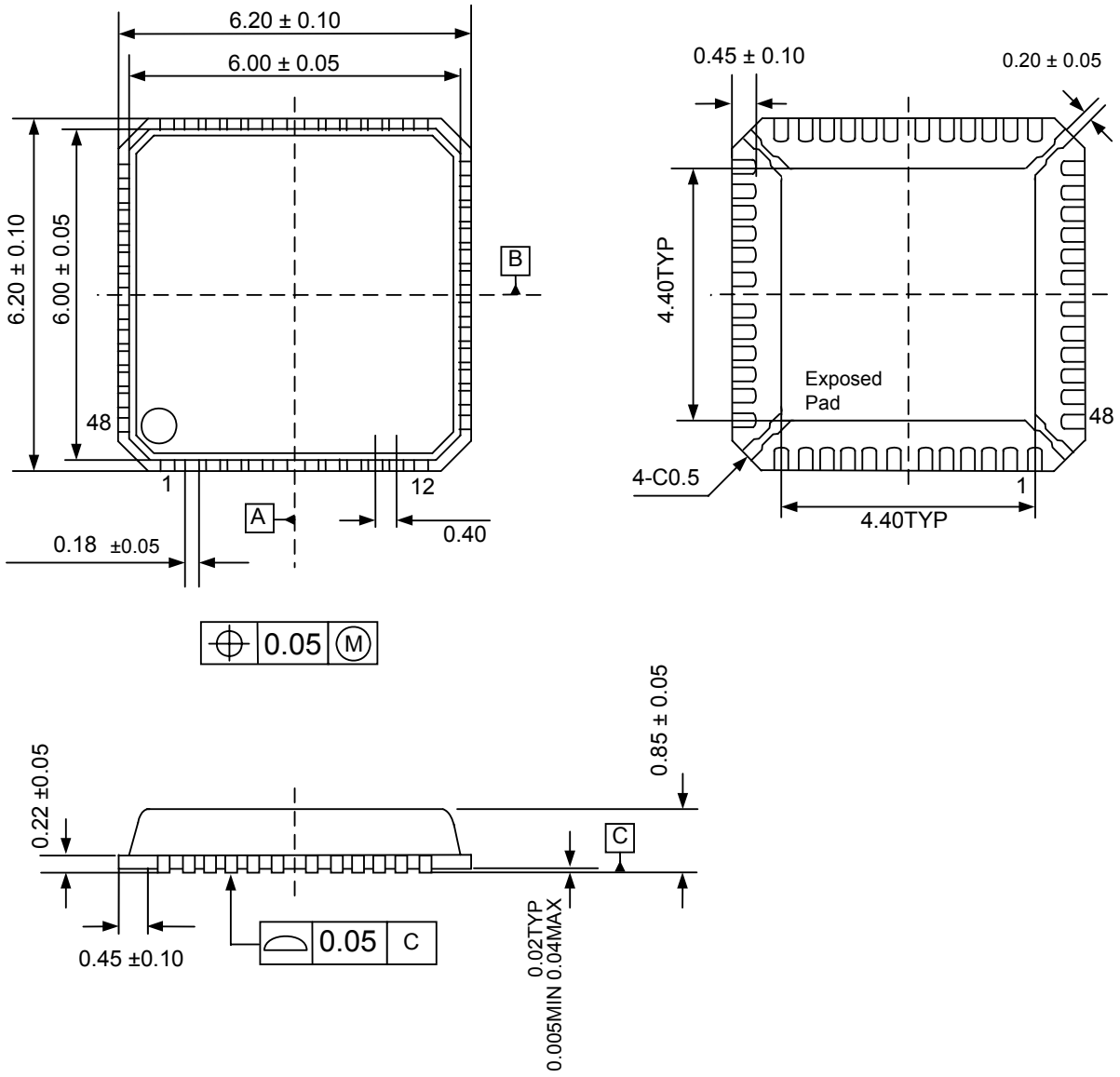


■ Materials and Lead Specification

Package:	Epoxy
Lead frame:	Copper
Lead-finish:	Soldering (Pb free) plate

PACKAGE (AK7742EN)

48pin QFN (Unit: mm)

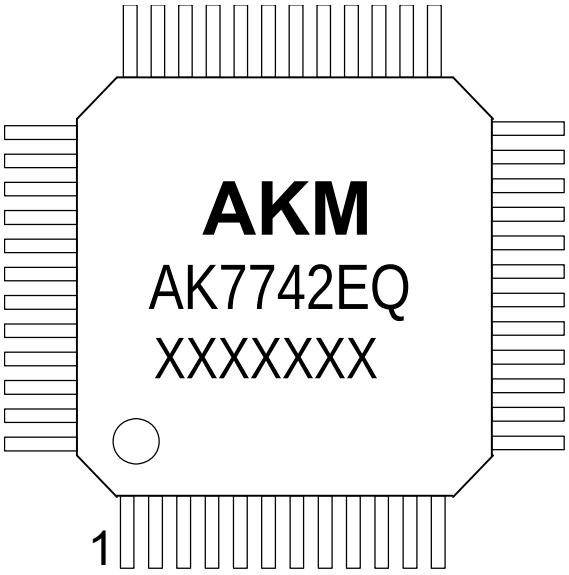


Note: The exposed pad must be open or connected to the ground.

■ Materials and Lead Specification

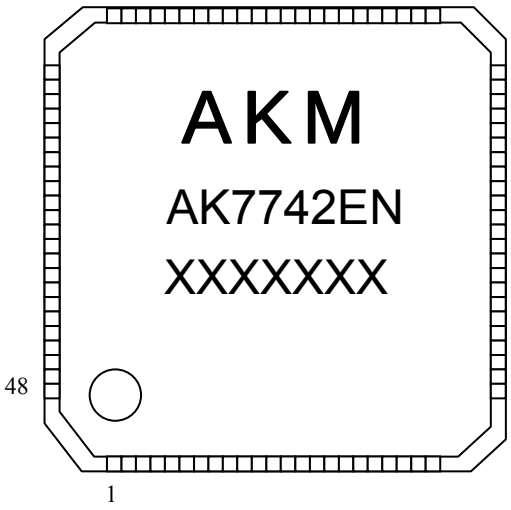
Package:	Epoxy
Lead frame:	Copper
Lead-finish:	Soldering (Pb free) plate

MARKING (AK7742EQ)



XXXXXXX: Date code identifier (7 digits)

MARKING (AK7742EN)



XXXXXXX: Date code identifier (7 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/11/07	00	First Edition		

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