



CYPRESS

CY7C167A

## 16K x 1 Static RAM

### Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 15 ns
- Low active power
  - 495 mW
- Low standby power
  - 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- $V_{IH}$  of 2.2V

### Functional Description

The CY7C167A is a high-performance CMOS static RAM organized as 16,384 words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ) and three-state drivers. The CY7C167A has an automatic power-down feature, reducing the power consumption by 67% when deselected.

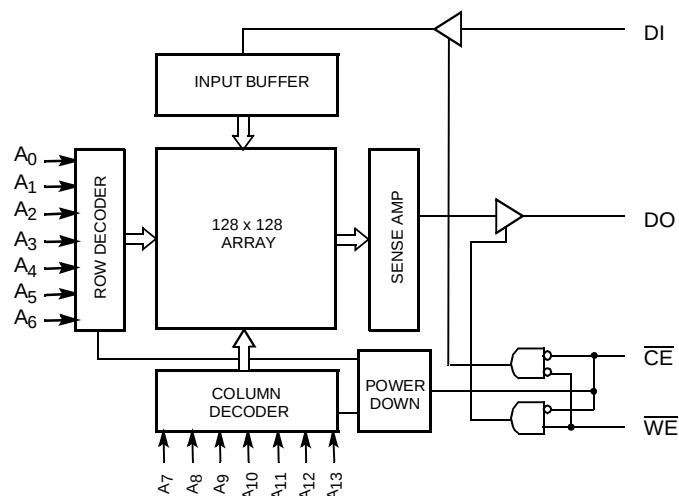
Writing to the device is accomplished when the Chip Select ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking the Chip Enable ( $\overline{CE}$ ) LOW, while ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the data output (DO) pin.

The output pin remains in a high-impedance state when Chip Enable is HIGH, or Write Enable ( $\overline{WE}$ ) is LOW.

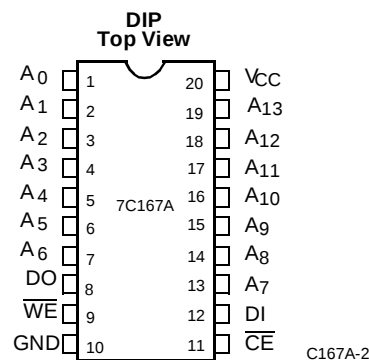
A die coat is used to insure alpha immunity.

### Logic Block Diagram



C167A-1

### Pin Configuration



C167A-2

### Selection Guide

|                                | 7C167A-15 | 7C167A-20 | 7C167A-25 | 7C167A-35 | 7C167A-45 |
|--------------------------------|-----------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns)       | 15        | 20        | 25        | 35        | 45        |
| Maximum Operating Current (mA) | 90        | 90        | 90        | 90        | 90        |



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential  
(Pin 20 to Pin 10) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature <sup>[1]</sup> | V <sub>CC</sub> |
|------------|------------------------------------|-----------------|
| Commercial | 0°C to +70°C                       | 5V ± 10%        |

## Electrical Characteristics Over the Operating Range

| Parameter       | Description                                                 | Test Conditions                                                  | 7C167A-15 |                 | 7C167A-20 |                 | 7C167A-25 |                 | Unit |
|-----------------|-------------------------------------------------------------|------------------------------------------------------------------|-----------|-----------------|-----------|-----------------|-----------|-----------------|------|
|                 |                                                             |                                                                  | Min.      | Max.            | Min.      | Max.            | Min.      | Max.            |      |
| V <sub>OH</sub> | Output High Voltage                                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                | 2.4       |                 | 2.4       |                 | 2.4       |                 | V    |
| V <sub>OL</sub> | Output Low Voltage                                          | V <sub>CC</sub> = Min.,<br>I <sub>OL</sub> = 12.0 mA, 8.0 mA Mil |           | 0.4             |           | 0.4             |           | 0.4             | V    |
| V <sub>IH</sub> | Input High Voltage                                          |                                                                  | 2.2       | V <sub>CC</sub> | 2.2       | V <sub>CC</sub> | 2.2       | V <sub>CC</sub> | V    |
| V <sub>IL</sub> | Input Low Voltage <sup>[2]</sup>                            |                                                                  | -0.5      | 0.8             | -0.5      | 0.8             | -0.5      | 0.8             | V    |
| I <sub>IX</sub> | Input Load Current                                          | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                           | -10       | +10             | -10       | +10             | -10       | +10             | μA   |
| I <sub>OZ</sub> | Output Leakage Current                                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled        | -10       | +10             | -10       | +10             | -10       | +10             | μA   |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[3]</sup>                 | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                   |           | -350            |           | -350            |           | -350            | mA   |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current                    | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA                  |           | 90              |           | 90              |           | 90              | mA   |
| I <sub>SB</sub> | Automatic $\overline{CE}$ Power-Down Current <sup>[4]</sup> | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$               |           | 40              |           | 40              |           | 20              | mA   |

| Parameter       | Description                                                 | Test Conditions                                                  | 7C167A-35 |                 | 7C167A-45 |                 | Unit |
|-----------------|-------------------------------------------------------------|------------------------------------------------------------------|-----------|-----------------|-----------|-----------------|------|
|                 |                                                             |                                                                  | Min.      | Max.            | Min.      | Max.            |      |
| V <sub>OH</sub> | Output High Voltage                                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                | 2.4       |                 | 2.4       |                 | V    |
| V <sub>OL</sub> | Output Low Voltage                                          | V <sub>CC</sub> = Min.,<br>I <sub>OL</sub> = 12.0 mA, 8.0 mA Mil |           | 0.4             |           | 0.4             | V    |
| V <sub>IH</sub> | Input High Voltage                                          |                                                                  | 2.2       | V <sub>CC</sub> | 2.2       | V <sub>CC</sub> | V    |
| V <sub>IL</sub> | Input Low Voltage <sup>[2]</sup>                            |                                                                  | -0.5      | 0.8             | -0.5      | 0.8             | V    |
| I <sub>IX</sub> | Input Load Current                                          | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                           | -10       | +10             | -10       | +10             | μA   |
| I <sub>OZ</sub> | Output Leakage Current                                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled        | -10       | +10             | -10       | +10             | μA   |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[3]</sup>                 | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                   |           | -350            |           | -350            | mA   |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current                    | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA                  |           | 90              |           | 90              | mA   |
| I <sub>SB</sub> | Automatic $\overline{CE}$ Power-Down Current <sup>[4]</sup> | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$               |           | 20              |           | 20              | mA   |

### Notes:

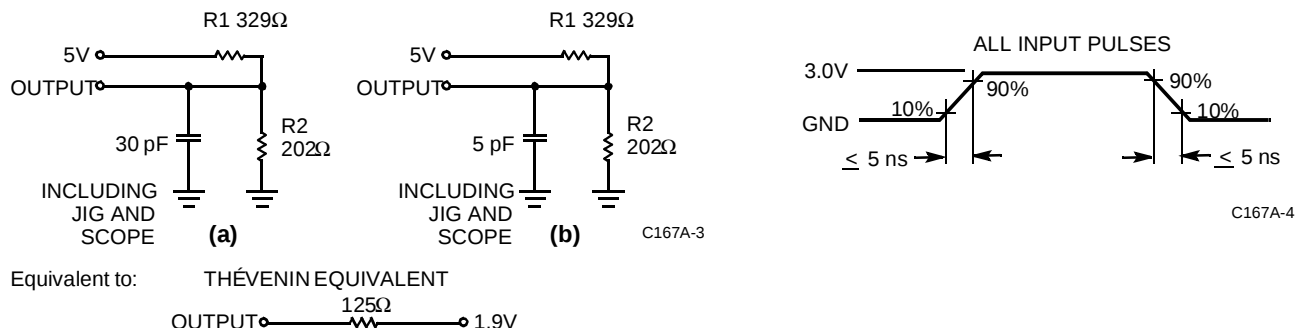
1. T<sub>A</sub> is the case temperature.
2. V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.
3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.



## Capacitance<sup>[5]</sup>

| Parameter        | Description             | Test Conditions                                             | Max. | Unit |
|------------------|-------------------------|-------------------------------------------------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance       | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance      |                                                             | 10   | pF   |
| C <sub>CE</sub>  | Chip Enable Capacitance |                                                             | 6    | pF   |

## AC Test Loads and Waveforms



## Switching Characteristics Over the Operating Range<sup>[6]</sup>

| Parameter                  | Description                                      | 7C167A-15 |      | 7C167A-20 |      | 7C167A-25 |      | 7C167A-35 |      | 7C167A-45 |      | Unit |
|----------------------------|--------------------------------------------------|-----------|------|-----------|------|-----------|------|-----------|------|-----------|------|------|
|                            |                                                  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |      |
| READ CYCLE                 |                                                  |           |      |           |      |           |      |           |      |           |      |      |
| t <sub>RC</sub>            | Read Cycle Time                                  | 15        |      | 20        |      | 25        |      | 30        |      |           |      | ns   |
| t <sub>AA</sub>            | Address to Data Valid                            |           | 15   |           | 20   |           | 25   |           | 30   |           |      | ns   |
| t <sub>OHA</sub>           | Data Hold from Address Change                    | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns   |
| t <sub>ACE</sub>           | $\overline{CE}$ LOW to Data Valid                |           | 15   |           | 20   |           | 25   |           | 35   |           | 45   | ns   |
| t <sub>LZCE</sub>          | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>      | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns   |
| t <sub>HZCE</sub>          | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |           | 8    |           | 8    |           | 10   |           | 15   |           | 15   | ns   |
| t <sub>PU</sub>            | $\overline{CE}$ LOW to Power-Up                  | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>PD</sub>            | $\overline{CE}$ HIGH to Power-Down               |           | 15   |           | 20   |           | 20   |           | 20   |           | 25   | ns   |
| WRITE CYCLE <sup>[9]</sup> |                                                  |           |      |           |      |           |      |           |      |           |      |      |
| t <sub>WC</sub>            | Write Cycle Time                                 | 15        |      | 20        |      | 20        |      | 25        |      | 40        |      | ns   |
| t <sub>SCE</sub>           | $\overline{CE}$ LOW to Write End                 | 12        |      | 15        |      | 20        |      | 25        |      | 30        |      | ns   |
| t <sub>AW</sub>            | Address Set-Up to Write End                      | 12        |      | 15        |      | 20        |      | 25        |      | 30        |      | ns   |
| t <sub>HA</sub>            | Address Hold from Write End                      | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>SA</sub>            | Address Set-Up to Write Start                    | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>PWE</sub>           | $\overline{WE}$ Pulse Width                      | 12        |      | 15        |      | 15        |      | 20        |      | 20        |      | ns   |
| t <sub>SD</sub>            | Data Set-Up to Write End                         | 10        |      | 10        |      | 10        |      | 15        |      | 15        |      | ns   |
| t <sub>HD</sub>            | Data Hold from Write End                         | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>HZWE</sub>          | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  |           | 7    |           | 7    |           | 7    |           | 10   |           | 15   | ns   |
| t <sub>LZWE</sub>          | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup>     | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns   |

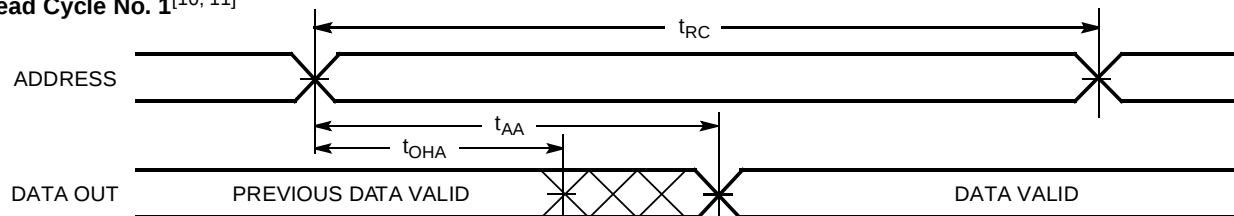
### Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



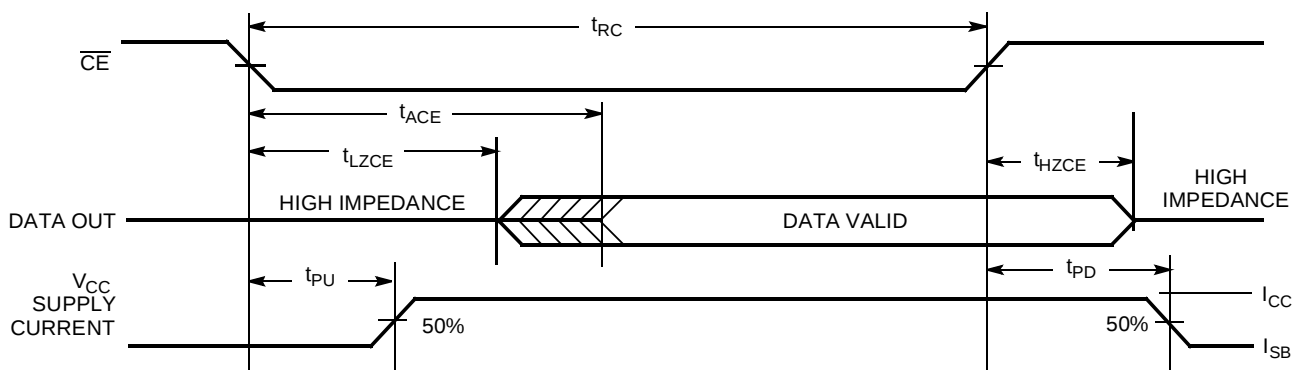
## Switching Waveforms

Read Cycle No. 1<sup>[10, 11]</sup>



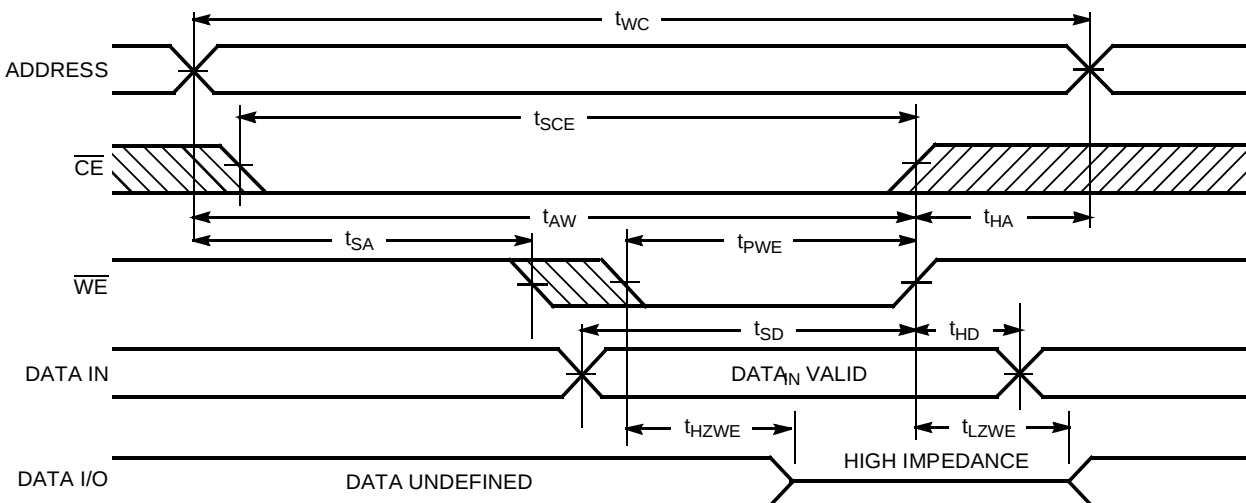
C167A-5

Read Cycle No. 2<sup>[10, 12]</sup>



C167A-6

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[9]</sup>



C167A-7

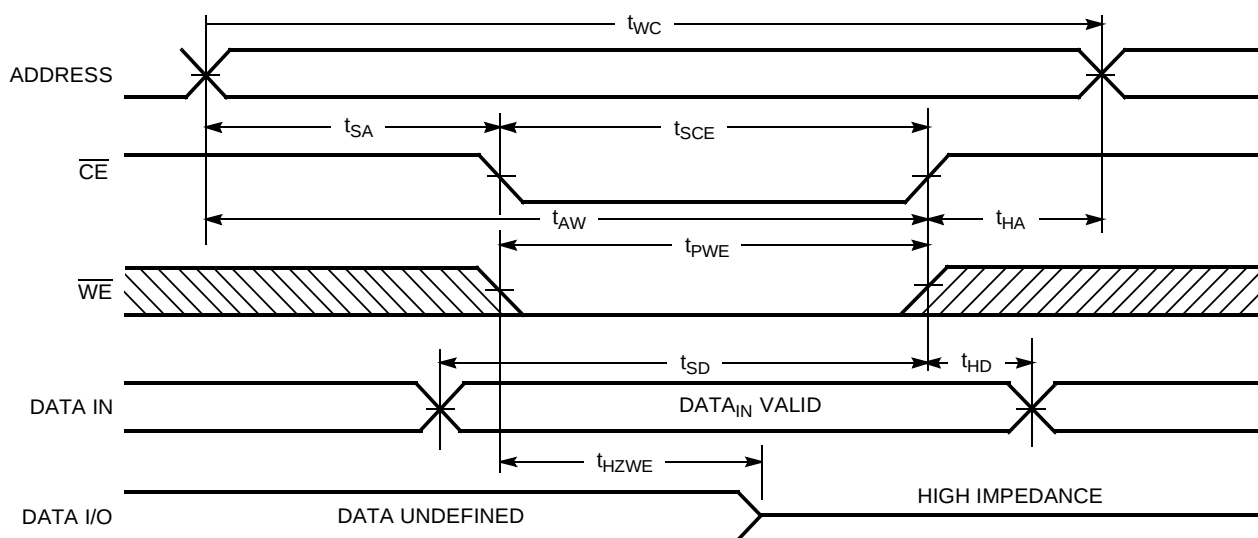
### Notes:

10.  $\overline{WE}$  is high for read cycle.
11. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.



# Switching Waveforms (continued)

## Write Cycle No. 2 ( $\overline{\text{CE}}$ Controlled)<sup>[9, 13]</sup>



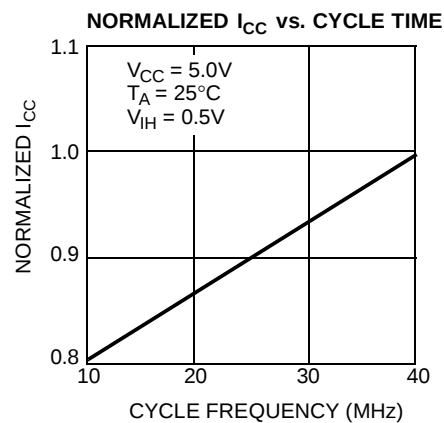
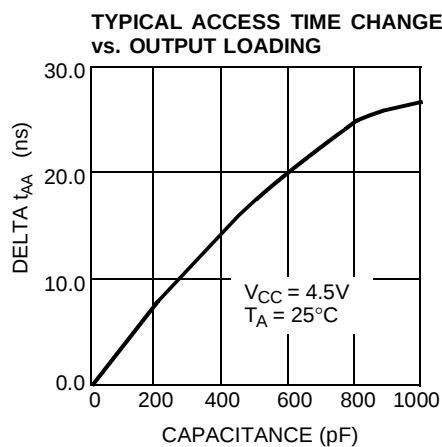
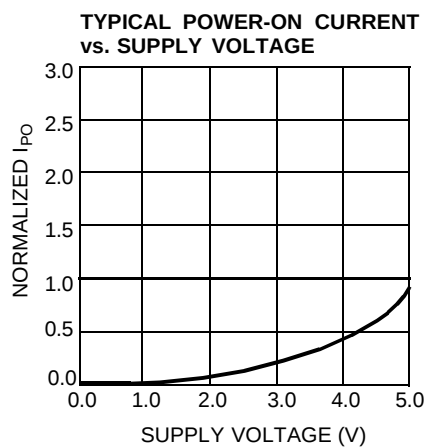
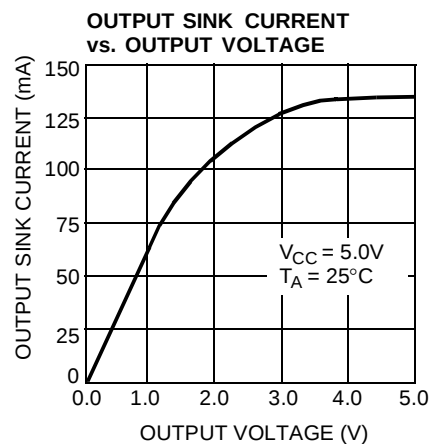
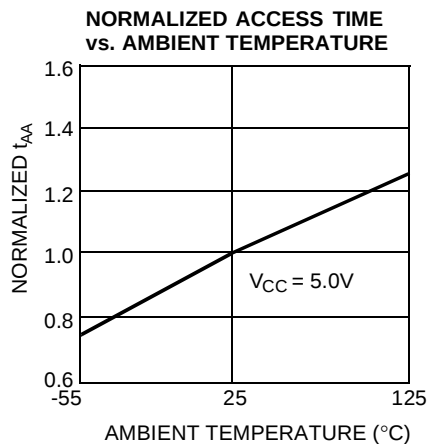
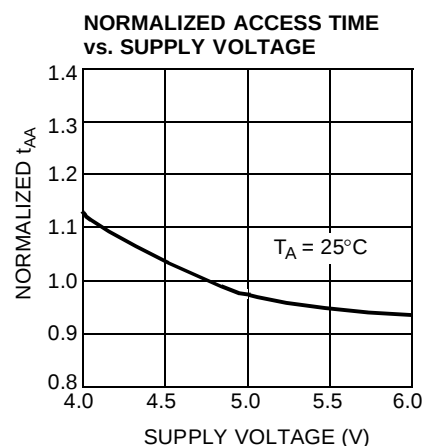
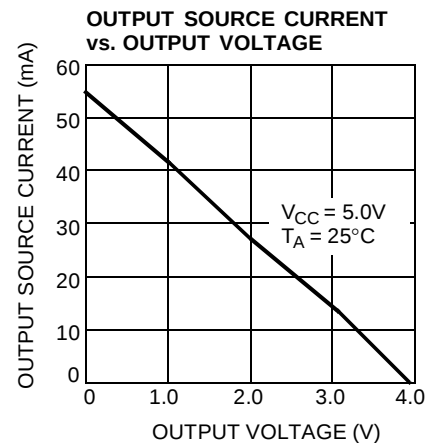
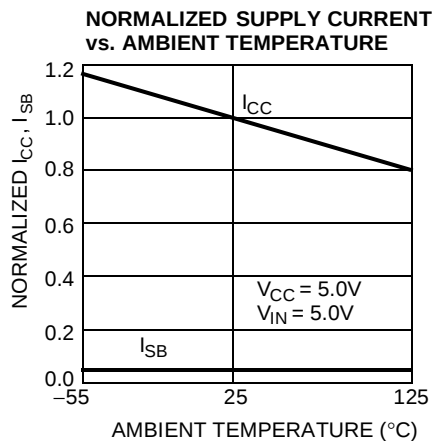
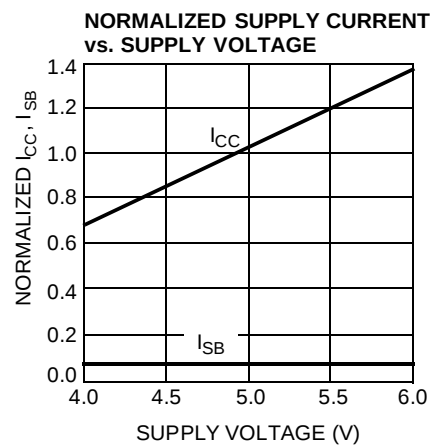
C167A-8

### Note:

13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.



## Typical DC and AC Characteristics





## Ordering Information

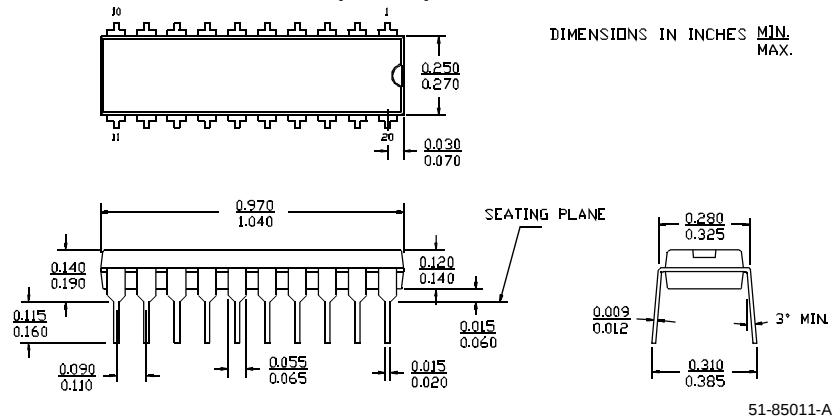
| Speed (ns) | I <sub>CC</sub> (mA) | Ordering Code | Package Name | Package Type                 | Operating Range |
|------------|----------------------|---------------|--------------|------------------------------|-----------------|
| 15         | 80                   | CY7C167A-15PC | P5           | 20-Lead (300-Mil) Molded DIP | Commercial      |
|            |                      | CY7C167A-15VC | V5           | 20-Lead Molded SOJ           |                 |
| 20         | 80                   | CY7C167A-20PC | P5           | 20-Lead (300-Mil) Molded DIP | Commercial      |
|            |                      | CY7C167A-20VC | V5           | 20-Lead Molded SOJ           |                 |
| 25         | 60                   | CY7C167A-25PC | P5           | 20-Lead (300-Mil) Molded DIP | Commercial      |
|            |                      | CY7C167A-25VC | V5           | 20-Lead Molded SOJ           |                 |
| 35         | 60                   | CY7C167A-35PC | P5           | 20-Lead (300-Mil) Molded DIP | Commercial      |
|            |                      | CY7C167A-35VC | V5           | 20-Lead Molded SOJ           |                 |
| 45         | 50                   | CY7C167A-45PC | P5           | 20-Lead (300-Mil) Molded DIP | Commercial      |
|            |                      | CY7C167A-45VC | V5           | 20-Lead Molded SOJ           |                 |

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## Package Diagrams

### 20-Lead (300-Mil) Molded DIP P5



### 20-Lead (300-Mil) Molded SOJ V5

