STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME Main Power Supply For TFT-LCD Display Module

TYPE **BD8156EFV**

FEATURES Built-in 4-channel outputs for TFT-LCD Display
Built-in Gate Shading

●ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	LIMITS	UNIT
Supply Voltage	Vcc PVCC	19	V
Vo1 Voltage	Vo1	19	V
Vo2 Voltage	Vo2	40	V
Junction Temperature	Tjmax	150	℃
Power Dissipation	Pd	4700*1	mW
Operating Temperature Range	Topr	-40～85	℃
Storage Temperature Range	Tstg	-55～150	℃

*1 Decreased in done 37.6mW/℃ for operating above Ta≧25℃,
mounted on 70×70×1.6mm 4 layer Glass-epoxy PCB.
(back foil 70.0mm×70.0mm)

●OPERATING CONDITIONS (Ta=-40℃～+85℃)

Parameter	Symbol	MIN	MAX	Unit
Supply Voltage	VCC,PVCC	6	18	V
Vo1 Voltage	Vo1	8	18	V
Vo2 Voltage	Vo2	-	39	V
SW Current	SW1,SW2	-	2	A

★This product is not designed for protection against radioactive rays.
★The product described in this specification is a strategic product(and/or Service) subject to COCOM regulations.
It should not be exported without Authorization from the appropriate government.

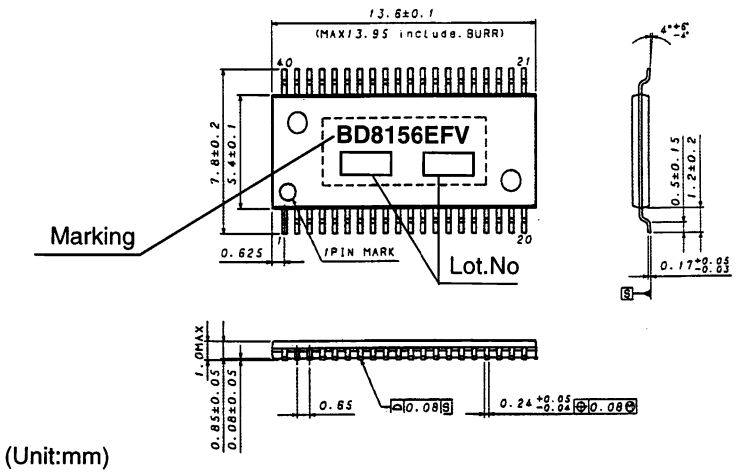
Status of this document
The English version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

●ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25℃ Vcc=15V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
〔Error Amplifier Block FB1,FB2〕						
FB Input Bias Current 1,2	IFB1,2	-	0.4	1.5	μA	VFB=0.5V
Feed Back Voltage 1,2	VFB1,2	1.230	1.250	1.270	V	Buffer
〔SW Block SW1 SW2〕						
High Side ON Resistance	Ron h	-	200	300	mΩ	Io=1A※
Low Side ON Resistance	Ron l	-	2	3	Ω	Io=20mA※
Current Limit	Insw	2	-	-	A	※
Maximum Duty	DMAX	-	97	-	%	
〔Error Amplifier Block FB3, FB4〕						
Input Bias Current 3,4	IFB3,4	-	0.1	0.5	μA	
Feed Back Voltage 3,4	VFB3,4	1.18	1.25	1.32	V	
〔SW Block C1L,C2L,C3〕						
Nch ON Resistance	RON_NC	-	1	2	Ω	Io=20mA ※
Pch ON Resistance	RON_PC	-	2	4	Ω	Io=20mA ※
〔Input Block IG〕						
IGH Voltage	IGH	1.9	2.9	5	V	
IGL Voltage	LGL	-	0	0.9	V	
〔Reference Block VREF〕						
VREF Voltage	VREF	2.75	2.90	3.05	V	
〔Regulator Block VREG 〕						
VREG Voltage	VREG	4.5	5.0	5.5	V	
〔Oscillation Block〕						
Frequency	Fosc	400	500	600	KHz	
〔Short Protection Block SCP〕						
SCP Source Current	Iscp	3	5	7	uA	
Threshold Voltage	Vth_scp	0.48	0.6	0.72	V	
〔VCOM Block VCOM〕						
Offset Voltage	Voso	-10	0	10	mV	
Drive Current	Ioo	30	50	-	mA	
〔Under Voltage Lock Out Block〕						
Detect Voltage	VUVLO	4.8	5.1	5.4	V	
〔Device〕						
Average Supply Current	Icc	3.0	4.5	6.0	mA	Standby Current

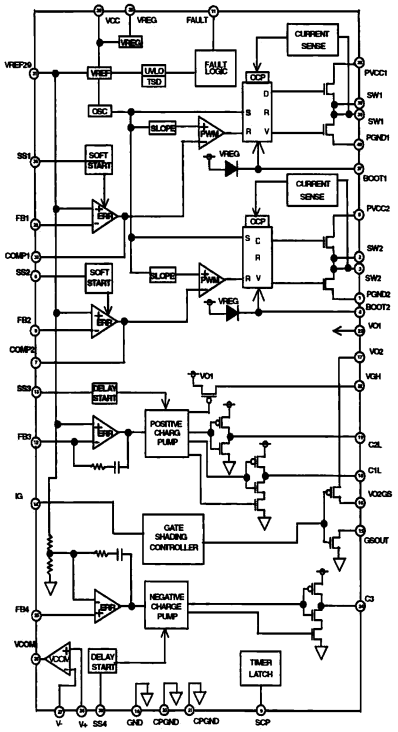
※Design Guarantee (Outgoing inspection is not done all products.)

●PHYSICAL DIMENSION・MARKING (HTSSOP-B40)



(Unit:mm)

●BLOCK DIAGRAM



*Please refer to Technical note concerning application circuit, and etc.

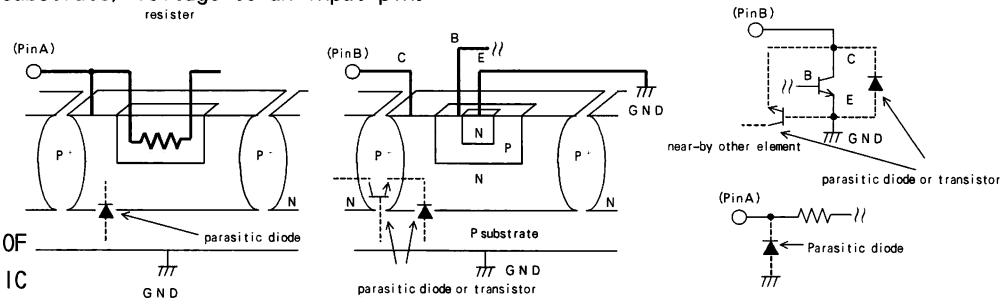
●PIN No. & FUNCTION TABLE

PIN NO.	Pin Name	Function	PIN NO.	Pin Name	Function
1	PGND2	Ground	21	CPGND	Ground
2	SW2	Power Switch Output 2	22	VGH	Positive Charge Pump Diode Connection Terminal
3	SW2	Power Switch Output 2	23	Vo1	Power Supply Input
4	BOOT2	Boot strap Terminal 2	24	C3	Charge Pump Clock Output 3
5	PVCC2	Power Supply Input	25	FB4	Feed Back Input 3
6	SS2	Soft Start Current Output 2	26	VCOM	VCOM Output
7	COMP2	Error Amp Output 2	27	V-	VCOM -Input
8	FB2	Feed Back Input 2	28	V+	VCOM +Input
9	SCP	Short Protection Current Output	29	VCC	Power Supply Input
10	GND	Ground	30	SS4	Delay Start Current Output 4
11	FAULT	Protect Detection Output	31	VREF29	Reference Voltage Output
12	FB3	Feed Back Input 3	32	FB1	Feed Back Input 1
13	SS3	Delay Start Current Output 3	33	COMP1	Error Amp Output 1
14	IG	Gate Shading Input	34	SS1	Soft Start Current Output 1
15	GSOUT	Gate Shading Sink Output	35	VREG	Boot strap Regulator Output
16	Vo2GS	Gate Shading Source Output	36	PVCC1	Power Supply Input
17	Vo2	Power Supply Input	37	BOOT1	Boot strap Terminal 1
18	C1L	Charge Pump Clock Output 1	38	SW1	Power Switch Output 1
19	C2L	Charge Pump Clock Output 2	39	SW1	Power Switch Output 1
20	CPGND	Ground	40	PGND1	Ground

●Operation Notes

1. Absolute maximum range
   This product are produced with strict quality control, but might be destroyed in using beyond absolute maximum ratings. Open IC destroyed a failure mode cannot be defined (like Short mode, or Open mode). Therefore physical security countermeasure, like fuse, is to be given when a specified mode to be beyond absolute maximum ratings is considered.
2. Ground potential
   GND terminal should be a lowest voltage potential every state.
   Please make sure all pins which is over ground even if include transient feature.
3. Setting of heat
   Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions..
4. Short Circuit between Terminal and Soldering
   Don' t short-circuit between Output pin and V_{DD} pin, Output pin and GND pin, or V_{DD} pin and GND pin. When soldering the IC on circuit board, please be unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.
5. Electromagnetic Field
   Mal-function may happen when the device is used in the strong electromagnetic field.
6. Ground wiring patterns
   When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.
7. This IC is a monolithic IC which has P+ isolation in the P substrate and between the various pins.
   A P-N junction is formed from this P layer and the N layer of each pin.
   For example, when a resistor and a transistor is connected to a pin.
   Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly, you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

SIMPLIFIED STRUCTURE OF BI-POLAR IC



8. Over current protection circuit
   The over-current protection circuits are built in at output, according to their respective current outputs and prevent the IC from being damaged when the load is short-circuited or over-current. But, these protection circuits are effective for preventing destruction by unexpected accident. When it' s in continuous protection circuit moving period don' t use please. And for ability, because this chip has minus characteristic, be careful for heat plan.
9. Built-in thermal circuit
   A temperature control circuit is built in the IC to prevent the damage due to overheat. Therefore, all the outputs are turned off when the thermal circuit works and are turned on when the temperature goes down to the specified level.
10. Testing on application boards
    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

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