

CMOS Analog Switches

FEATURES

- $\pm 15\text{-V}$ Input Range
- Low $r_{DS(on)}$: $30\ \Omega$
- Single Supply Operation
- Pin and Function Compatible with the JFET DG180 Family

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

DESCRIPTION

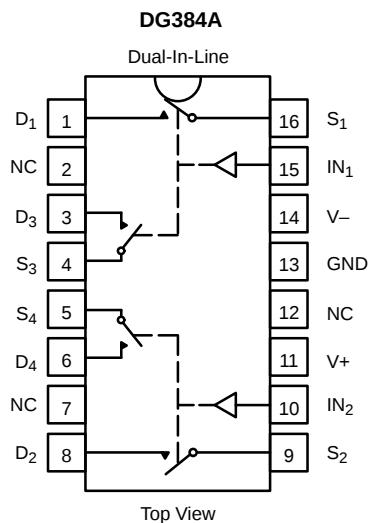
The DG384A and DG387A monolithic CMOS analog switches were designed for applications in instrumentation, communications, and process control. This series is suited for applications requiring fast switching and nearly flat on-resistance over the entire voltage range.

switches are ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation is allowed by connecting the V– rail to 0 V.

Designed on Vishay Siliconix' PLUS-40 CMOS process, these devices achieve low power consumption (3.5 mW typical) and excellent on/off switch performance. These

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS and quasi TTL logic compatible.

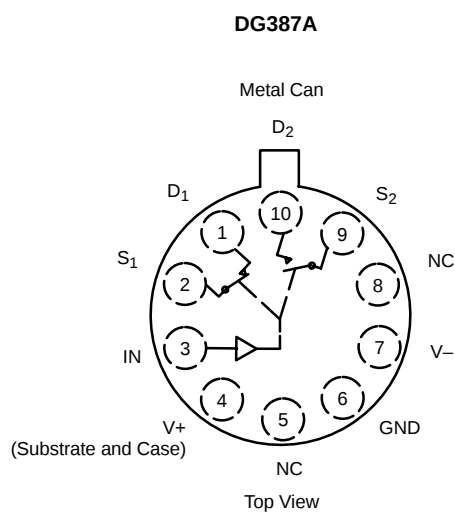
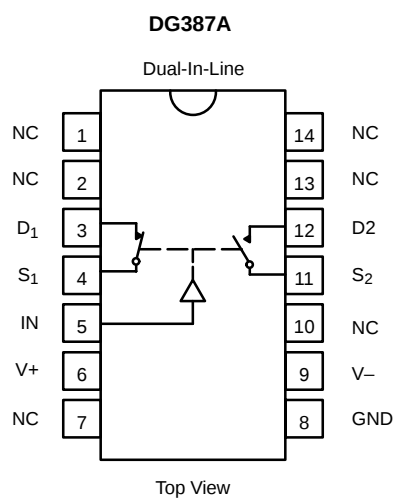
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic "0" $\leq 0.8\text{ V}$
Logic "1" $\geq 4\text{ V}$

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	SW_1	SW_2
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
DG384A		
0 to 70°C	16-Pin Plastic DIP	DG384ACJ
–55 to 125°C	16-Pin CerDIP	DG384AAK/883, 5962-9678801QEA
DG387A		
0 to 70°C	14-Pin Plastic DIP	DG387ACJ
–55 to 125°C	14-Pin CerDIP	DG387AAK/883
	10-Pin Metal Can	DG387AAA/883

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ 44 V

GND 25 V

Digital Inputs^a, V_S, V_D (V–) –2 V to (V+) +2V or
30 mA, whichever occurs first

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 30 mA

(Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature (AA, AK, Suffix) –65 to 150°C
(CJ Suffix) –65 to 125°C

Power Dissipation^b

14-Pin Plastic DIP^d 470 mW

14-Pin CerDIP^c 825 mW

10-Pin Metal Can^e 450 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 11 mW/°C above 75°C

d. Derate 6.5 mW/°C above 25°C

e. Derate 6 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

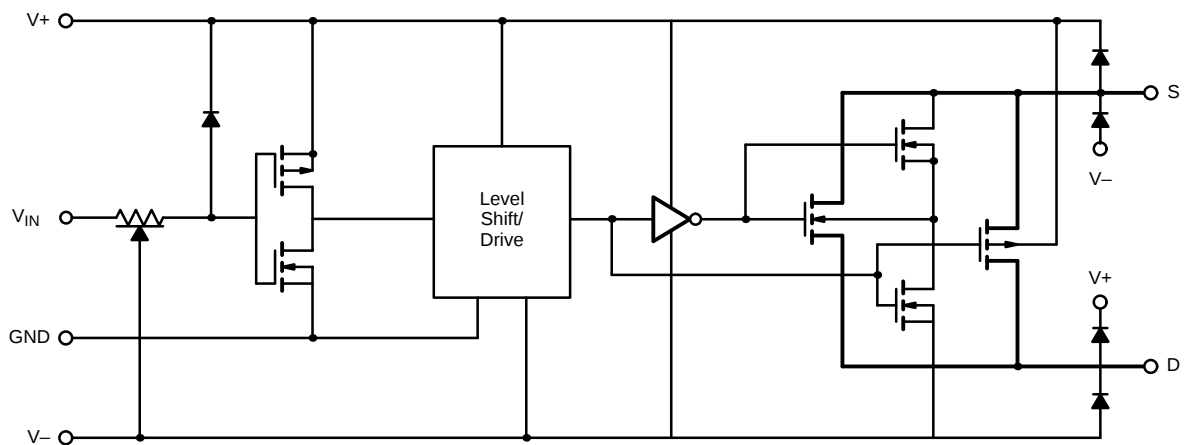


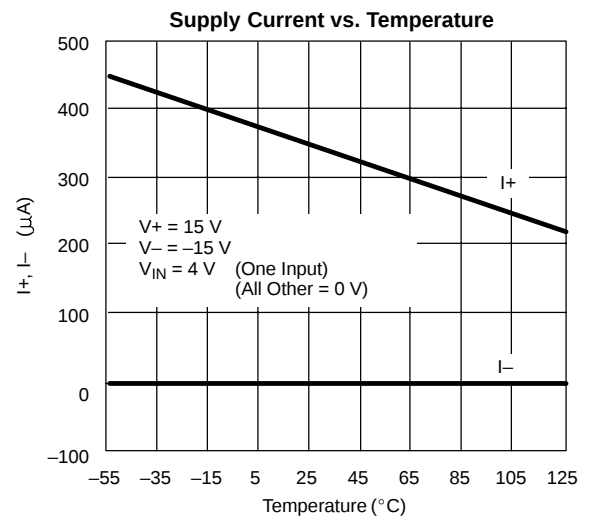
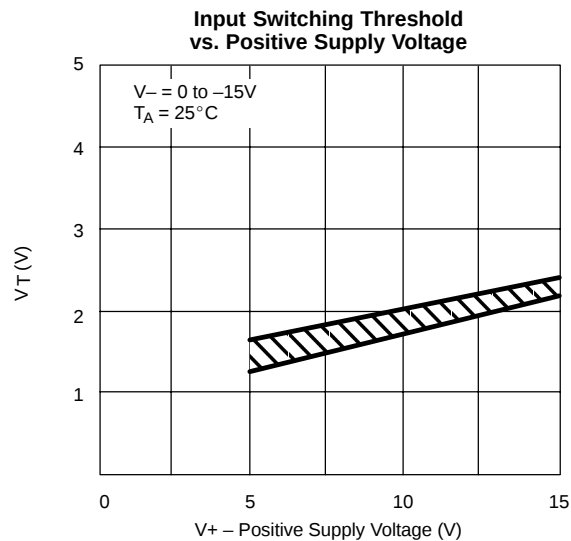
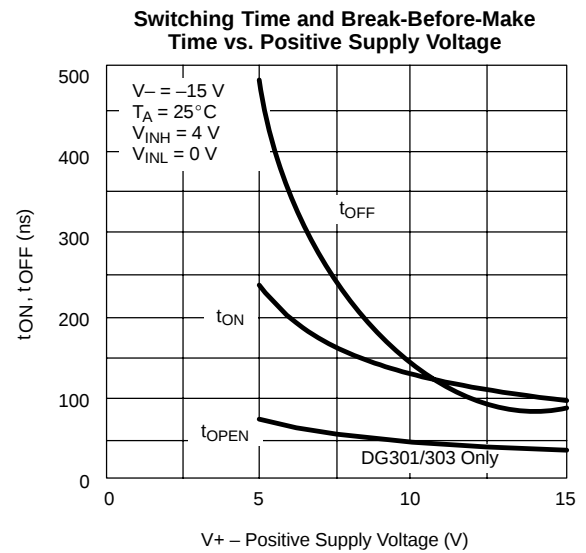
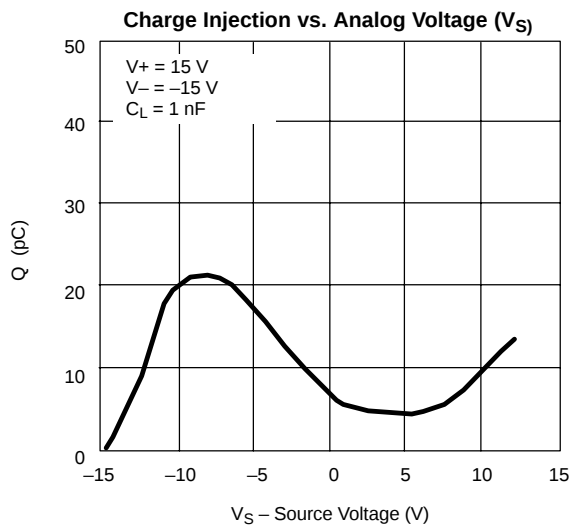
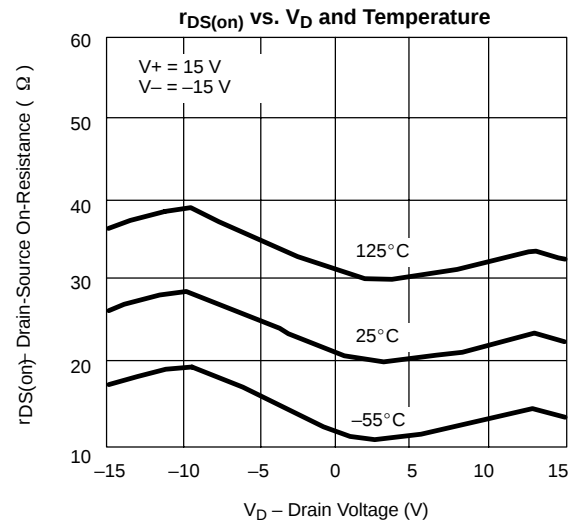
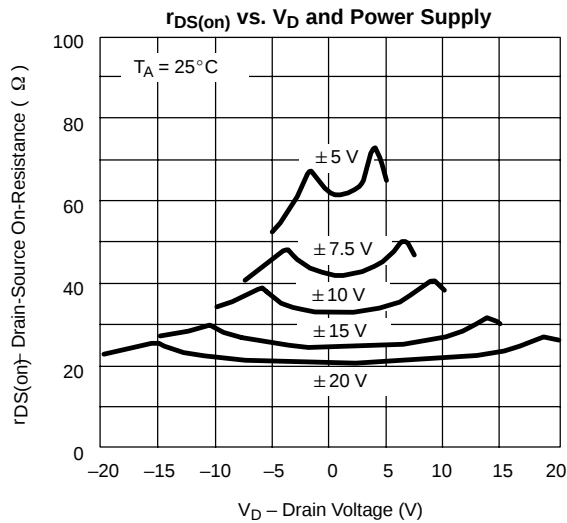
FIGURE 1.



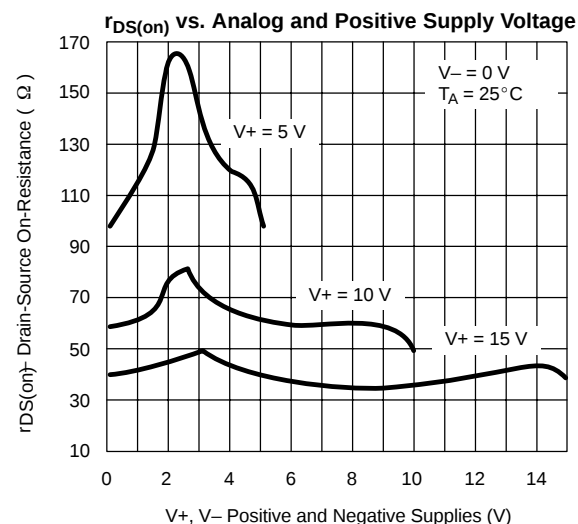
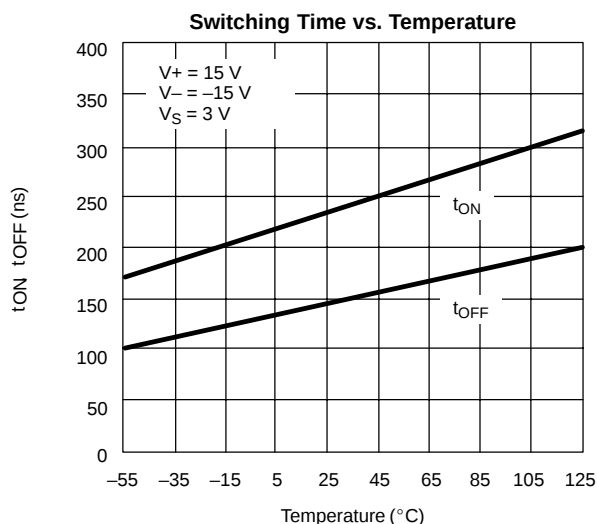
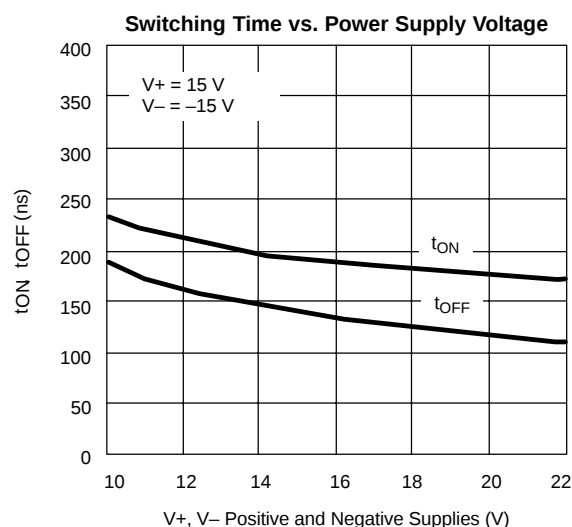
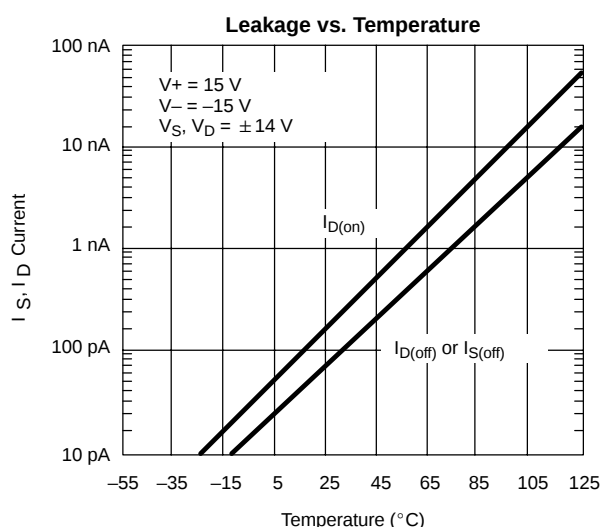
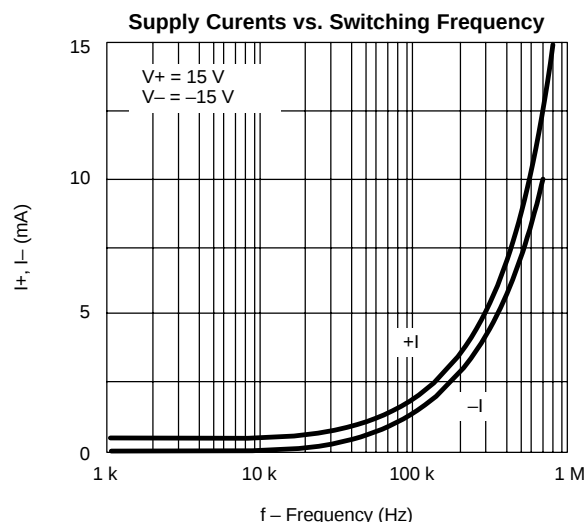
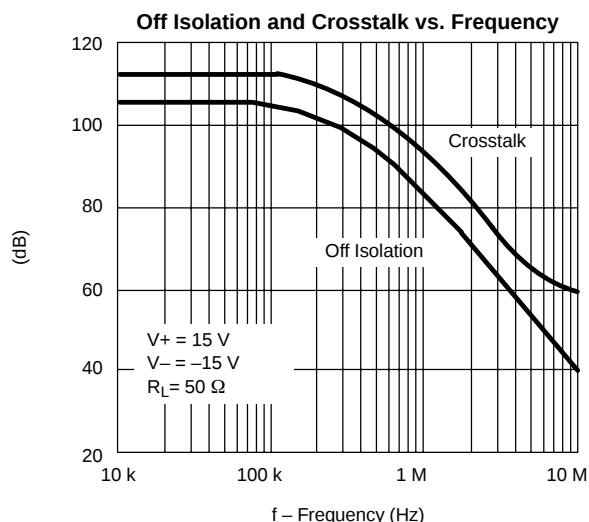
SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 15 V, V _– = –15 V V _{IN} = 0.8 V or 4 V ^f	Temp ^b	Typ ^c	A Suffix –55 to 125°C		C Suffix 0 to 70°C		Unit	
					Min ^d	Max ^d	Min ^d	Max ^d		
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}		Full		–15	15	–15	15	V	
Drain-Source On-Resistance	r _{DS(on)}	V _D = ± 10 V, I _S = –10 mA	Room Full	30		50 75		50 75	Ω	
Source Off Leakage Current	I _{S(off)}	V _S = ± 14 V, V _D = ∓ 14 V	Room Hot	± 0.1	–1 –100	1 100	–5 –100	5 100	nA	
Drain Off Leakage Current	I _{D(off)}	V _S = ± 14 V, V _D = ∓ 14 V	Room Hot	± 0.1	–1 –100	1 100	–5 –100	5 100		
Drain On Leakage Current	I _{D(on)}	V _D = V _S = ± 14 V	Room Hot	± 0.1	–11 –100	1 100	–5 –100	5 100		
Digital Control										
Input Current with Input Voltage High	I _{INH}	V _{IN} = 5 V	Room Full	–0.001	–1 –1		–1		μA	
		V _{IN} = 15 V	Room Full	0.001		1 1		1		
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0 V	Room Full	–0.001	–1 –1		–1			
Dynamic Characteristics										
Turn-On Time	t _{ON}	See Figure 2		Room	150		300		ns	
Turn-Off Time	t _{OFF}			Room	130		250			
Break-Before-Make Time	t _{OPEN}	See Figure 3		Room	50					
Charge Injection	Q	C _L = 0.01 μF, R _{gen} = 0 Ω V _{gen} = 0 V		Room	10				pC	
Source-Off Capacitance	C _{S(off)}	f = 1 MHz; V _S , V _D = 0 V		Room	14				pF	
Drain-Off Capacitance	C _{D(off)}			Room	14					
Channel-On Capacitance	C _{D(on)}			Room	40					
Input Capacitance	C _{IN}	f = 1 MHz	V _{IN} = 0 V	Room	6					
			V _{IN} = 15 V	Room	7					
Off-Isolation	OIRR	V _{IN} = 0 V, R _L = 1 kΩ V _S = 1 V _{rms} , f = 500 kHz		Room	62				dB	
Crosstalk (Channel-to-Channel)	X _{TALK}			Room	74					
Power Supplies										
Positive Supply Current	I ₊	V _{IN} = 4 V (One Input) (All Others = 0)		Room Full	0.23		0.5 1.0		1	mA
Negative Supply Current	I _–			Room Full	–0.001	–10 –100		–100		
Positive Supply Current	I ₊	V _{IN} = 0.8 V (All Inputs)		Room Full	0.001		10 100		100	μA
Negative Supply Current	I _–			Room Full	–0.001	–10 –100		–100		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TEST CIRCUITS

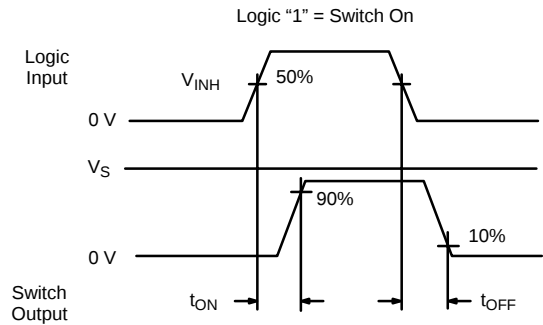
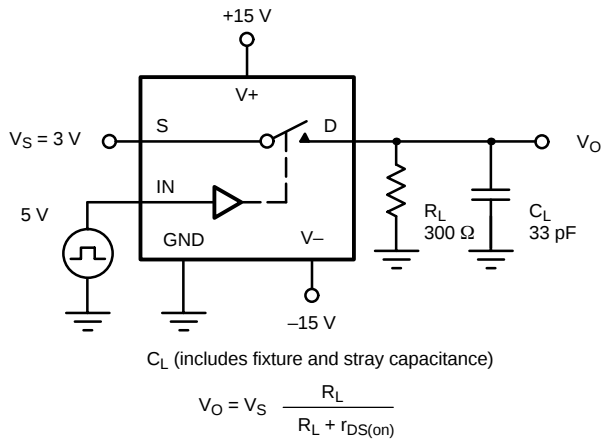


FIGURE 2. Switching Time

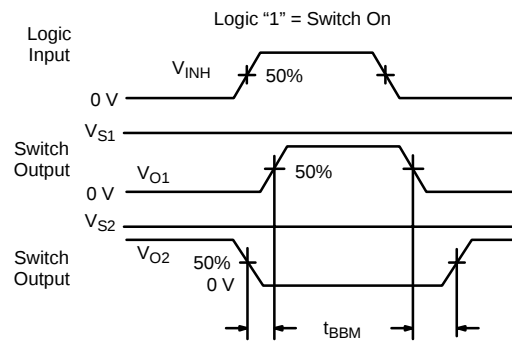
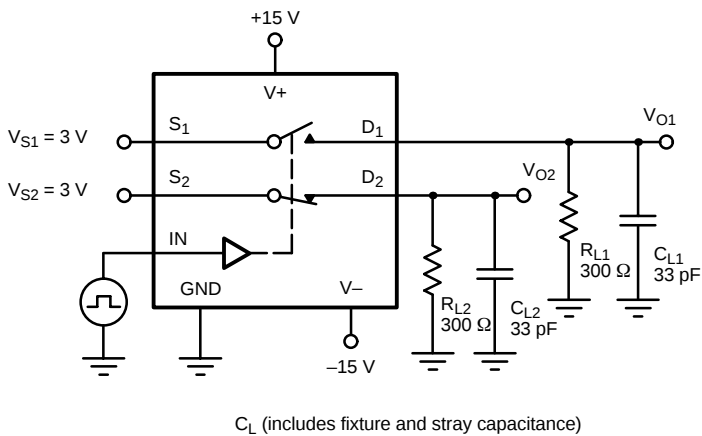


FIGURE 3. Break-Before-Make SPDT (DG387A)

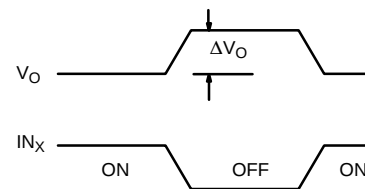
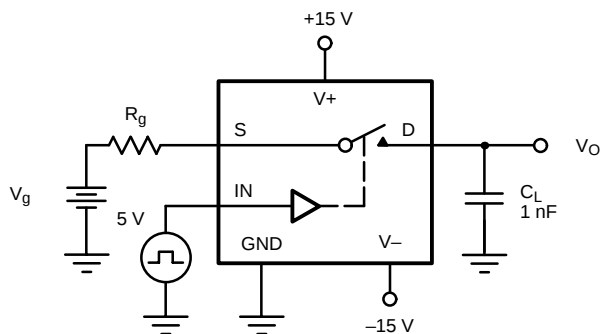


FIGURE 4. Charge Injection

APPLICATIONS

The DG384A and DG387A will switch positive analog signals while using a single positive supply. This allows their use in applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased $r_{DS(on)}$, 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied (see Typical Characteristics). The analog voltage should not go above or below the supply voltages which in single operation are $V+$ and 0 V.

In the integrator of Figure 4, R_D controls the discharge rate of the capacitor so that the pulsed or continuous current ratings are not exceeded. During reset SW_1 is closed and SW_2 is open. Opening SW_2 with SW_1 also open will hold the integrator output at its present value.

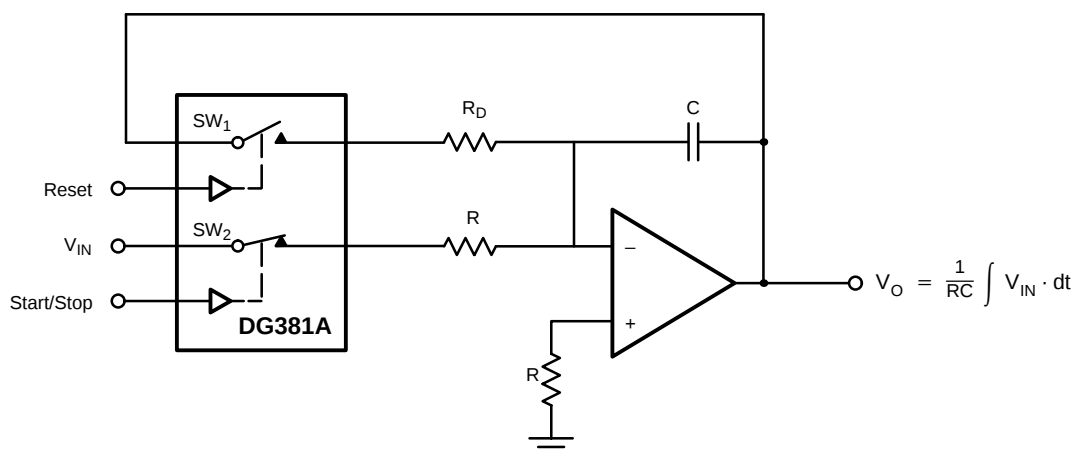


FIGURE 5. Integrator with Reset and Start/Stop