IR3513Z

DATASHEET

XPHASE3™ POL CONTROL IC

DESCRIPTION

The IR3513Z Control IC provides overall control of a scalable number of phases along with an internal gate driver, current sense/sharing, and PWM. This allows the IR3513Z to implement a stand-alone single-phase regulator or interface with additional Phase ICs to develop a power solution with any number of phases. With this arrangement, the final solution requires only 1 IC per phase to deploy 1 to X phases. Other approaches require a control IC plus 1 to X driver ICs or scalable "all-in-one" ICs that do not utilize all IC pins or circuitry leading to increased solution cost and size.

FEATURES

- 0.8V reference supports 0.8V to 5.1V output voltage with +/-0.5% system set point accuracy
- Dynamic margin function provides ± 5 % reference offset
- 1 (stand-alone) to X phase operation with additional Phase IC
- Programmable 250 KHz to 9 Mhz daisy-chain digital phase timing provides a per phase switching frequency of 250 KHz to 1.5 MHz with no external components
- Differential remote sense amplifier with 100kohm input impedance
- IC bias linear regulator control with programmable output voltage and UVLO
- Programmable converter current limit during soft-start, hiccup with delay during normal operation
- Over voltage protection communicated to Phase ICs
- System over voltage signal protects against failures such as a shorted high side MOSFET
- Detection and protection of open remote sense lines
- Open control loop protection
- 7V/2A gate drivers (4A GATEL sink current)
- Integrated boot-strap synchronous PFET
- Small thermally enhanced 32L 5 x 5mm MLPQ package

APPLICATION CIRCUIT

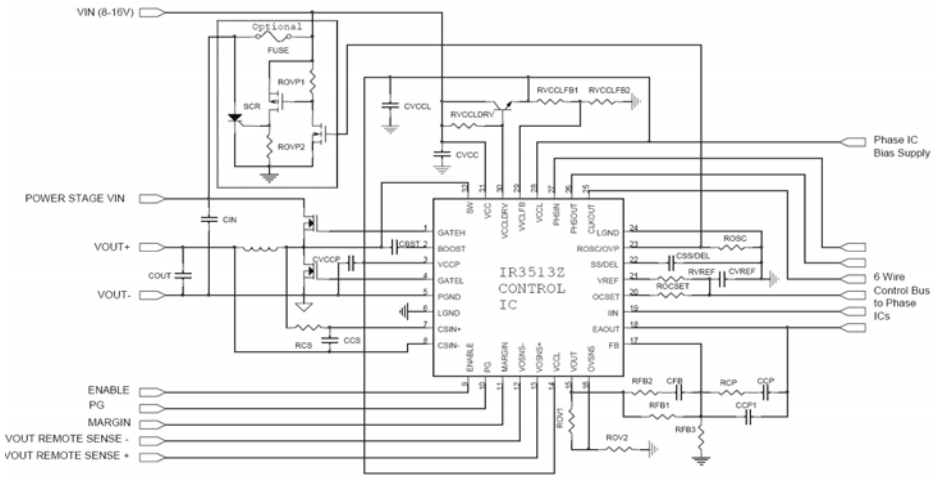


Figure 1 - IR3513Z Application Circuit

ORDERING INFORMATION

Device	Package	Order Quantity
IR3513ZMTRPBF	32 Lead MLPQ (5 x 5 mm body)	3000 per reel
* IR3513ZMPBF	32 Lead MLPQ(5 x 5 mm body)	100 piece strips

- Samples only

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	GATEH	High-side driver output and input to GATEL non-overlap comparator.
2	BOOST	Supply for high-side driver. An internal bootstrap synchronous PFET is connected between this pin and the VCCP pin.
3	VCCP	Supply for low-side driver. An internal bootstrap synchronous PFET is connected from this pin to the BOOST pin.
4	GATEL	Low-side driver output and input to GATEH non-overlap comparator.
5	PGND	Return for low side driver and reference for GATEH non-overlap comparator.
6, 24	LGND	Local Ground for internal circuitry and the IC substrate connection.
7	CSIN+	Non-Inverting input to the current sense amplifier and input to debug comparator.
8	CSIN-	Inverting input to the current sense amplifier and input to synchronous rectification disable comparator.
9	ENABLE	Enable input. A logic low applied to this pin puts the IC into fault mode. Do not float this pin as the logic state will be undefined.
10	PG	Open drain output that drives low during startup and under any external fault condition. Connect external pull-up.
11	MARGIN	Tri-state input with internal pull-up to 1.425 V. Low/High voltage shifts the Error Amplifier reference voltage Up/Down 5%. V(MARGIN) should not be biased to a voltage greater than V(VCCL).
12	VOSEN-	Inverting remote sense amplifier input. Connect to ground at the load.
13	VOSEN+	Non-inverting remote sense amplifier input. Connect to output at the load.
14, 28	VCCL	Output of the voltage regulator, power input for clock oscillator circuitry and other internal circuitry. Connect a decoupling capacitor to LGND.
15	VOUT	Remote sense amplifier output.
16	OVSNS	Over voltage sense input during normal operation.
17	FB	Inverting input to the Error Amplifier.
18	EAOUT	Output of the Error Amplifier.
19	IIN	Average current input signal from active and inactive phase IC(s). This pin is also used to communicate an over voltage condition to the phase IC(s).
20	OCSET	An external resistor tied to VREF along with a fixed internal current source programs the constant output current limit and hiccup over-current thresholds. Over-current protection can be disabled by programming the threshold higher than the possible signal on the IIN pin, but no greater than 5V (do not float this pin).
21	VREF	Reference voltage for the Error Amplifier. An external RC network to LGND programs the margin slew rate and compensates the internal buffer amp.
22	SS/DEL	An external capacitor to LGND programs converter startup and over current protection delay timing. It is also used to compensate the constant output current loop during soft start.

PIN DESCRIPTION CONTINUED

23	ROSC/OVP	A resistor to LGND to program the oscillator frequency and the OCSET bias current. Oscillator frequency equals the phase switching frequency. The pin voltage is 0.6V during normal operation and higher than 1.6V if over-voltage condition is detected.
25	CLKOUT	Frequency is equivalent to the phase switching frequency multiplied by the number of phases. Connect to CLKIN pins of phase ICs.
26	PHSOUT	Phase timing output switching at the phase frequency. Connect to PHSIN pin of the first phase IC.
27	PHSIN	Feedback input of the phase timing clock. Connect to the PHSOUT pin of the last phase IC.
29	VCCLFB	Non-inverting input of the voltage regulator error amplifier. Output voltage of the regulator is programmed by a resistor divider connected to VCCL.
30	VCCLDRV	Output of the VCCL regulator error amplifier to control an external transistor. The pin senses the input of the power supply through a resistor at power-up.
31	VCC	Power Input for under voltage lockout (UVLO) detection and supply for internal IC circuits.
32	SW	Return for high-side driver and reference for GATEL non-overlap comparator.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Operating Junction Temperature……..0 to 150°C
Storage Temperature Range…….-65°C to 150°C
MSL Rating……2
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	GATEH	34V	-0.3VDC, -5V for 100ns	3A for 100ns, 100mA DC	3A for 100ns, 100mA DC
2	BOOST	34V	-0.3V	1A for 100ns, 100mA DC	3A for 100ns, 100mA DC
3	VCCP	8V	-0.3V	n/a	5A for 100ns, 200mA DC
4	GATEL	8V	-0.3VDC, -5V for 100ns	5A for 100ns, 200mA DC	5A for 100ns, 200mA DC
5	PGND	0.3V	-0.3V	5A for 100ns, 200mA DC	n/a
6, 24	LGND	n/a	n/a	20mA	1mA
7	CSIN+	8V	-0.5V	1mA	1mA
8	CSIN-	8V	-0.5V	1mA	5mA
9	ENABLE	3.5V	-0.3V	1mA	1mA
10	PG	VCCL + 0.3V	-0.3V	1mA	20mA
11	MARGIN	8V	-0.3V	1mA	1mA
12	VOSEN-	1.0V	-0.5V	5mA	1mA
13	VOSEN+	8V	-0.5V	5mA	1mA
14, 28	VCCL	8V	-0.3V	1mA	25mA
15	VOUT	8V	-0.3V	5mA	25mA
16	OVSNS	8V	-0.3V	1mA	1mA
17	FB	8V	-0.3V	1mA	1mA
18	EAOUT	8V	-0.3V	25mA	10mA
19	IIN	8V	-0.3V	5mA	1mA
20	OCSET	8V	-0.3V	1mA	1mA
21	VDAC	3.5V	-0.3V	1mA	1mA
22	SS/DEL	8V	-0.3V	1mA	1mA
23	ROSC/OVP	8V	-0.3V	5mA	1mA
25	CLKOUT	8V	-0.3V	100mA	100mA
26	PHSOUT	8V	-0.3V	10mA	10mA
27	PHSIN	8V	-0.3V	1mA	1mA
29	VCCLFB	3.5V	-0.3V	1mA	1mA
30	VCCLDRV	10V	-0.3V	1mA	50mA
31	VCC	18V	-0.3V	1mA	1mA
32	SW	34V	-0.3V DC, -5V for 100ns	3A for 100ns, 100mA DC	n/a

Note: Maximum GATEH – SW = 8V, Maximum BOOST – GATEH = 8V

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

4.75V ≤ VCCL ≤ 7.5V, 4.75V ≤ VCCP ≤ 7.5V, 8V ≤ VCC ≤ 16V, -0.3V ≤ VOSEN- ≤ 0.3V, 0 °C ≤ T_J ≤ 125 °C, 7.75 kΩ ≤ R_{OSC} ≤ 50 kΩ

ELECTRICAL CHARACTERISTICS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C. 7.75KΩ ≤ R_{OSC} ≤ 50.0 KΩ, $C_{SS/DEL}$ = 0.1μF +/- 10%, C_{GATEH} = 3.3nF, C_{GATEL} = 6.8nF (unless otherwise specified).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VREF Reference					
System Set-Point Accuracy (per test circuit in Fig. 2)	MARGIN = OPEN	796	800	804	mV
	MARGIN = 0V	755	760	765	mV
	MARGIN = VCCL	835	840	845	mV
Source & Sink Currents	Include OCSET current	50	88	116	μA
Margin Input Thresholds	Margin Low	0.475	0.575	0.675	V
	Margin High	2.1	2.2	2.3	V
MARGIN Float Voltage		1.325	1.425	1.55	V
MARGIN Pull-up resistor		3	4	6	KΩ
Oscillator					
ROSC Voltage		0.575	0.600	0.625	V
CLKOUT High Voltage	I(CLKOUT)=-10mA, measure V(VCCL)–V(CLKOUT)			1	V
CLKOUT Low Voltage	I(CLKOUT)= 10mA			1	V
CLKOUT Phase Delay	Measure time from CLKIN < 1V to GATEH > 1V	40	75	125	ns
PHSOUT Frequency	R_{OSC}=50.0 KΩ	225	250	275	kHz
PHSOUT Frequency	R_{OSC}=24.5 KΩ	450	500	550	kHz
PHSOUT Frequency	R_{OSC}=7.75 KΩ	1.35	1.50	1.65	MHz
PHSOUT High Voltage	I(PHSOUT)= -1mA			1	V
PHSOUT Low Voltage	I(PHSOUT)= 1mA			1	V
PHSIN Threshold Voltage	Compare to V(VCCL)	30	50	70	%
Enable Input					
Threshold Voltage	ENABLE rising	815	850	885	mV
Threshold Voltage	ENABLE falling	765	800	835	mV
Hysteresis		25	50	75	mV
Bias Current	0V ≤ V(ENABLE) ≤ 3.3V	-5	0	5	μA
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Over-Current Comparator					
Input Offset Voltage	1V ≤ V(OCSET) ≤ 3.3V	-70	-40	-10	mV
OCSET Bias Current		-5%	605 / Rosc(kΩ)	+5%	μA
Over-Current Delay Counter	ROSC = 7.75 KΩ (PHSOUT=1.5MHz)		4096		Cycle
Over-Current Delay Counter	ROSC = 15.0 KΩ (PHSOUT=800kHZ)		2048		Cycle
Over-Current Delay Counter	ROSC = 50.0 KΩ (PHSOUT=250kHz)		1024		Cycle
Over-Current Limit Amplifier					
Input Offset Voltage		-10	0	15	mV
Transconductance	Note 1	0.50	1.00	1.75	mA/V
Sink Current		35	55	75	uA
Unity Gain Bandwidth	Note 1	0.75	2.00	3.00	kHz
Over Voltage Detection (OVD) Comparator					
Threshold Offset Rising	Compare to V(VREF)	60	85	105	mV
Threshold Offset Falling	Compare to V(VREF)	-15	5	25	mV
Threshold Hysteresis		55	70	80	mV
Propagation Delay to IIN	Measure time from V(VOUT) > V(VREF) (250mV overdrive) to V(IIN) transition to > 0.9 * V(VCCL).		90	180	ns
IIN Pull-up Resistance			5	20	Ω
OVSNS Input Bias Current	0V ≤ V(OVSNS) ≤ V(VCCL),	-1	0	1	μA
Over Voltage Protection (OVP) Comparator					
OVP Threshold	Step V(ISHARE) up until GATEL drives high. Compare to V(VCCL)	-1.0	-0.8	0	V
Propagation Delay	V(VCCL)=5V, Step V(ISHARE) up from V(DACIN) to V(VCCL). Measure time to V(GATEL)>4V.	0	40	70	ns
Propagation Delay to ROSC	Measure time from V(VO) > V(VDAC) (250mV overdrive) to V(ROSC/OVP) transition to >1V. Note 1.		90	300	ns
OVP ROSC High Voltage	Measure V(VCCL)-V(ROSC/OVP)	0	0.5	1.2	V
Remote Sense Differential Amplifier					
Unity Gain Bandwidth	Note 1	3.0	6.4	9.0	MHz
Input Offset	Relative to [V(VOSEN+) - V(VOSEN-)]. 1.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 5.5V 0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.5V	 -0.2 -3	 0 0	 0.2 3	% mV
Source Current	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 5.5V	0.5	1.0	1.7	mA
Sink Current	Vout=0.5V Vout=5.5V	1 11	4 25	9 34	mA
Slew Rate	Note 1	2	4	8	V/us
Input Impedance		63	100	185	kΩ
VOSEN+ Input Voltage Range	V(VCCL)=7V			5.5	V
High Voltage	V(VCCL) – V(VO)		0.03	0.1	V
Low Voltage	V(VCCL)=7V			250	mV

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Delay					
Start Delay		1.0	2.2	3.5	ms
Soft Start Time		0.9	1.5	4.5	ms
PG Delay		0.4	1.3	3.8	ms
OC Delay Time	V(IIN) – V(OCSET) = 500 mV	75	125	300	us
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.7	1.4	1.9	V
Charge Current		30	50	65	μA
Discharge Current		2	4	6	μA
Charge/Discharge Current Ratio		10	12	17	μA/μA
Charge Voltage		2.8	3	3.3	V
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL rising – Note 1		80		mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL falling – Note 1		120		mV
Delay Comparator Hysteresis	Note 1		30		mV
Discharge Comparator Threshold		125	200	275	mV
Error Amplifier					
Input Offset Voltage	Measure V(FB) – V(VREF). Note 2	-1	0	1	mV
FB Bias Current		-1	0	1	μA
DC Gain	Note 1	100	110	120	dB
Bandwidth	Note 1	20	30	40	MHz
Slew Rate	Note 1	7	12	20	V/μs
Sink Current		0.40	0.85	1.00	mA
Source Current		5	8	12	mA
Maximum Voltage	Measure V(VCCL) – V(EAOUT)	500	780	950	mV
Minimum Voltage			120	250	mV
Open Voltage Loop Detection Threshold	Measure V(VCCL) - V(EAOUT), Relative to Error Amplifier maximum voltage.	100	500	1000	mV
Open Voltage Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUT) = V(VCCL) to PG = low.		8		Pulses
Headroom Control					
Activation Voltage	V(VCC) – V(CSIN-)	2.7	2.95	3.3	V
FB Bias Current	V(VCC) – V(CSIN-) = 1.0V	-640	-470	-300	uA
PG Comparator Threshold		-18.5	-13.5	-9	uA
PG Comparator Hysteresis		5	8	13.5	uA
VCC Under Voltage Lockout Comparator (UVLO)					
Start Threshold		6.9	7.4	7.9	V
Stop Threshold		6.5	7.0	7.5	V
Hysteresis	Start – Stop	350	450	650	mV

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Open Sense Line Detection					
Sense Line Detection Active Comparator Threshold Voltage		150	200	250	mV
Sense Line Detection Active Comparator Offset Voltage	V(VOUT) < [V(VOSEN+) – V(LGND)] / 2	40	60	90	mV
VOSEN+ Open Sense Line Comparator Threshold	Compare to V(VCCL)	87.5	90	92.5	%
VOSEN- Open Sense Line Comparator Threshold		0.36	0.40	0.44	V
Sense Lines Detection Source Currents	V(VOUT) = 100mv	250	500	750	uA
VCCL Regulator Amplifier					
Reference Feedback Voltage		1.15	1.19	1.23	V
VCCLFB Bias Current		-1	0	1	uA
VCCLDRV Sink Current		10	30		mA
UVLO Start Threshold	Compare to V(VCCL)	90	94	98	%
UVLO Stop Threshold	Compare to V(VCCL)	82	86	90	%
Hysteresis	Compare to V(VCCL)	7.0	8.5	9.5	%
Gate Drivers					
GATEH Source Resistance	BOOST – SW = 7V. Note 1		1.0	2.5	Ω
GATEH Sink Resistance	BOOST – SW = 7V. Note 1		1.0	2.5	Ω
GATEL Source Resistance	VCCP – PGND = 7V. Note 1		1.0	2.5	Ω
GATEL Sink Resistance	VCCP – PGND = 7V. Note 1		0.4	1.0	Ω
GATEH Source Current	BOOST=7V,GATEH=2.5V,SW=0V. Note 1		2.0		A
GATEH Sink Current	BOOST=7V,GATEH=2.5V,SW=0V. Note 1		2.0		A
GATEL Source Current	VCCP=7V, GATEL=2.5V, PGND=0V Note 1		2.0		A
GATEL Sink Current	VCCP=7V, GATEL=2.5V, PGND=0V Note 1		4.0		A
GATEH Rise Time	BOOST – SW = 7V, measure 1V to 4V transition time		5	10	ns
GATEH Fall Time	BOOST - SW = 7V, measure 4V to 1V transition time		5	10	ns
GATEL Rise Time	VCCP – PGND = 7V, Measure 1V to 4V transition time		10	20	ns
GATEL Fall Time	VCCP – PGND = 7V, Measure 4V to 1V transition time		5	10	ns
GATEL low to GATEH high delay	BOOST = VCCP = 7V, SW = PGND = 0V, measure time from GATEL falling to 1V to GATEH rising to 1V	10	20	40	ns
GATEH low to GATEL high delay	BOOST = VCCP = 7V, SW = PGND = 0V, measure time from GATEH falling to 1V to GATEL rising to 1V	10	20	40	ns
Disable Pull-Down Resistance	Ta=25 °C Note 1		80	130	kΩ

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PWM Comparator					
PWM Ramp Slope		42	52.5	57	mV/ DC%
Input Offset Voltage	Note 1	-5	0	5	mV
Minimum Pulse Width	Note 1		65	75	ns
Minimum GATEH Turn-off Time		20	80	160	ns
Current Sense Amplifier					
CSIN+/- Bias Current		-200	0	200	nA
CSIN+/- Bias Current Mismatch	Note 1	-50	0	50	nA
Input Offset Voltage	CSIN+ = CSIN- = VREF. Measure input referred offset from VREF	-1	0	1	mV
Gain	Csin+=25mV+Csin-	30.5	33.0	35.5	V/V
Unity Gain Bandwidth	C(IIN)=10pF. Measure at IIN. Note 1	4.8	6.8	8.8	MHz
Slew Rate	Note 1		6		V/μs
Differential Input Range		-10		50	mV
Differential Input Range		-5		50	mV
Common Mode Input Range		-0.2		Note3	V
Rout at T_J = 25 °C	Note 1	2.3	3.0	3.7	kΩ
Rout at T_J = 65 °C		2.9	3.7	4.6	kΩ
Rout at T_J = 125 °C		3.6	4.7	5.4	kΩ
ISHARE Source Current		500			μA
ISHARE Sink Current		500			μA
Share Adjust Amplifier					
Input Offset Voltage	Note 1	-3	0	3	mV
Differential Input Range	Note 1	-1		1	V
Gain	CSIN+ = CSIN- = VREF, Adjust V(IIN) from V(Ramp floor) – 10mV to V(Ramp floor) + 10mV and measure change in PWM Ramp Start Voltage. Note 1.	4	5.0	6	V/V
Unity Gain Bandwidth	Note 1	4	8.5	17	kHz
Maximum PWM Ramp Adjust Voltage	CSIN+ = CSIN- = VREF, EAOUT =LGND, and V(IIN) = V(Ramp floor) - 100mV. Maximum adjust voltage =V(PWMRMP) – V(Ramp floor)	90	150	250	mV
Minimum PWM Ramp Adjust Voltage	CSIN+ = CSIN- = VREF, EAOUT =LGND, and V(ISHARE) = V(Ramp floor) + 100mV. Minimum adjust voltage = V(PWMRMP) – V(Ramp floor)	-230	130	-70	mV
Body Brake Comparator					
Threshold Voltage Increasing	Compare to V(Ramp floor)	-225	-125	-25	mV
Threshold Voltage decreasing	Compare to V(Ramp floor)	-315	-215	-115	mV
Threshold Hysteresis		40	90	140	mV
Propagation Delay	VCCL = 5V. Measure time from EAOUT < V(VREF) (200mV overdrive) to GATEL transition to < 4V.	20	40	70	ns

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Synchronous Rectification Disable Comparator					
Threshold Voltage	The ratio of V(CSIN-) / V(VREF), below which V(GATEL) is always low.	63	75	89	%
Negative Current Comparator					
Input Offset Voltage	Note 1	-16	0	16	mV
Propagation Delay Time	Apply step voltage to V(CSIN+) – V(CSIN-). Measure time to V(GATEL)< 1V.		200	400	ns
Bootstrap Diode					
Forward Voltage	I(BOOST) = 30mA, 6V ≤ VCCL ≤ 7V	180	260	470	mV
Debug Comparator					
Threshold Voltage	Compare to V(VCCL)	-260	-150	-60	mV
PG Output					
Output Voltage	I(PG) = 4mA		150	300	mV
Leakage Current	V(PG) = 5.5V		0	10	μA
VCC PG Activation Threshold	I(PG)=4mA, V(PG)<300mV	1	2	3.5	V
Output Under Voltage Comparator					
Threshold Voltage Falling		0.600	0.665	0.730	V
Threshold Voltage Rising		0.660	0.715	0.770	V
Threshold Hysteresis		20	50	90	mV
General					
VCC Supply Current	V(VCC) – V(VOUT) > 2.5V	1.1	3.0	6.1	mA
VCCL Supply Current		9	14	19	mA
VCCP Supply Current	V(VCCP)=7V, V(BOOST)=7V	50	150	300	uA
BOOST Supply Current	4V ≤ V(BOOST) ≤ 30V	1.2	3.5	5.8	mA
SW Floating Voltage	Measured in the application		0.3		V

Note 1: Guaranteed by design, but not tested in production
Note 2: VREF Output is trimmed to compensate for Error & Remote Sense Amp input offsets
Note 3: VCCL-0.5V or VCC – 2.5V, whichever is lower

SYSTEM SET POINT TEST

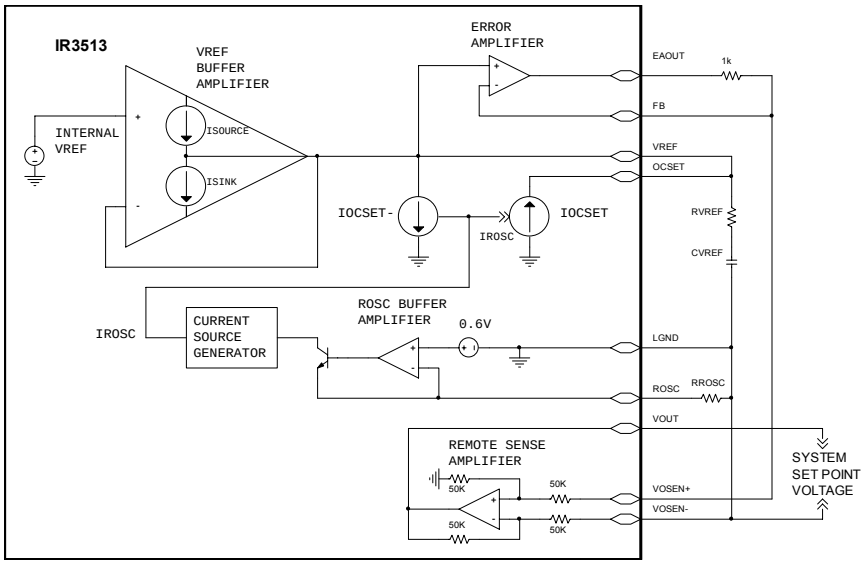


Figure 2 - System Set Point Test Circuit

SYSTEM THEORY OF OPERATION

PWM Control Method

The PWM block diagram of the *XPhase*™ architecture is shown in Figure 3. Feed-forward voltage mode control with trailing edge modulation is used. A voltage-type error amplifier with high-gain (110dB) and wide-bandwidth is used for the control loop. It is not unity gain stable. The power-stage input voltage is sensed by the IR3513Z, and optional phase ICs, to provide feed-forward control. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

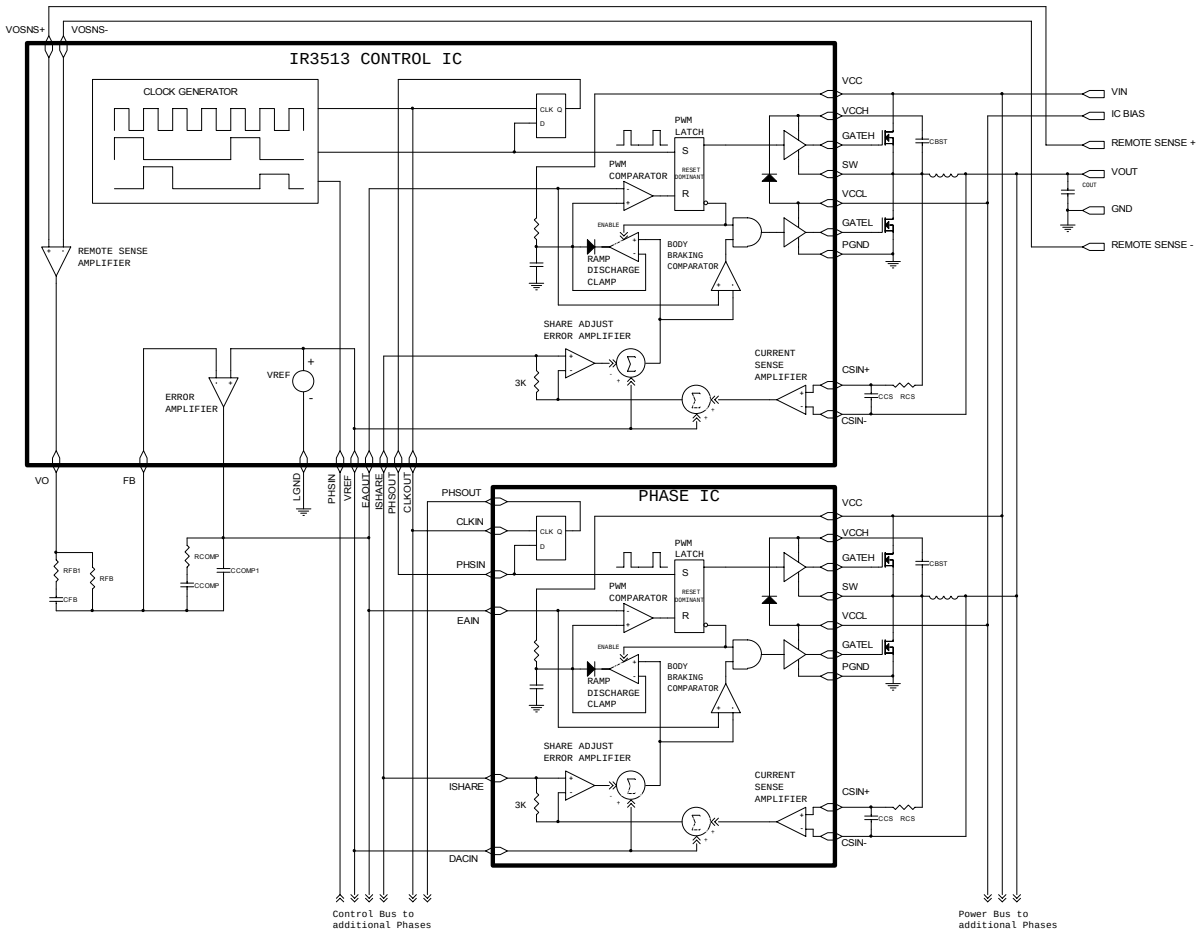


Figure 3 - PWM Block Diagram

Frequency and Phase Timing Control

The oscillator system clock frequency is programmable from 500 kHz to 9 MHZ by an external resistor. The IR3513Z system clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop, where the IR3513Z phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. The last phase IC (PHSOUT) is connected back to PHSIN of the control IC to complete the loop. During power up, the IR3513Z sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. Figure 4 shows the phase timing for a four-phase converter. For single-phase operation, PHSOUT (pin 26) and PHSIN (pin 27) must be shorted together to prevent an Open Control Loop fault from occurring.

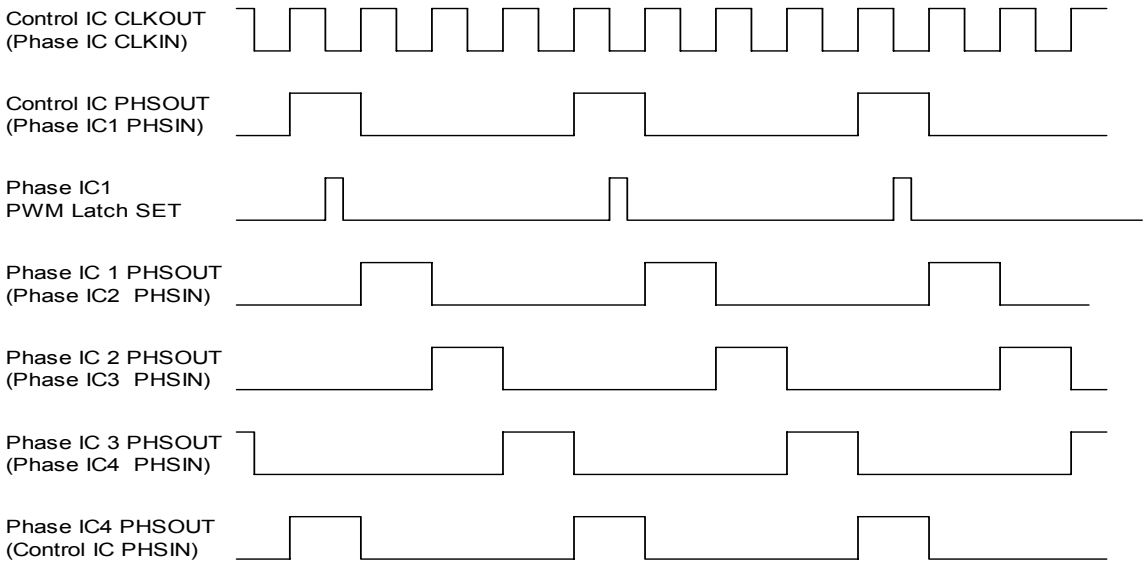


Figure 4 - Five Phase Oscillator Waveforms

PWM Operation

Upon receiving the falling edge of a clock pulse, the PWM latch is set; the PWM ramp voltage begins to increase; the low side driver is turned off, and the high side driver is then turned on after the non-overlap time. When the PWM ramp voltage exceeds the error amplifier's output voltage the PWM latch is reset. This turns off the high side driver and then turns on the low side driver after the non-overlap time and activates the ramp discharge clamp. The ramp discharge clamp quickly discharges the PWM ramp capacitor to the output voltage of the share adjust amplifier in the phase IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in up to 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease, which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VREF.

Figure 5 depicts PWM operating waveforms under various conditions.

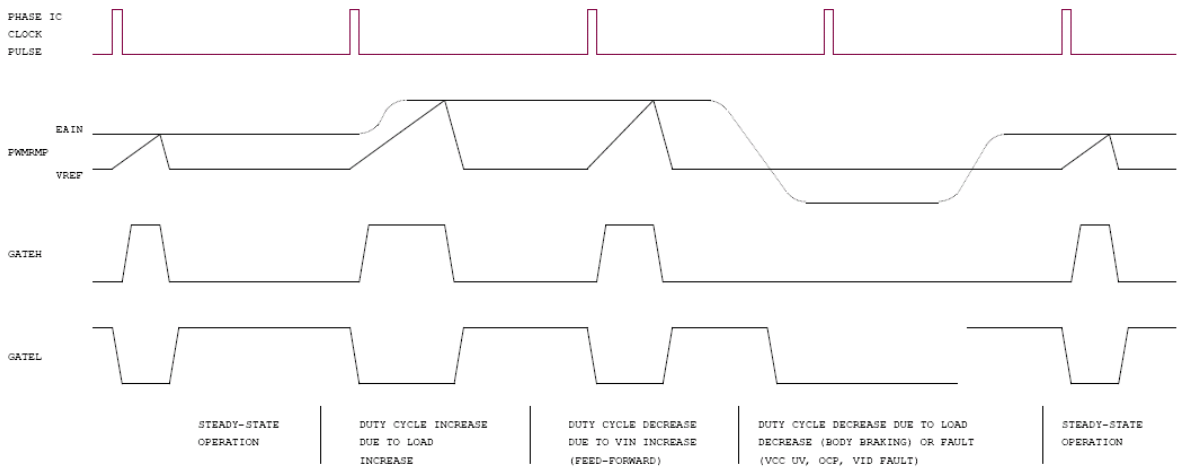


Figure 5 - PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often higher than the output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "body braking comparator". If the error amplifier's output voltage drops below the VREF voltage or a programmable voltage, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 6. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

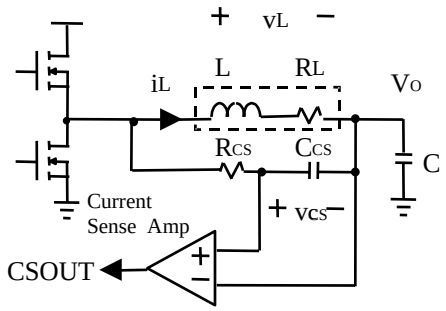


Figure 6 - Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is included in both the IR3513Z and optional phase ICs, as shown in Figure 6. Its gain is nominally 33 at 25ºC, and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the VREF voltage and sent to other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection. The input offset of this amplifier is calibrated to +/- 1mV in order to reduce the current sense error.

The input offset voltage is the primary source of error for the current share loop. In order to achieve very small input offset error and superior current sharing performance, the current sense amplifier continuously calibrates itself. This calibration algorithm creates ripple on ISHARE bus with a frequency of fsw/896.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3513Z THEORY OF OPERATION

Block Diagram

The IR3513Z Block diagram is shown in Figure 7, and specific features are discussed in the following sections.

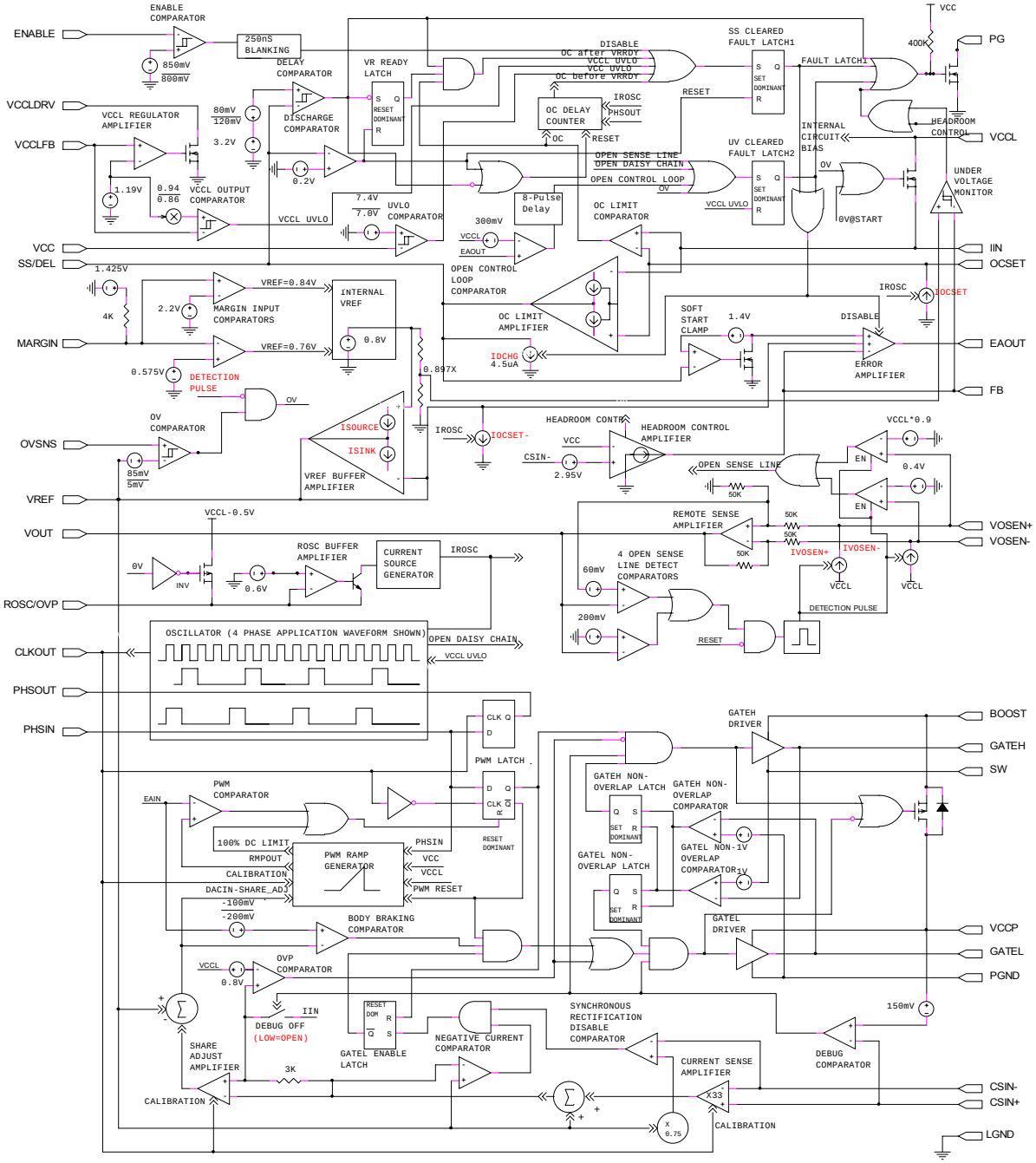


Figure 7 - Block Diagram

VREF Control

The MARGIN input comparators monitor the MARGIN pin and control the internal reference voltage whose output is sent to the VREF buffer amplifier. The output of the buffer amplifier is the VREF pin. The VREF voltage, input offsets of error amplifier and remote sense differential amplifier are post-package trimmed to provide 0.8% **system set-point** accuracy. The actual VREF voltage does not determine the system accuracy, which has a wider tolerance.

The IR3513Z can accept changes in the MARGIN input while operating and vary the VREF voltage accordingly. The slew rate of the voltage at the VREF pin can be adjusted by an external capacitor between VREF pin and LGND pin. A resistor connected in series with this capacitor is required to compensate the VREF buffer amplifier. Margin transitions result in a smooth analog transition of the VREF voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

Remote Voltage Sensing

VOSEN+ and VOSEN- are used for remote sensing and are connected directly to the load. The remote sense differential amplifier with high speed, low input offset and low input bias current ensures accurate voltage sensing and fast transient response.

Start-up Sequence

The IR3513Z has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start timing, over-current protection delay and hiccup mode timing. A charge current of 52.5uA (typical) and discharge current of 4.5uA (typical) control the up and down slope of the voltage at the SS/DEL pin respectively.

Figure 8 shows normal converter start-up. If there is no fault, the SS/DEL pin will start charging. The error amplifier output EAOUT is clamped low until SS/DEL reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage, less the 1.4V offset, until the converter output reaches the level determined by the VREF (0.8 V typically) inputs. The SS/DEL voltage continues to increase until it rises above 3.12V and allows the PG signal to be asserted. SS/DEL finally settles at 3.2V indicating the end of the soft start.

VCCL under voltage lock out, over current, as well as a low signal on the ENABLE input immediately sets the fault latch, which causes the EAOUT pin to drive low turning off the phase IC drivers. The PG pin also drives low, and SS/DEL begins to discharge until the voltage reaches 0.2V. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

Other fault conditions, such as over voltage, open sense lines, and open daisy chain, set different fault latches, which start discharging SS/DEL, pull down EAOUT voltage and drive PG low. However, the latches can only be reset by cycling VCCL power.

If SS/DEL pin is pulled below 0.7V, the converter can be disabled.

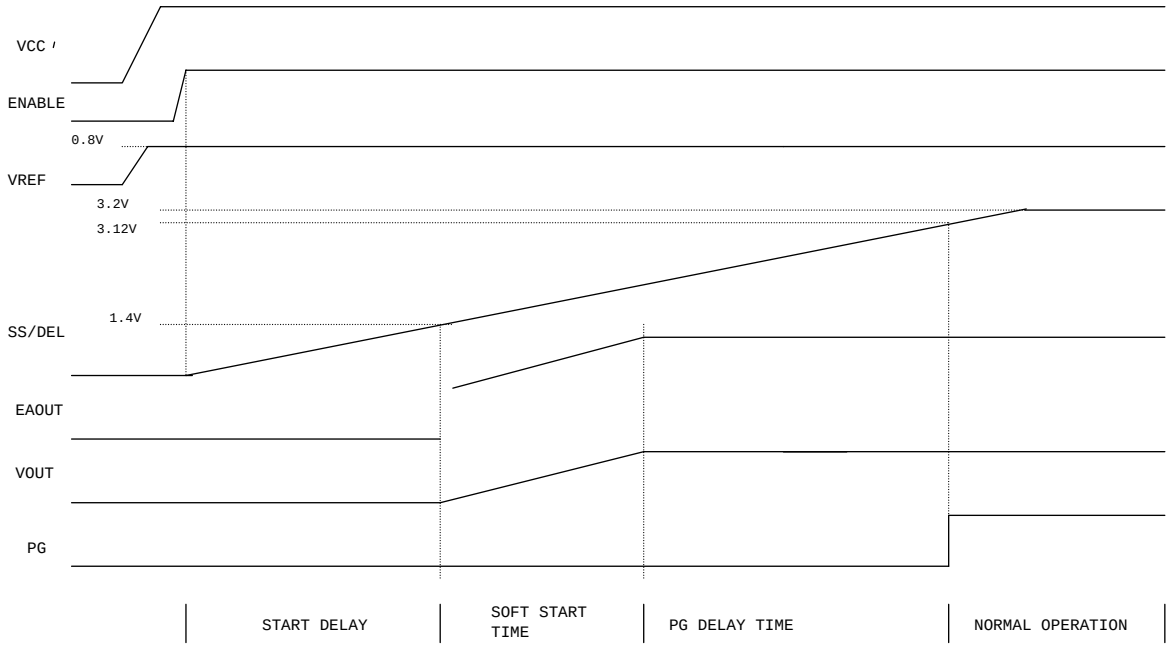


Figure 8 - Start-up sequence

Constant Over-Current Control during Soft Start

The over-current limit threshold is set by a resistor connected between OCSET and VREF pins. If the IIN pin voltage, which is proportional to the average current plus VREF voltage, exceeds the OCSET voltage during soft start, the constant over-current control is activated.

Figure 9 shows the constant over-current control with delay during soft start. The delay is required since over-current conditions can occur as part of normal operation due to inrush current.

If an over-current occurs during soft start (before PG is asserted), the SS/DEL voltage is regulated by the over current amplifier to limit the output current below the threshold set by OCSET voltage. If the over-current condition persists after the delay time is reached, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs. The SS/DEL capacitor will discharge until it reaches 0.2V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the constant over-current control actions will repeat and the converter will be in hiccup mode. The delay time is controlled by a counter, which is triggered by the oscillator. The counter values vary with switching frequency per phase in order to have a similar delay time for different switching frequencies.

Over-Current Hiccup Protection after Soft Start

The over current limit threshold is set by a resistor connected between OCSET and VREF pins. Figure 9 shows the constant over-current control with delay after PG is asserted. The delay is required since over-current conditions can occur as part of normal operation due to load transients or margin transitions.

If the IIN pin voltage, which is proportional to the average current plus VREF voltage, exceeds the OCSET voltage after PG is asserted, it will initiate the discharge of the capacitor at SS/DEL. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 120mV offset of the delay comparator, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs and de-asserting the PG signal. The output current is not controlled during the delay time. The SS/DEL capacitor will discharge until it reaches 200 mV and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the over-current action will repeat and the converter will be in hiccup mode.

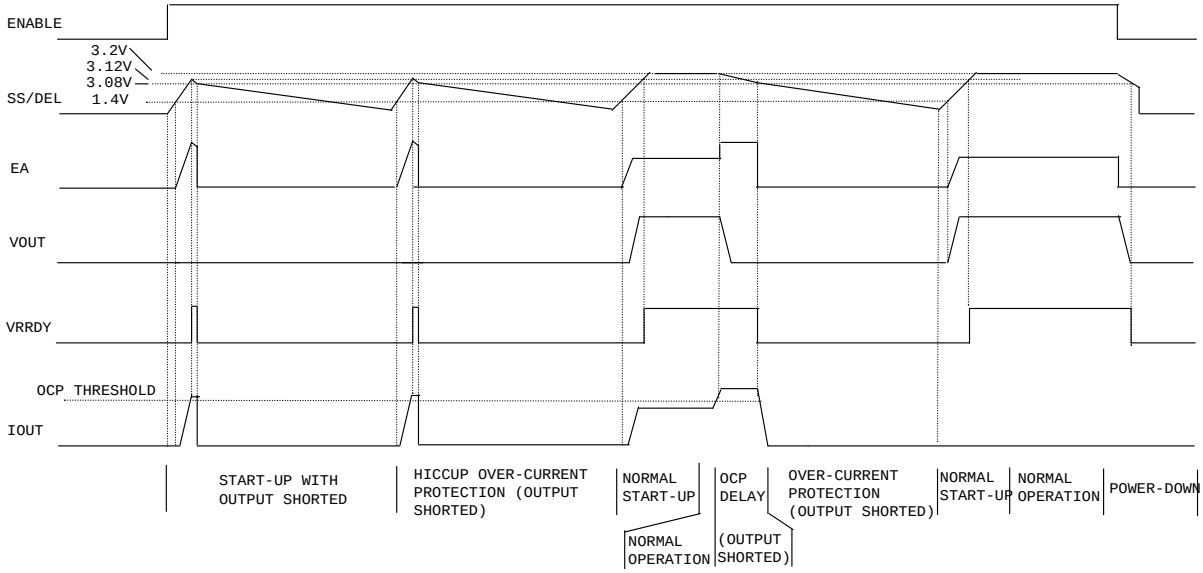


Figure 9 - Constant over-current control waveforms during and after soft start

Linear Regulator Output (VCCL)

The IR3513Z has a built-in linear regulator controller, and only an external NPN transistor is needed to create a linear regulator. The output voltage can be programmed between 4.75V and 7V by the resistor divider at VCCLFB pin. The regulator output powers the gate drivers of the phase ICs and circuits in the control IC, and the voltage is usually programmed to optimize the converter efficiency. The linear regulator can be compensated by a 4.7uF capacitor at the VCCL pin. As with any linear regulator, due to stability reasons, there is an upper limit to the maximum capacitor value that can be used at this pin and it is a function of the number of phases used in the multiphase architecture and their switching frequency. Figure 10 shows the stability plots for the linear regulator with 5 phases switching at 750 kHz.

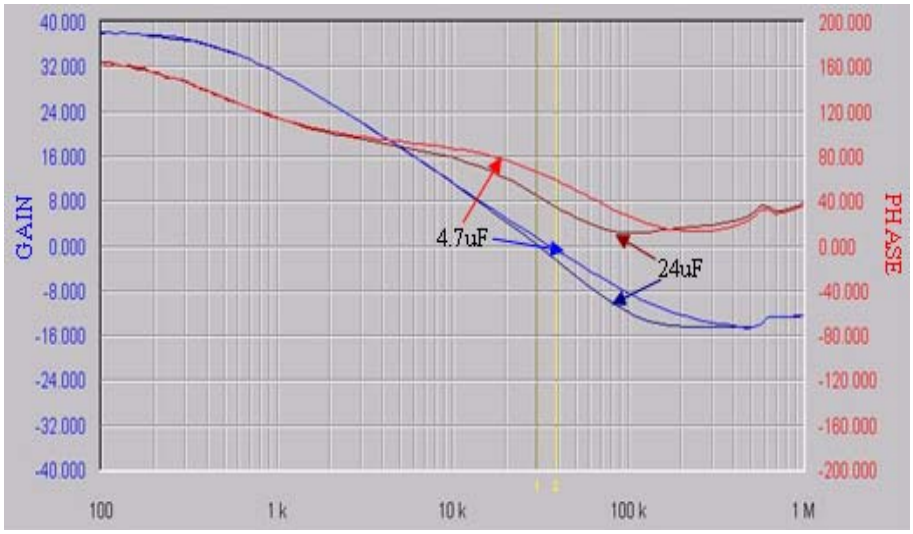


Figure 10 - VCCL regulator stability with 5 phases and PHSOUT equals 750 kHz

VCCL Under Voltage Lockout (UVLO)

The IR3513Z IC monitors both the Vcc and VCCL for under voltage condition. During power up, the fault latch will be reset if VCCL is above 94% (typical) of the voltage set by resistor divider at VCCLFB pin and the VCC exceeds 7.5V (typical). If VCCL voltage drops below 86% (typical) of the set value or VCC drops below 7V (typical), the fault latch will be set.

Power Good (PG)

The PG pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft start, the PG remains low until the output voltage is in regulation and SS/DEL is above 3.12V. The PG pin becomes low if the fault latch, over voltage latch, open sense line latch, or open daisy chain latch is set. A high level at the PG pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

Open Voltage Loop Detection

The output voltage range of error amplifier is detected all the time to ensure the voltage loop is in regulation. If any fault condition forces the error amplifier output above VCCL-0.3V for 8 switching cycles, the fault latch is set. The fault latch can only be cleared by cycling power to VCCL.

Load Current Indicator Output

The IIN pin voltage represents the average current of the converter plus the VREF voltage. The load current information can be retrieved by a differential amplifier which subtracts the VREF voltage from the IIN voltage.

Enable Input

Pulling the ENABLE pin below 0.8V sets the Fault Latch and a voltage above 0.85V enables the soft start of the converter.

Over Voltage Protection (OVP)

Output over-voltage can occur during normal operation if a high side MOSFET short or other failure occurs. The over-voltage protection comparator monitors the OVSNS pin voltage. If the OVSNS pin voltage exceeds VREF by 85mV, as shown in Figure 11, the ROSC/OVP pin voltage is driven to V(VCCL) - 1V sending an over voltage signal to the host system. The ROSC/OVP pin can also be connected to a crowbar circuit, which pulls the converter input low in over voltage conditions.

The over voltage condition also sets the over voltage fault latch, which pulls the error amplifier output low to turn off the converter output. At the same time IIN pin (ISHARE of phase ICs) is pulled up to VCCL to communicate the over voltage condition to phase ICs (if present), as shown in Figure 11. The OVP circuit overrides the normal PWM operation and will fully turn-on the low side MOSFET within approximately 150ns. The low side MOSFET will remain on until ISHARE pin voltage drops below V(VCCL) - 800mV, which signals the end of over voltage condition. An over voltage fault condition is latched in the IR3513Z and can only be cleared by cycling power to VCCL.

In the event of a high side MOSFET short before power up, the OVP flag is activated with as little supply voltage as possible, as shown in Figure 12. The OVSN pin is compared against a fixed voltage of 1.73V (typical) for OVP conditions at power-up. The ROSC/OVP pin will be pulled higher than 1.6V with VCCLDRV voltage as low as 1.8V. An external MOSFET or comparator should be used to disable the silver box, activate a crowbar, or turn off the supply source. The 1.8V threshold is used to prevent false over-voltage triggering caused by pre-charging of output capacitors.

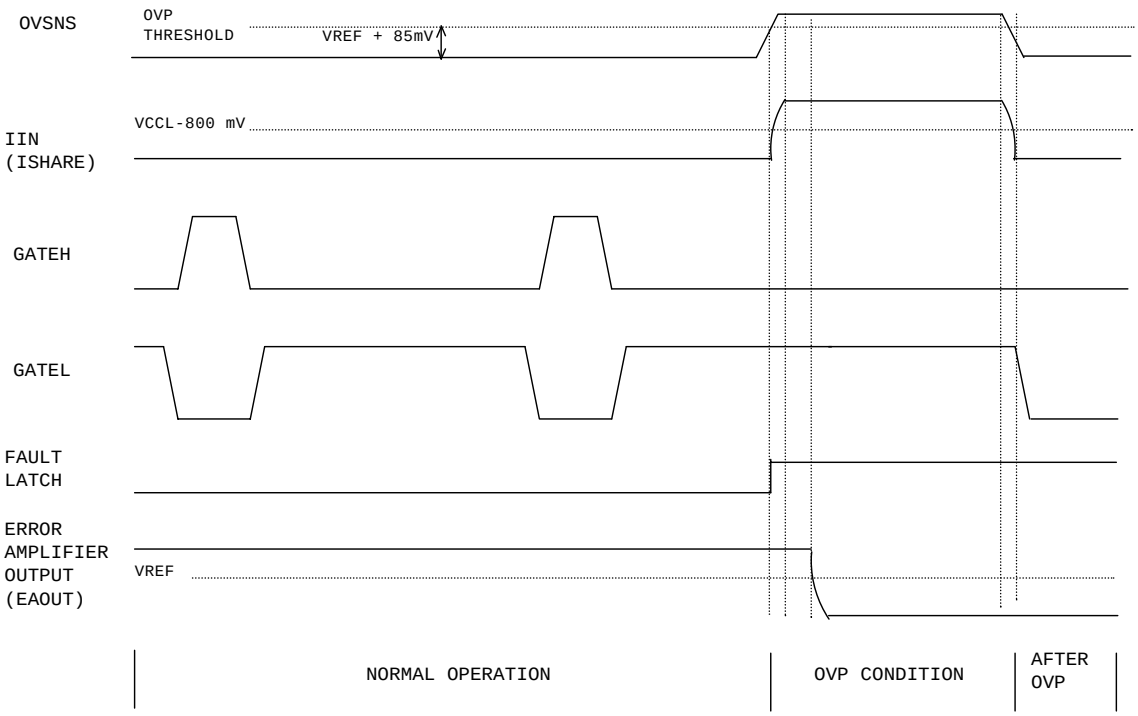


Figure 11 Over-voltage protection during normal operation

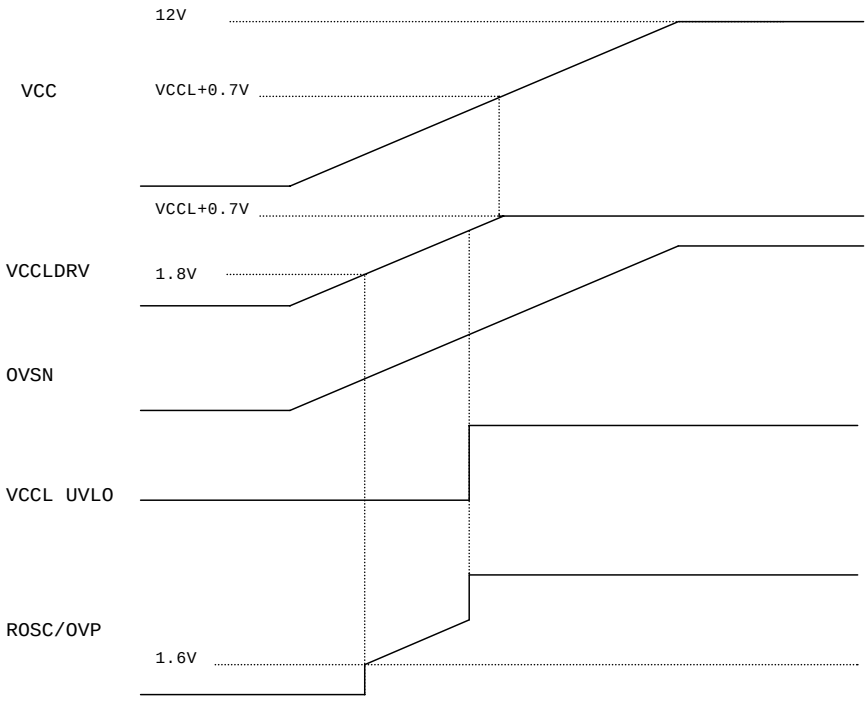


Figure 12 - Over-voltage protection during power-up

Pre-charging of the converter output voltage may trigger OVP. If the converter output is pre-charged above 1.73V as shown in Figure 17, ROSC/OVP pin voltage will be higher than 1.6V when VCCLDRV voltage reaches 1.8V. ROSC/OVP pin voltage will be VCCLDRV-1V and rise with VCCLDRV voltage until VCCL is above UVLO threshold, after which ROSC/OVP pin voltage will be VCCL-1V. The converter cannot start unless the over voltage condition stops and VCCL is cycled. If the converter output is pre-charged 130mV above VREF but lower than 1.73V, as shown in Figure 17, the converter will soft start until SS/DEL voltage is above 3.92V (4.0V-0.08V). Then, over voltage comparator is activated and fault latch is set.

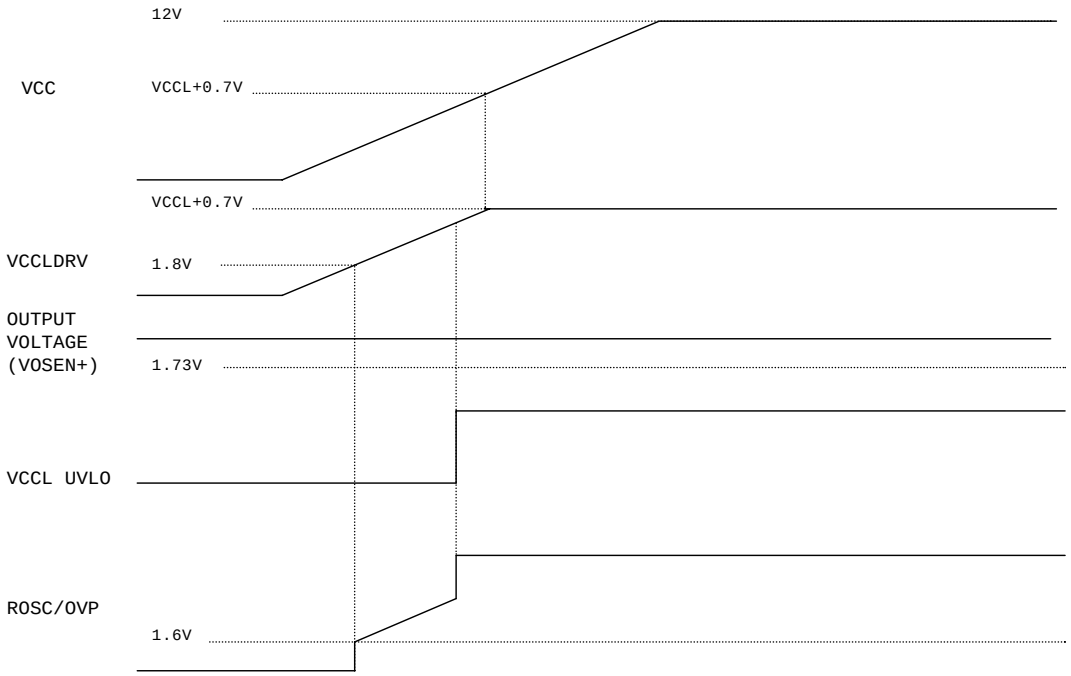


Figure 13 - Over-voltage protection with pre-charging converter output Vo > 1.73V

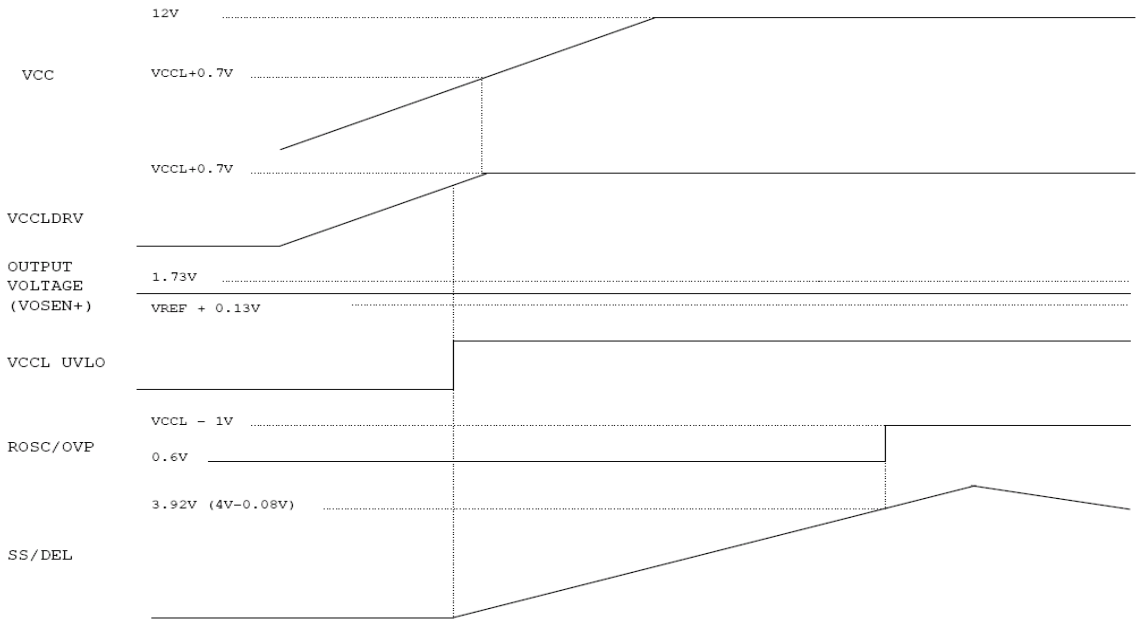


Figure 14 - Over-voltage protection with pre-charging converter output VREF + 0.13V <Vo < 1.73V

During a MARGIN up to a MARGIN down event (80mV excursion on VREF), OVP may be triggered since the OVP threshold is a fixed 85mV above VREF. This can occur due to large output capacitance and light/no load operation where the output voltage remains high while the OVP threshold falls.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered and provide effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter.

Error Amplifier Head Room Control

In high converter output voltage applications, there may not be enough head room in error amplifier and current sense amplifiers of phase ICs when VCC is just above UVLO start and stop thresholds. A head room control circuit is implemented to ensure V(VCC) – V(VO) > 2.5V by sourcing extra current to the resistor connecting to FB pin. When this circuit is activated, the converter voltage is lower than the required and therefore the PG is also driven low.

Open Remote Sense Line Protection

If either remote sense line VOSEN+ or VOSEN- or both is open, the output of remote sense amplifier (VOUT) drops. The IR3513Z monitors VO pin voltage continuously. If VOUT voltage is lower than 200 mV, two separate pulse currents are applied to VOSEN+ and VOSEN- pins respectively to check if the sense lines are open. If VOSEN+ is open, a voltage higher than 90% of V(VCCL) will be present at VOSEN+ pin and the output of open line detect comparator will be high. If VOSEN- is open, a voltage higher than 400mV will be present at VOSEN- pin and the output of open line detect comparator will be high. The open sense line fault latch is set, which pulls error amplifier output low immediately and shut down the converter. SS/DEL voltage is discharged, and the fault latch can only be reset by cycling VCCL power.

Open Daisy Chain Protection

IR3513Z checks the daisy chain every time it powers up. It starts a daisy chain pulse on the PHSOUT pin and detects the feedback at PHSIN pin. If no pulse comes back after 30 CLKOUT pulses, the pulse is restarted again. If the pulse fails to come back the second time, the open daisy chain fault is registered, and SS/DEL is not allowed to charge. The fault latch can only be reset by cycling the power to VCCL.

After powering up, the IR3513Z monitors PHSIN pin for a phase input pulse equal or less than the number of phases detected. If PHSIN pulse does not return within the number of phases in the converter, another pulse is started on PHSOUT pin. If the second started PHSOUT pulse does not return on PHSIN, an open daisy chain fault is registered.

Phase Number Determination

After a daisy chain pulse is started, the IR3513Z checks the timing of the input pulse at PHSIN pin to determine the phase number.

Output Voltage Under-voltage Monitoring

The IR3513Z compares the FB pin to a voltage, V, equal to 0.897×Vref. If the FB pin is 50mV (typical) below the aforementioned V, the output voltage under-voltage monitor will trigger, pulling the PG pin low. The output voltage under-voltage monitor does not effect switching of the phases or soft start.

Fault Table

The Fault Table below describes the different faults that can occur and how IR3513Z would react to protect the supply and the load from possible damage. The fault types that can occur are listed in row 1. Row 2 has the method that a fault is cleared. The first 4 faults are latched in the UV fault latch and the VCCL power has to be recycled by switching off the input and switching it back on for the converter to work again. The rest of the faults (except for UVLO Vout) are latched in the SS fault latch and do not need to recycle the VCCL power in order for IR3513Z to resume operation. IR3513Z will automatically resume operation when these fault conditions no longer apply in the system. Most of the faults disable the error amplifier (EA) and discharge the soft start capacitor. All the faults flag PGood. PGood returns back to high when the faults are cleared. The delay row shows how long it takes IR3513Z to react after detecting a fault condition. Delays are provided to minimize the possibility of nuisance faults.

Fault table

	Fault Type									
	Open Daisy	**Open Control Loop**	**Open Sense Line**	**Over Voltage**	**Disable**	**VCC UVLO**	**VCCL UVLO**	**OC Before Start-up**	**OC After Start-up**	**VOUT UVLO**
Fault Clearing Method	Recycle VCCL				Resume Normal Operation when Condition Clears					
Error Amp Disabled	Yes									No
ROSC/OVP & IIN drive high until OV clears	No			Yes	No					
SS/DEL Discharge	Yes									No
Flags PGood	Yes									
Delay?	30 Clock Pulses	8 PHSOUT Pulses	No	No	250 ns Blank Time	No		PHSOUT Pulses. Count Programmed by ROSC value	SS/DEL Discharge Threshold	No

APPLICATIONS INFORMATION

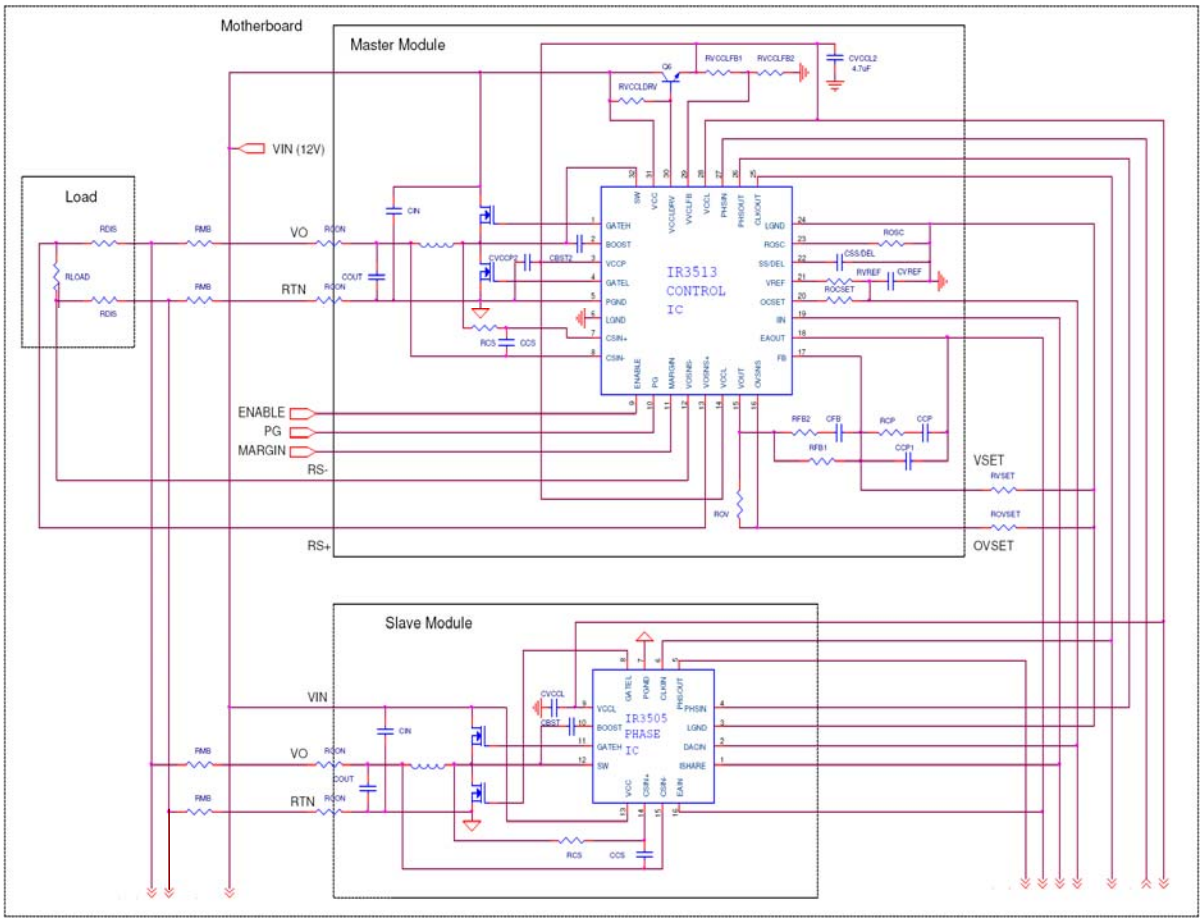


Figure 15 - Scalable Master (IR3513Z) & Slave (IR3505Z) POL modules with programmable output voltage and redundant OVP sense

DESIGN PROCEDURES

IR3513Z EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

The oscillator of IR3513Z generates square-wave pulses to synchronize the phase ICs. The switching frequency of the each phase converter equals the PHSOUT frequency, which is set by the external resistor ROSC according to the curve in Figure 16. The CLKOUT frequency equals the switching frequency multiplied by the phase number.

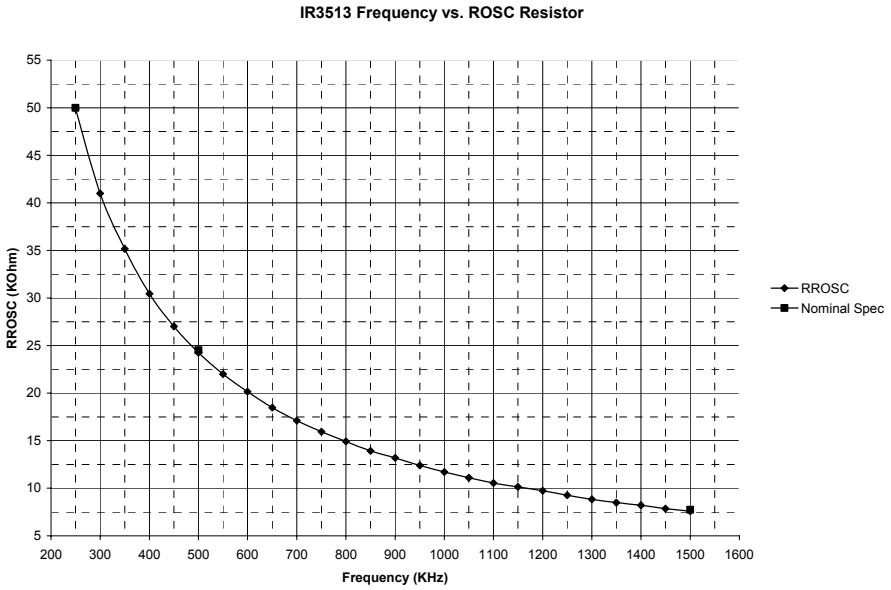


Figure 16 Operational Frequency vs Rosc Resistor

Soft Start Capacitor *CSS/DEL*

The CSS/DEL capacitor programs four different time parameters, i.e. soft start delay time, soft start time, VR ready delay time and over-current fault latch delay time after VR ready. These parameters can be calculated with the following equations:

$$T_{ssdelay} = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{52.5 * 10^{-6}} \quad (1)$$

$$T_{ss} = \frac{C_{SS/DEL} * Vref}{I_{CHG}} = \frac{C_{SS/DEL} * 0.8}{52.5 * 10^{-6}} \quad (2)$$

$$T_{PG\_delay} = \frac{C_{SS/DEL} * (3.12 - Vref)}{I_{CHG}} = \frac{C_{SS/DEL} * 2.32}{52.5 * 10^{-6}} \quad (3)$$

$$T_{OC\_delay} = \frac{C_{SS/DEL} * 120 * 10^{-3}}{I_{CHG}} = \frac{C_{SS/DEL} * 120 * 10^{-3}}{52.5 * 10^{-6}}. \quad (4)$$

Over Current Setting Resistor *ROCSET*

The inductor DC resistance is utilized to sense the inductor current. The copper wire of the inductor has a constant temperature coefficient of 3850 ppm/°C, and therefore the maximum inductor DCR can be calculated from (5). R_{L_MAX} and R_{L_ROOM} are the inductor DCR value at maximum temperature (T_{L_MAX}) and room temperature ($T_{\_ROOM}$), respectively.

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})] \quad (5)$$

The total input offset voltage (V_{CS_TOFST}) of current sense amplifier in phase ICs is the sum of input offset (V_{CS_OFST}) of the amplifier itself and that created by the amplifier input bias current flowing through the current sense resistor R_{CS}.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS} \quad (6)$$

The over-current limit is set by the external resistor, R_{OCSET}, as defined in (7), where I_{LIMIT} is the required over current limit. I_{OCSET}, the bias current of OCSET pin, changes with switching frequency set by resistor R_{OSC} and is determined by equation (9). G_{CS} is the gain of the current sense amplifier. In a multiphase architecture the peak to peak ripple of the net inductor current is much smaller than the stand alone phase due to interleaving. The ratio of the peak to average current in this case can be approximated using (8).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS} / I_{OCSET} \quad (7)$$

$$K_P = \frac{\left[V_I \cdot D \cdot (1-D) \cdot n \cdot (D - \frac{m}{n}) \cdot (\frac{m+1}{n} - D)\right]}{(I_{LIMIT}/n) \cdot L \cdot f_{sw} \cdot 2 \cdot D \cdot (1-D)} \quad (8)$$

$$Iocset = \frac{600}{Rosc(K\Omega)} \quad (9)$$

Where

I_{LIMIT}=Maximum over current limit
n=Number of phases
K_P=Ratio of the peak to average current for the inductor
G_{CS}=Gain of the current sense amplifier
I_{OCSET}= Determined by the ROSC and given (9)
D=Vo/V_I
m=Maximum integer that doesn't exceed (n*D)

Vout Programming Resistor *RFB1* and *RFB3*

The Feedback pin (FB) is connected to an external resistor divider to set the output voltage. The error amplifier has a 0.8 V reference (Typical) and the output voltage is determined by selecting resistor divider values (See Figure 1).

$$R_{FB3} = \frac{R_{FB1} * 0.8}{Vout - 0.8} \quad (10)$$

VCCL Programming Resistor *RVCCLFB1* and *RVCCLFB2*

Since VCCL voltage is proportional to the MOSFET gate driver loss and inversely proportional to the MOSFET conduction loss, the optimum voltage should be chosen to maximize the converter efficiency. VCCL linear regulator consists of an external NPN transistor, a ceramic capacitor and a programmable resistor divider. Pre-select RVCCLFB1, and calculate RVCCLFB2 from (11).

$$R_{VCCLFB2} = \frac{R_{VCCLFB1} * 1.19}{VCCL - 1.19} \quad (11)$$

VCCL Capacitor *CVCCL*

The capacitor is selected based on the stability requirement of the linear regulator and the load current to be driven. The linear regulator supplies the bias and gate drive current of the phase ICs. A 4.7uF normally ensures stable VCCL performance for most applications.

VCCL Regulator Drive Resistor *RVCCLDRV*

The drive resistor is primarily dependent on the load current requirement of the linear regulator and the minimum input voltage requirements. The following equation gives an estimate of the average load current of the switching phase ICs.

$$I_{drive\_avg} = (Q_{gb} + Q_{gt}) \cdot n + I_{VCCL\_PHS} \cdot (n-1) + I_{VCCL\_C} \quad (12)$$

Q_{gb} and Q_{gt} are the gate charge of the top and bottom FET, I_{VCCL_PHS} is the VCCL current of the phase IC-s, I_{VCCL_C} is the VCCL current of the controller and n is the number of phases. For a minimum input voltage and a maximum VCCL, the maximum $R_{VCCLDRV}$ required to use the full pull-down current of the VCCL driver is given by

$$R_{VCCLDRV} = \frac{V_I(\min) - 0.7 - VCCL(\max)}{I_{drive\_avg} / \beta_{\min}} \quad (13)$$

Due to limited pull down capability of the VCCLDRV pin, make sure the following condition is satisfied.

$$\frac{V_I(\max) - 0.7 - VCCL(\min)}{R_{VCCLDRV}} < 10mA \quad (14)$$

In the above equation, V_I(min) and V_I(max) is the minimum and maximum anticipated input voltage. If the above condition is not satisfied there is a need to use a device with higher β_{min} or Darlington configuration can be used instead of a single NPN transistor.

Inductor Current Sensing Capacitor *CCS* and Resistor *RCS*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor RCS and capacitor CCS in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor CCS represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affects the current signal ISHARE.

Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor CCS and calculate RCS as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}} \quad (15)$$

Bootstrap Capacitor *CBST*

Depending on the duty cycle and gate drive current of the phase IC, a capacitor in the range of 0.1uF to 1uF is needed for the bootstrap circuit.

Decoupling Capacitors for Phase IC

0.1uF-1uF decoupling capacitors are required at VCC and VCCL pins of phase ICs.

Over-voltage Resistors *ROV1* and *ROV2*

The over-voltage resistors are used to set the voltage at the OVSNS pin. If the voltage of the OVSNS pin exceeds VREF by 85mV then the over-voltage protection will be activated and the error amplifier voltage will be pulled down turning the converter off. The over-voltage fault is latched, which means that the power to the converter has to be recycled for the fault to clear. Choose VOVSNS a certain value ΔV below VREF. VREF is typically 0.8 V. The over-voltage threshold will then be ΔV+85mV. Select *ROV1. ROV2* is calculated based on (16).

$$R_{OV2} = \frac{VOVSNS * R_{OV1}}{V_{OUT} - VOVSNS} \quad (16)$$

VREF Slew Rate Programming Capacitor *CVREF* and Resistor *RVREF*

The slew rate of MARGIN down-slope can be programmed by the external capacitor CVREF as defined in (17), where ISINK is the sink current of the VREF pin. The slew rate of MARGIN up-slope is the same as that of down-slope. The resistor RVREF is used to compensate the VREF circuit and can be calculated as shown in (18).

$$C_{VREF} = \frac{I_{SINK}}{SR_{MARGIN}} = \frac{132 * 10^{-6}}{SR_{MARGIN}} \quad (17)$$

$$R_{VREF} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VREF}^{\ 2}} \quad (18)$$

Type III Compensation

Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase, the desired phase margin θc and Rfb1 (see Figure 17). Determine the component values based on the equations below. wc is 2*π*fc (the crossover angular frequency), Le is the equivalent inductance of the converter, C is the output capacitance, Rst is the total equivalent resistance in series with the inductor, Rc is the output capacitance ESR and R is the load resistance.

$$Ccp = \frac{1}{K \cdot Rfb1} \quad (19)$$

$$Rcp = \frac{1}{Ccp \cdot wz1} \quad (20)$$

$$Cfb = \frac{1}{wz2 \cdot Rfb1} \quad (21)$$

$$Ccp1 = \frac{1}{wp2 \cdot Rcp} \quad (22)$$

$$Rfb2 = \frac{1}{wp1 \cdot Cfb} \tag{23}$$

where,

$$wz1 = \frac{wc}{10} \tag{24}$$

$$wz2 = wc \cdot \sqrt{\frac{1-\sin(\theta c)}{1+\sin(\theta c)}} \tag{25}$$

$$wp1 = wc \cdot \sqrt{\frac{1+\sin(\theta c)}{1-\sin(\theta c)}} \tag{26}$$

$$wp2 = 1.4 \cdot wp1 \tag{27}$$

$$K = \frac{(wc^4 \cdot t_4^2 + wc^2 \cdot t_2^2)((1-b \cdot wc^2)^2 + a^2 \cdot wc^2)(R+Rst)}{Gpwm \cdot H \cdot t_5 \cdot t_6 \cdot R} \tag{28}$$

where Gpwm is the gain of the PWM generator, H is the gain of the feedback filter and

$$a = \frac{Le + C(R \cdot Rst + R \cdot Rc + Rst \cdot Rc)}{R + Rst} \tag{29}$$

$$b = Le \cdot C \frac{R + Rc}{R + Rst} \tag{30}$$

$$t_1 = 1 - \frac{wc^2}{wz1 \cdot wz2} \tag{31}$$

$$t_2 = 1 - \frac{wc^2}{wp1 \cdot wp2} \tag{32}$$

$$t_3 = \frac{1}{wz1} + \frac{1}{wz2} \tag{33}$$

$$t_4 = \frac{1}{wp1} + \frac{1}{wp2} \tag{34}$$

$$t_5 = \sqrt{(1-b \cdot wc^2 + wc^2 \cdot Rc \cdot C \cdot a)^2 + wc^2 (Rc \cdot C(1-b \cdot wc^2) - a)^2} \tag{35}$$

$$t_6 = \sqrt{wc^4 (t_2 \cdot t_3 - t_1 \cdot t_4)^2 + wc^2 (t_1 \cdot t_2 + wc^2 \cdot t_3 \cdot t_4)^2} \tag{36}$$

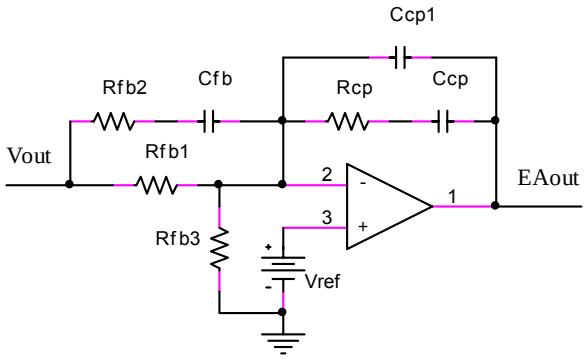
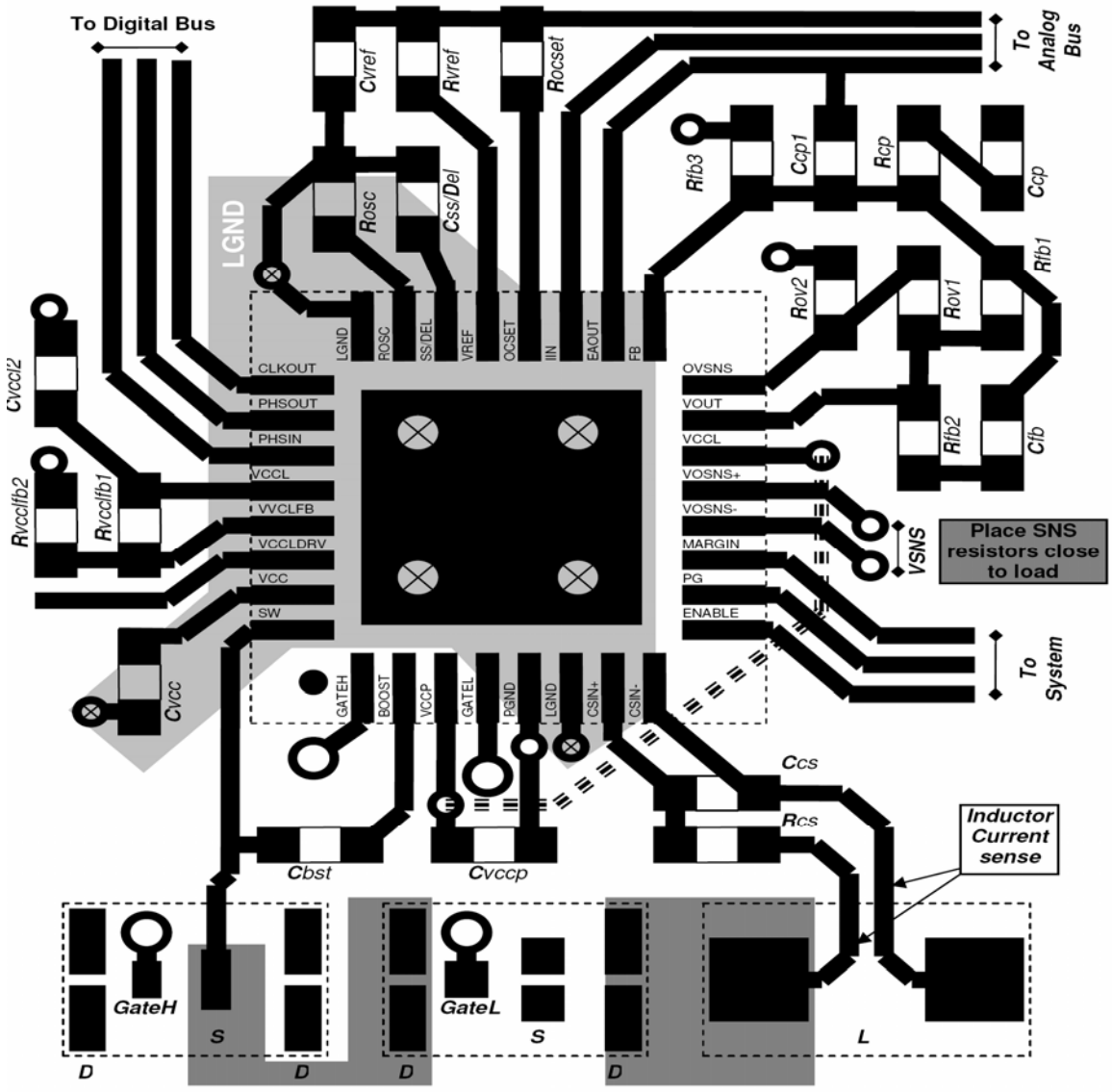


Figure 17 Voltage Loop Compensation Network

LAYOUT GUIDELINES

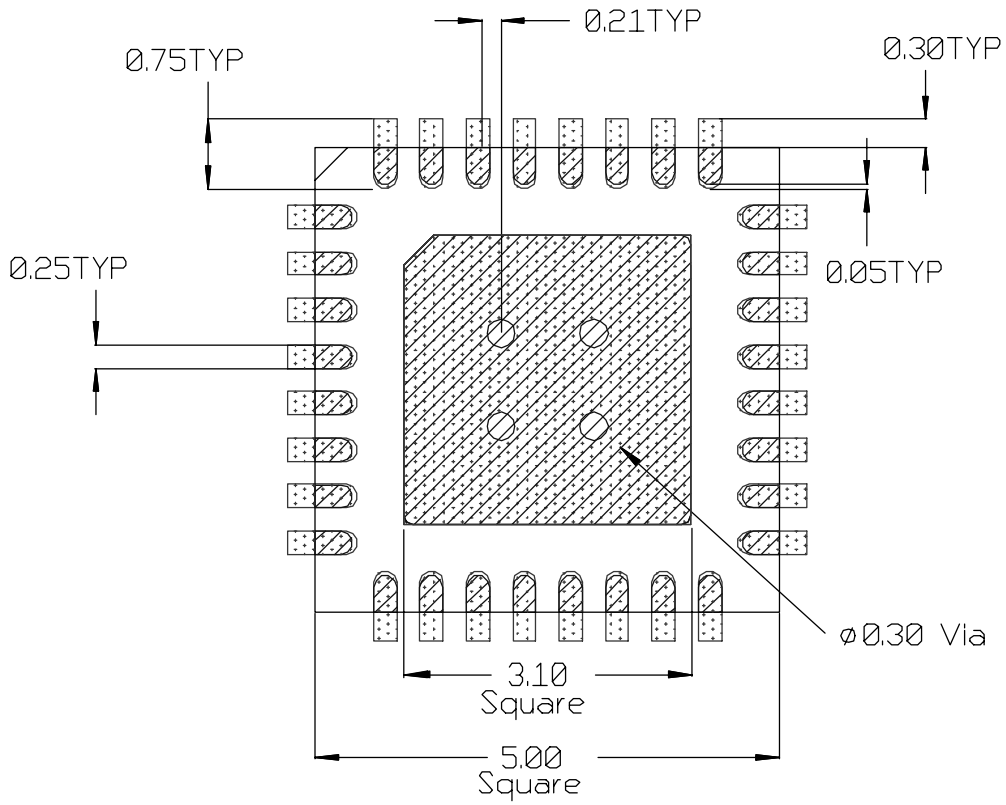
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane.
- Separate analog bus (EAIN, DACIN and ISHARE) from digital bus (CLKIN, PHSIN, and PHSOUT) to reduce the noise coupling.
- Connect PGND to LGND pins to the ground plane through vias
- Place current sense resistors and capacitors (RCS and CCS) close to IC. Use Kelvin connection for the inductor current sense wires, but separate the two wires by ground polygon. The wire from the inductor terminal to CSIN- should not cross over the fast transition nodes, i.e. switching nodes, gate drive outputs and bootstrap nodes.
- Place the IC, gate drive side as close as possible to the MOSFETs to reduce the parasitic resistance and inductance of the gate drive paths.
- Place the input ceramic capacitors close to the drain of top MOSFET and the source of bottom MOSFET.



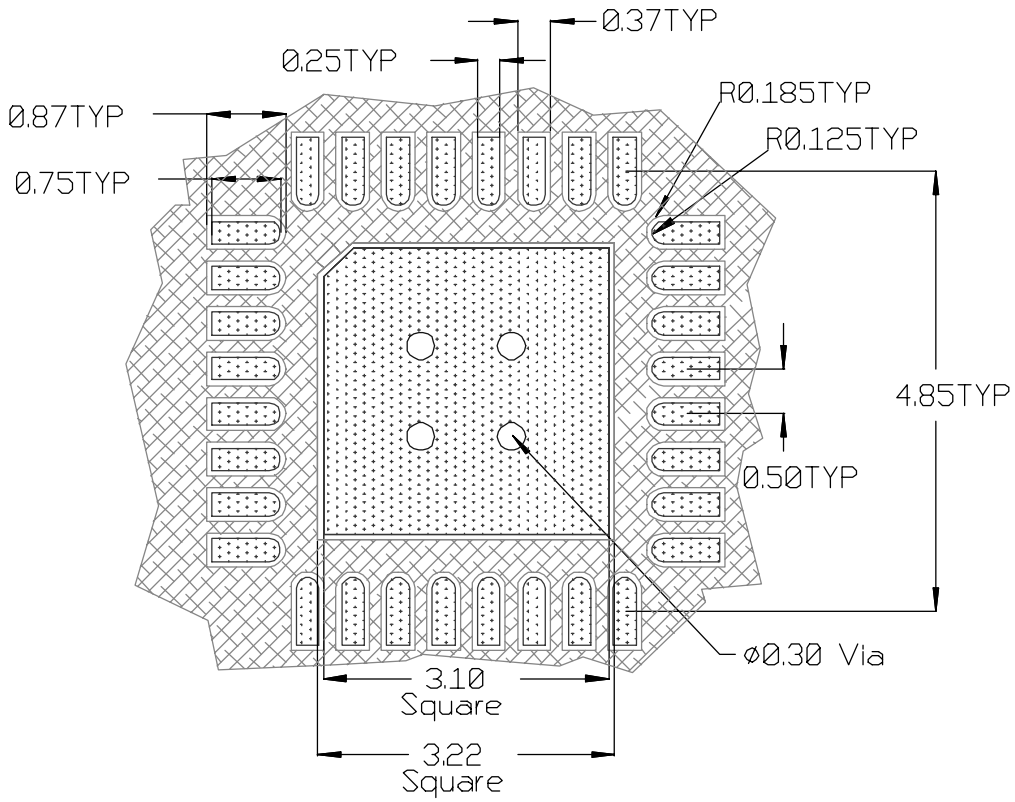
PCB Metal and Component Placement

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.30mm diameter vias shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.
- No PCB traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.



Solder Resist

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The four vias in the land pad should be tented or plugged from bottom board side with solder resist.



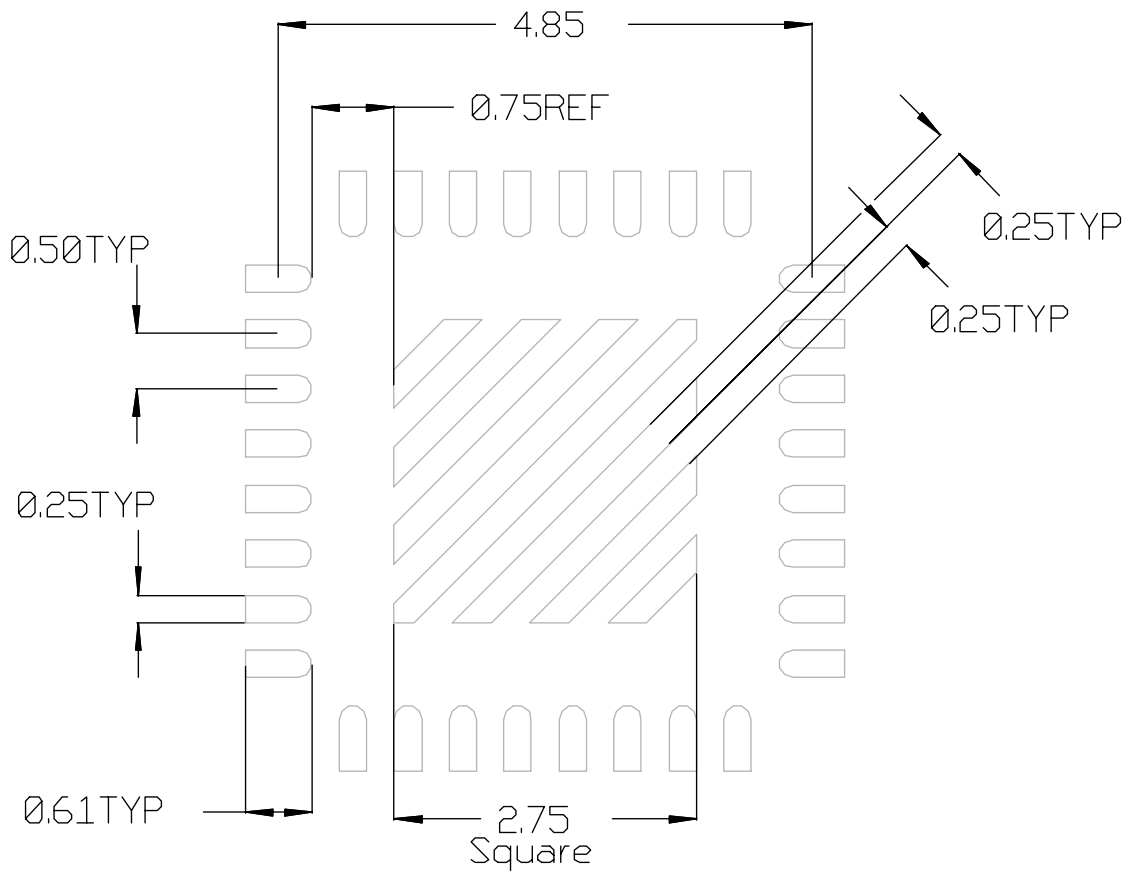
All Dimensions in mm

PCB Copper

PCB Solder Resist

Stencil Design

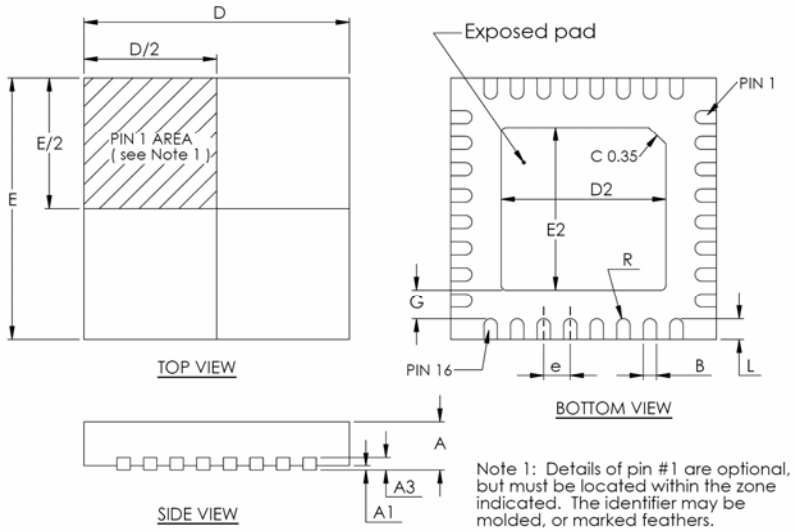
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

APPLICATIONS PACKAGE INFORMATION

32L MLPQ (5 x 5 mm Body) – θ_{JA} = 22.4 °C/W, θ_{JC} = 0.86 °C/W



32-PIN 5x5 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	4.95	5.00	5.05
D2	3.00	3.10	3.20
E	4.95	5.00	5.05
E2	3.00	3.10	3.20
e	0.5 REF		
G	0.55 REF		
L	0.30	0.40	0.50
R	0.125 TYP		

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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