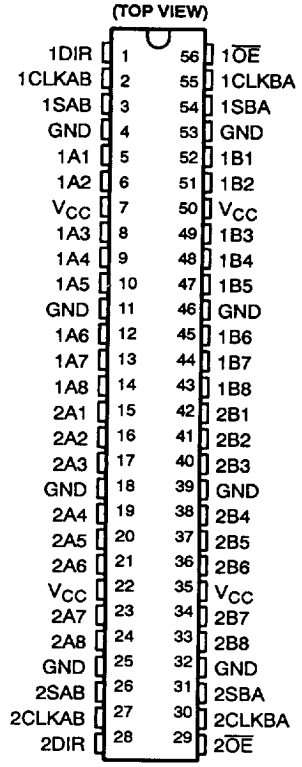
- **Members of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16646 . . . WD PACKAGE
74ACT16646 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16646 is a 16-bit bus transceiver, which consists of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock input (CLKAB or CLKBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus receives data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74AC16646 is packaged in the TI shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16646 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16646 is characterized for operation from −40°C to 85°C.

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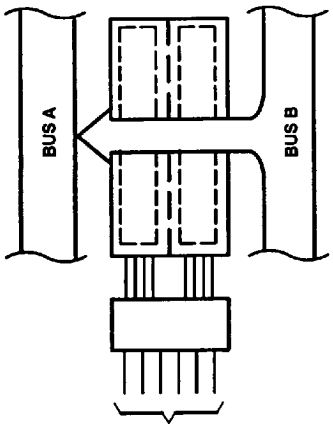
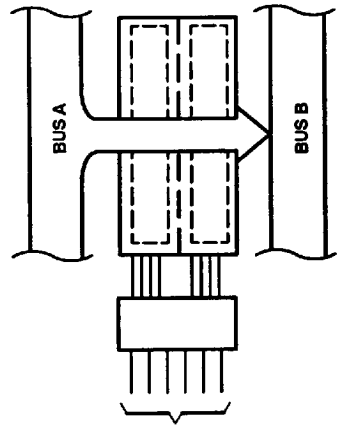


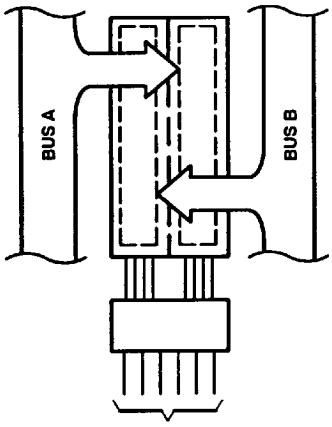
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



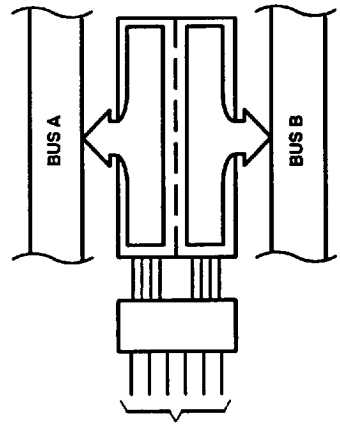
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B OR A AND B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

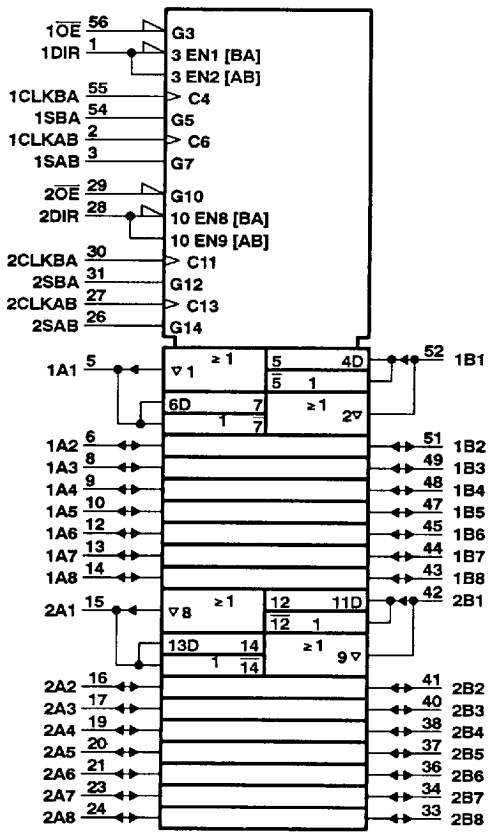
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

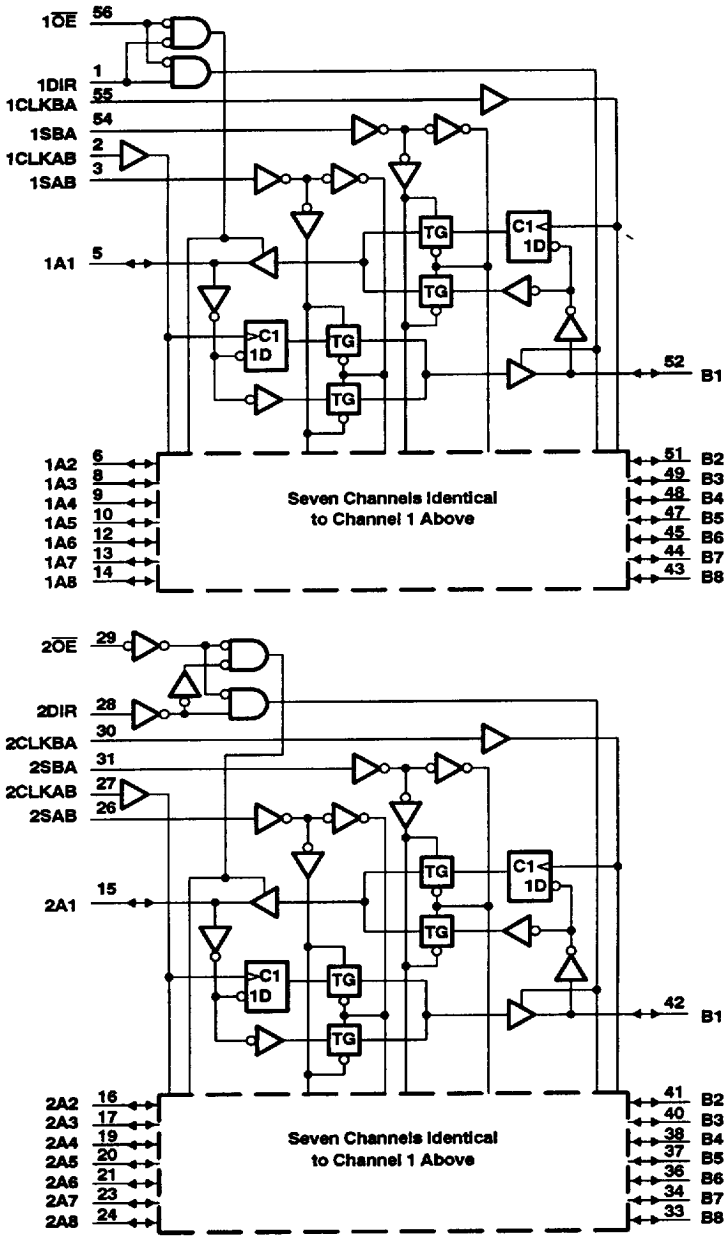
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16646			74AC16646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage				V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4			–4	mA
		V_{CC} = 4.5 V			–24			–24	
		V_{CC} = 5.5 V			–24			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16646		74AC16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_I = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_I = V_{CC}$ or GND	5 V		16						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54AC16646		74AC16646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	65	0	65	0	65	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	7				7		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	6.5				6.5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54AC16646		74AC16646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	75	0	75	0	75	MHz
t_w	Pulse duration, CLKAB or CLkBA high or low	6.5				6.5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	5				5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16646		74AC16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			65			65		65		MHz
t_{PLH}	A or B	B or A	3.4	9.3	13.2	3.4	15.7	3.4	14.8	ns
t_{PHL}			3.6	10	13.4	3.6	15.1	3.6	4.5	
t_{PZH}	$\overline{OE}$	A or B	3.8	10.5		3.8	17.6	3.8	16.4	ns
t_{PZL}			4.8	13.9		4.8	22.1	4.8	20.9	
t_{PHZ}	$\overline{OE}$	A or B	4.4	7.6		4.4	11	4.4	10.7	ns
t_{PLZ}			4	7		4	10.4	4	10.1	
t_{PLH}	CLKBA or CLKAB	A or B	4.7	12.1		4.7	19.9	4.7	18.7	ns
t_{PHL}			4.8	12.2		4.8	18.8	4.8	18	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	4.7	12		4.7	19.9	4.7	18.5	ns
t_{PHL}			4.5	11.4		4.5	17.2	4.5	16.4	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	4	10.5		4	17.3	4	16.3	ns
t_{PHL}			5.2	13.3		5.2	20.3	5.2	19.3	
t_{PZH}	DIR	A or B	3.6	10.3		3.6	17.9	3.6	16.8	ns
t_{PZL}			4.7	13.5		4.7	22.1	4.7	20.8	
t_{PHZ}	DIR	A or B	4.6	7.8		4.6	11.6	4.6	11.2	ns
t_{PLZ}			3.9	7		3.9	11	3.9	10.6	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

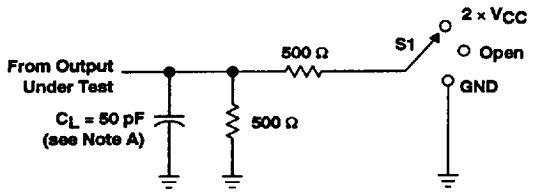
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16646		74AC16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	A or B	B or A	2.9	5.5	8.5	2.9	10.1	2.9	9.5	ns
t_{PHL}			2.9	5.7	8.9	2.9	10.1	2.9	9.7	
t_{PZH}	$\overline{OE}$	A or B	3.1	6.1	9.4	3.1	11.1	3.1	10.5	ns
t_{PZL}			4.1	7.3	11	4.1	12.9	4.1	12.2	
t_{PHZ}	$\overline{OE}$	A or B	4	6.1	8.4	4	9.1	4	8.9	ns
t_{PLZ}			3.8	5.7	8	3.8	8.9	3.8	8.6	
t_{PLH}	CLKBA or CLKAB	A or B	3.9	7	10.8	3.9	12.8	3.9	12.1	ns
t_{PHL}			3.9	7.1	10.8	3.9	12.5	3.9	11.9	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	4	7.4	11.1	4	13.4	4	12.5	ns
t_{PHL}			3.6	6.7	10.2	3.6	11.8	3.6	11.2	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	3.3	6.1	9.5	3.3	11.2	3.3	10.6	ns
t_{PHL}			4.3	8	11.7	4.3	13.9	4.3	13.1	
t_{PZH}	DIR	A or B	3	5.9	9.6	3	11.6	3	10.9	ns
t_{PZL}			3.6	7	11.1	3.6	12.9	3.6	12.2	
t_{PHZ}	DIR	A or B	4	6.2	8.8	4	9.6	3	9.4	ns
t_{PLZ}			3.7	5.7	8.2	3.7	9	3.7	8.8	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

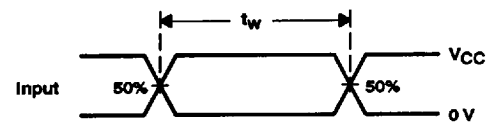
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	62	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

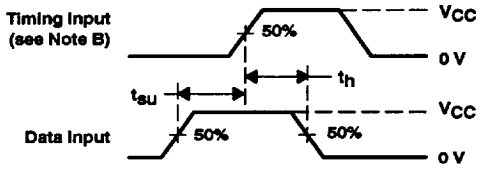


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



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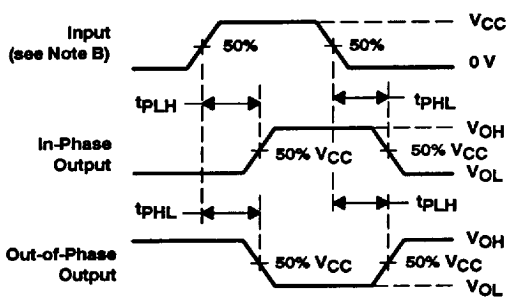
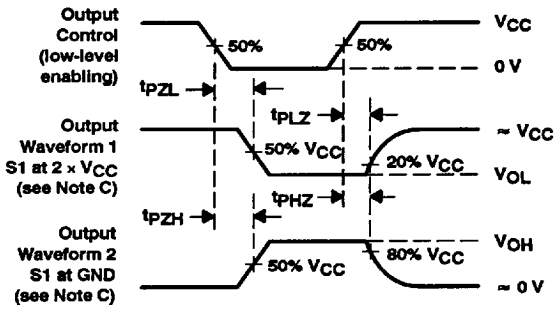


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms