

8-Mbit (512 K × 16) Static RAM

Features

■ High Speed: 45 ns

■ Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V

■ Ultra Low Standby Power

Typical standby current: 2 μA

Maximum standby current: 8 μA

■ Ultra Low Active Power

□ Typical active current: 1.8 mA at f = 1 MHz

■ Easy Memory Expansion with \overline{CE}_1 , CE_2 , and \overline{OE} Features

■ Automatic Power Down when Deselected

■ CMOS for Optimum Speed and Power

 Available in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) packages

Functional Description

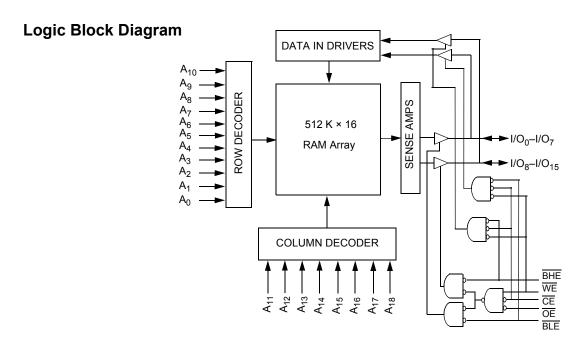
The CY62156ESL is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable

applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device in standby mode when deselected (CE $_1$ HIGH or CE $_2$ LOW). The input or output pins (I/O $_0$ through I/O $_{15}$) are placed in a high impedance state when the device is deselected (CE $_1$ HIGH or CE $_2$ LOW), the outputs are disabled (OE $_1$ HIGH), Byte High Enable and Byte Low Enable are disabled (BHE, BLE $_1$ HIGH), or a write operation is active (CE $_1$ LOW, CE $_2$ HIGH and WE LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 <u>HIGH</u>) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O $_0$ through I/O $_7$) is written into the location specified on the address pins (A_0 through A $_18$). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O $_8$ through I/O $_15$) is written into the location specified on the address pins (A_0 through A $_18$).

To read from the device, take Chip Enable ($\overline{\text{CE}}_1$ LOW and CE₂ HIGH) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.







Contents

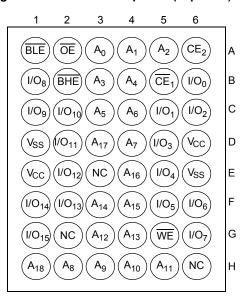
Pin Configurations	3
Product Portfolio	
Maximum Ratings	
Operating Range	
Electrical Characteristics	
Capacitance	
Thermal Resistance	
AC Test Loads and Waveforms	5
Data Retention Characteristics	6
Data Retention Waveform	
Switching Characteristics	
Switching Waveforms	
Truth Table	

Ordering information	12
Ordering Code Definitions	12
Package Diagrams	
Acronyms	14
Document Conventions	14
Units of Measure	14
Document History Page	15
Sales, Solutions, and Legal Information	16
Worldwide Sales and Design Support	16
Products	16
PSoC® Solutions	16
Cypress Developer Community	16
Technical Support	16



Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [1]



Product Portfolio

Ī					Power Dissipation					
	Product	Range	V _{CC} Range (V) [2] Speed Operating I _{CC} , (mA) St		Operating I _{CC} , (mA)		Standb	y, I _{SB2}		
	Floudet	ixalige	ACC Isaude (A)	(ns)	f = 1MHz		$f = 1MHz$ $f = f_{max}$		_ Standby, I _{SB2} (μ A)	
					Typ ^[3]	Max	Typ [3]	Max	Typ [3]	Max
ĺ	CY62156ESL	Industrial	2.2 V to 3.6 V and 4.5 V to 5.5 V	45	1.8	3	18	25	2	8

- NC pins are not connected on the die.
 Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature-65 °C to + 150°C Ambient Temperature with Supply Voltage to Ground Potential-0.5 V to 6.0 V DC Voltage Applied to Outputs in High Z State $^{[4,\ 5]}$ -0.5 V to 6.0 V DC Input Voltage [4, 5]-0.5 V to 6.0 V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2,001V
Latch Up Current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V cc ^[6]
CY62156ESL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V, and 4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

D	Dona suite 4 i a sa	To at One			11!4		
Parameter	Description	lest Cor	Test Conditions			Max	Unit
V _{OH}	Output HIGH Voltage	2.2 ≤ V _{CC} ≤ 2.7	$I_{OH} = -0.1 \text{ mA}$	2.0	_	_	V
		2.7 ≤ V _{CC} ≤ 3.6	$I_{OH} = -1.0 \text{ mA}$	2.4	_	-	
		4.5 ≤ V _{CC} ≤ 5.5	$I_{OH} = -1.0 \text{ mA}$	2.4	_	-	
V _{OL}	Output LOW Voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA	-	_	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1mA	-	_	0.4	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OL} = 2.1mA	-	_	0.4	
V _{IH}	Input HIGH Voltage	2.2 ≤ V _{CC} ≤ 2.7		1.8	_	V _{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	_	V _{CC} + 0.3	
		4.5 ≤ V _{CC} ≤ 5.5		2.2	_	V _{CC} + 0.5	
V _{IL}	Input LOW Voltage	2.2 ≤ V _{CC} ≤ 2.7	-0.3	_	0.6	V	
		$2.7 \le V_{CC} \le 3.6$		-0.3	_	0.8	
		$4.5 \le V_{CC} \le 5.5$		-0.5	_	0.8	
I _{IX}	Input Leakage Current	$GND \le V_1 \le V_{CC}$		-1	_	+1	μΑ
I _{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}, C$	Output Disabled	-1	_	+1	μΑ
I _{CC}	V _{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$	-	18	25	mA
		f = 1 MHz	I _{OUT} = 0 mA, CMOS levels	_	1.8	3	
I _{SB1}	Automatic CE Power down Current – CMOS Inputs		-	2	8	μА	
I _{SB2} ^[7]	Automatic CE Power down Current – CMOS Inputs	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V}$ $\text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V}$ $\text{f} = 0, \text{V}_{\text{CC}} = \text{V}_{\text{CC}(\text{m})}$	$^{\prime}$ or $CE_2 \le 0.2 \text{ V}$, or $V_{\text{IN}} \le 0.2 \text{ V}$, hax)	-	2	8	μА

- 4. V_{IL}(min) = -2.0 V for pulse durations less than 20 ns.
 5. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 6. Full Device AC ope<u>ration</u> assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
 7. Only chip enables (CE₁ and CE₂) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.



Capacitance

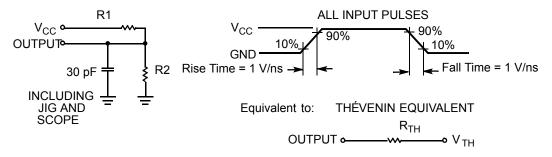
Parameter [8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)		8.86	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.20	1.75	1.77	V

Note

^{8.} Tested initially and after any design or process changes that may affect these parameters.



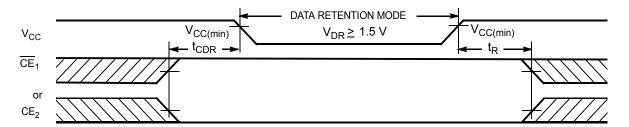
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	T yp ^[9]	Max	Unit
V_{DR}	V _{CC} for Data Retention		1.5	-	-	V
I _{CCDR} [10]	Data Retention Current	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V}, \ \text{CE}_2 \le 0.2 \text{ V}, \ \text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V or V}_{\text{IN}} \le 0.2 \text{ V}, \ \text{V}_{\text{CC}} = 1.5 \text{ V}$	_	2	5	μА
t _{CDR} [11]	Chip Deselect to Data Retention Time		0	_	_	ns
t _R [12]	Operation Recovery Time		45	_	_	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



^{9.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C. 10. Only chip enables (CE₁ and CE₂) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating. 11. Tested initially and after any design or process changes that may affect these parameters.

^{12.} Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \ge 100~\mu s$ or stable at $V_{CC(min)} \ge 100~\mu s$.



Switching Characteristics

Over the Operating Range

Parameter [13]	Decembries	45	ns	11!4		
Parameter	Description	Min	Max	Unit		
Read Cycle						
t _{RC}	Read Cycle Time	45	_	ns		
t _{AA}	Address to Data Valid	-	45	ns		
t _{OHA}	Data Hold from Address Change	10	_	ns		
t _{ACE}	CE ₁ LOW and CE ₂ HIGH to Data Valid	-	45	ns		
t _{DOE}	OE LOW to Data Valid	-	22	ns		
t _{LZOE}	OE LOW to Low Z ^[14]	5	-	ns		
t _{HZOE}	OE HIGH to High Z ^[14, 15]	_	18	ns		
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to Low Z ^[14]	10	_	ns		
t _{HZCE}	CE ₁ HIGH and CE ₂ LOW to High Z ^[14, 15]	_	18	ns		
t _{PU}	CE ₁ LOW and CE ₂ HIGH to Power Up	0	_	ns		
t _{PD}	CE ₁ HIGH and CE ₂ LOW to Power Down	_	45	ns		
t _{DBE}	BLE/BHE LOW to Data Valid	_	22	ns		
t _{LZBE}	BLE/BHE LOW to Low Z ^[14]	5	_	ns		
t _{HZBE}	BLE/BHE HIGH to High Z ^[14, 15]	_	18	ns		
Write Cycle ^{[16,}	17]					
t _{WC}	Write Cycle Time	45	_	ns		
t _{SCE}	CE ₁ LOW and CE ₂ HIGH to Write End	35	_	ns		
t _{AW}	Address Setup to Write End	35	_	ns		
t _{HA}	Address Hold from Write End	0	_	ns		
t _{SA}	Address Setup to Write Start	0	_	ns		
t _{PWE}	WE Pulse Width	35	_	ns		
t _{BW}	BLE/BHE LOW to Write End	35	_	ns		
t _{SD}	Data Setup to Write End	25	_	ns		
t _{HD}	Data Hold from Write End	0	_	ns		
t _{HZWE}	WE LOW to High Z ^[14, 15]	-	18	ns		
t _{LZWE}	WE HIGH to Low Z ^[14]	10	_	ns		

^{13.} Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.

14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZDE}, and t_{HZWE} is less than t_{LZWE} for any device.

^{15.} t_{HZOE}, t_{HZOE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.

16. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, BHE, BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

^{17.} The minimum write cycle pulse width for Write Cycle No. 3 (WE controlled, OE LOW) should be equal to the sum of tsp and thzwe.



Switching Waveforms

Figure 4. Read Cycle No. 1: Address Transition Controlled [18, 19]

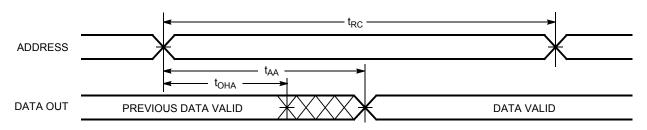
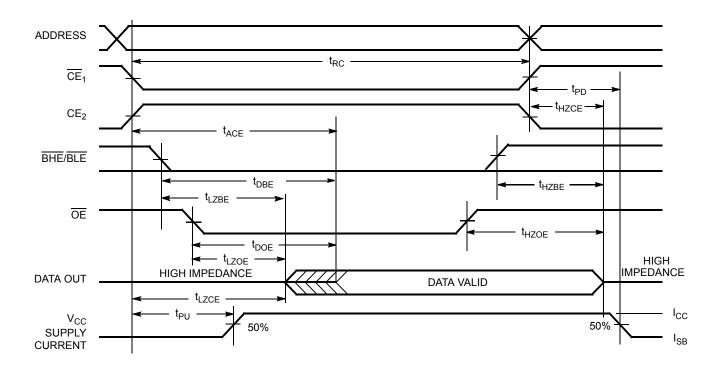


Figure 5. Read Cycle No. 2: OE Controlled [19, 20]



^{18.} The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} , and $\overline{CE}_2 = V_{IH}$.

^{19.} WE is HIGH for read cycle.

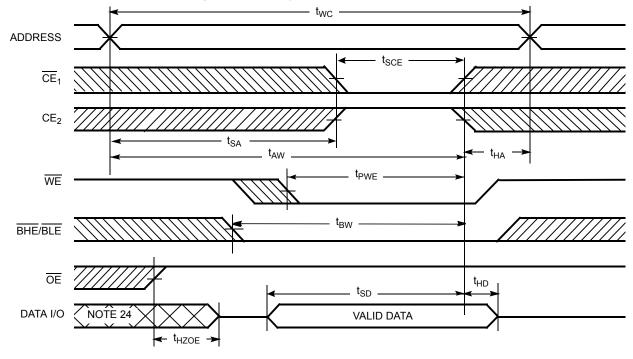
^{20.} Address valid before or similar to $\overline{\text{CE}}_1$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW and $\overline{\text{CE}}_2$ transition HIGH.



Switching Waveforms (continued)

Figure 6. Write Cycle No 1: $\overline{\text{WE}}$ Controlled [21, 22, 23] - t_{WC} **ADDRESS** t_{SCE} CE₁ CE_2 t_{AW} t_{HA} $\mathsf{t}_{\mathsf{PWE}}$ WE t_{BW} BHE/BLE ΘE t_{HD} t_{SD} NOTE 24 DATA I/O VALID DATA

Figure 7. Write Cycle 2: $\overline{\text{CE}}$ Controlled [21, 22, 23]



- 21. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, BHE, BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 22. Data I/O is high impedance if $\overline{\text{OE}} = \text{V}_{\text{IH}}$.

 23. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = \text{V}_{\text{IH}}$, the output remains in a high impedance state.

 24. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 8. Write Cycle 3: $\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW $^{[25,\ 27]}$

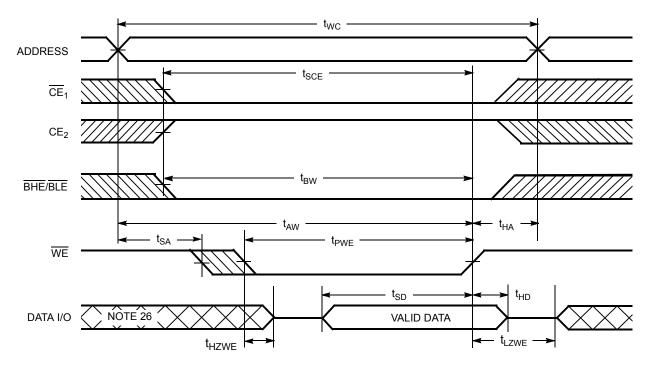
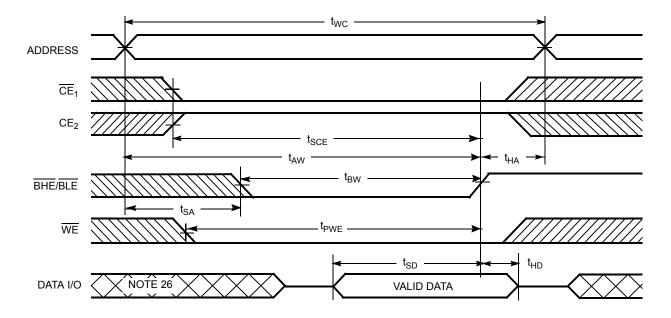


Figure 9. Write Cycle 4: BHE/BLE Controlled, OE LOW [25]



- 25. If $\overline{\text{CE}}_1$ goes HIGH and $\overline{\text{CE}}_2$ goes LOW simultaneously with $\overline{\text{WE}} = V_{\text{IH}}$, the output remains in a high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.
- 27. The minimum write cycle pulse width should be equal to the sum of tsD and tHZWE.



Truth Table

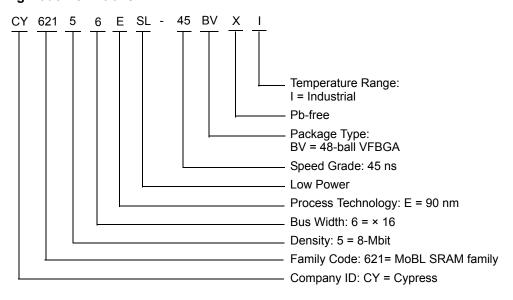
CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	Х	Х	Х	High Z	Deselect/Power Down	Standby (I _{SB})
Х	L	Х	Х	Х	Х	High Z	Deselect/Power Down	Standby (I _{SB})
L	Н	Х	Χ	Н	Н	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	L	Н	L	Data Out (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	L	L	Н	High Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	Н	L	Н	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	Н	Н	L	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	Н	L	L	High Z	Output Disabled	Active (I _{CC})
L	Н	L	Χ	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	Н	L	Data In (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	L	Н	High Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})



Ordering Information

Speed (ns)	Ordering Code	Package Diagram		Operating Range
45	CY62156ESL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

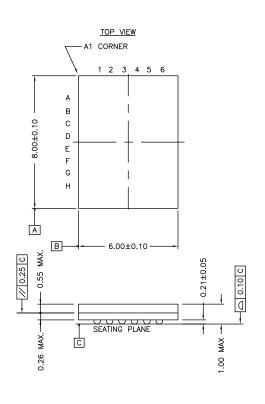
Ordering Code Definitions

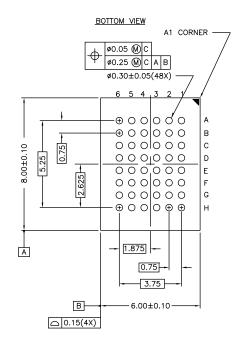




Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150





NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H



Acronyms

Acronym	Description				
CE	Chip Enable				
CMOS	Complementary Metal Oxide Semiconductor				
I/O	Input/Output				
ŌĒ	Output Enable				
RAM	Random Access Memory				
SRAM	Static Random Access Memory				
VFBGA	Very Fine-Pitch Ball Grid Array				
WE	Write Enable				

Document Conventions

Units of Measure

Symbol	Unit of Measure				
°C	degree Celsius				
MHz	megahertz				
μA	microampere				
μs	microsecond				
mA	milliampere				
mm	millimeter				
ns	nanosecond				
Ω	ohm				
%	percent				
pF	picofarad				
V	volt				
W	watt				



Document History Page

Document Title: CY62156ESL MoBL [®] , 8-Mbit (512 K × 16) Static RAM Document Number: 001-54995						
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change		
**	2751673	VKN	08/13/09	New data sheet.		
*A	2899866	AJU	03/26/10	Removed inactive parts from Ordering Information. Updated Package Diagram.		
*B	3109032	AJU	12/13/2010	Obsolete document.		
*C	3903222	AJU	02/19/2013	Changed from Obsolete to Active. Removed all references of TSOP packages across the document and added 48-ball VFBGA package related information in the corresponding places. Updated Features. Updated Functional Description. Updated Logic Block Diagram. Updated Ordering Information (Updated part numbers) and added Ordering Code Definitions. Updated Package Diagrams: Removed spec 51-85087 and spec 51-85183. Added spec 51-85150. Added Acronyms and Units of Measure. Updated in new template.		
*D	3996550	MEMJ	05/13/2013	Changed status from Preliminary to Final.		
*E	4273754	VINI	02/06/2014	Updated in new template. Completing Sunset Review.		
*F	4571885	VINI	11/17/2014	Added related documentation hyperlink in page 1. Added Note 17 in Switching Characteristics. Added note reference 17 in the Switching Characteristics table. Added Note 27 in Switching Waveforms. Added note reference 27 in Figure 8.		



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive Clocks & Buffers Interface

Lighting & Power Control

Memory PSoC Touch Sensing USB Controllers Wireless/RF cypress.com/go/automotive cypress.com/go/clocks cypress.com/go/interface cypress.com/go/powerpsoc cypress.com/go/plc cypress.com/go/memory cypress.com/go/psoc cypress.com/go/touch cypress.com/go/USB cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2009-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document Number: 001-54995 Rev. *F

Revised November 28, 2014