

EB52F4D20CV-8.192M

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REGULATORY COMPLIANCE (Data Sheet downloaded on Oct 23, 2016)



ITEM DESCRIPTION

Temperature Compensated Quartz Crystal Clock Oscillators TCXO LVCMOS (CMOS) 3.3Vdc 14-Pin DIP Metal Thru-Hole 8.192MHz ± 2.5 ppm Maximum ± 2.0 ppm Maximum -20°C to +70°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	8.192MHz
Initial Tolerance	± 2.5 ppm Maximum (Measured at Nominal Vdd and Vc)
Frequency Stability	± 2.0 ppm Maximum
Frequency Stability vs. Input Voltage	± 0.3 ppm Maximum (Vdd $\pm 5\%$)
Frequency Stability vs. Load	± 0.2 ppm Maximum ($\pm 10\%$)
Frequency Stability vs. Aging	± 1 ppm/Year Maximum (at 25°C)
Operating Temperature Range	-20°C to +70°C
Supply Voltage	3.3Vdc $\pm 5\%$
Input Current	15mA Maximum (Measured at Steady State at 25°C)
Output Voltage Logic High (Voh)	90% of Vdd Minimum
Output Voltage Logic Low (Vol)	10% of Vdd Maximum
Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50 ± 5 (%) (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Control Voltage	1.65Vdc ± 1.35 Vdc
Control Voltage Range	0.0Vdc to Vdd
Frequency Deviation	± 7 ppm Minimum, ± 20 ppm Maximum (Referenced to Fo at Vc=1.65Vdc; Vdd=3.3Vdc)
Linearity	$\pm 10\%$ Maximum
Transfer Function	Positive Transfer Characteristic
Input Impedance	10kOhms Typical
Phase Noise	-70dBc/Hz at 10Hz Offset -100dBc/Hz at 100Hz Offset -130dBc/Hz at 1kHz Offset -140dBc/Hz at 10kHz Offset -145dBc/Hz at 100kHz Offset (Typical Values at 19.440MHz)
Storage Temperature Range	-55°C to +125°C

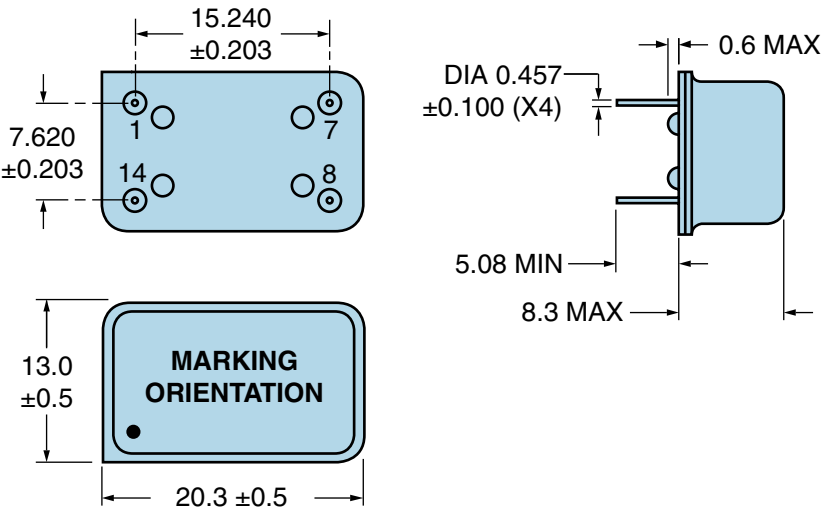
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A
Gross Leak Test	MIL-STD-883, Method 1014 Condition C
Lead Integrity	MIL-STD-883, Method 2004
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)



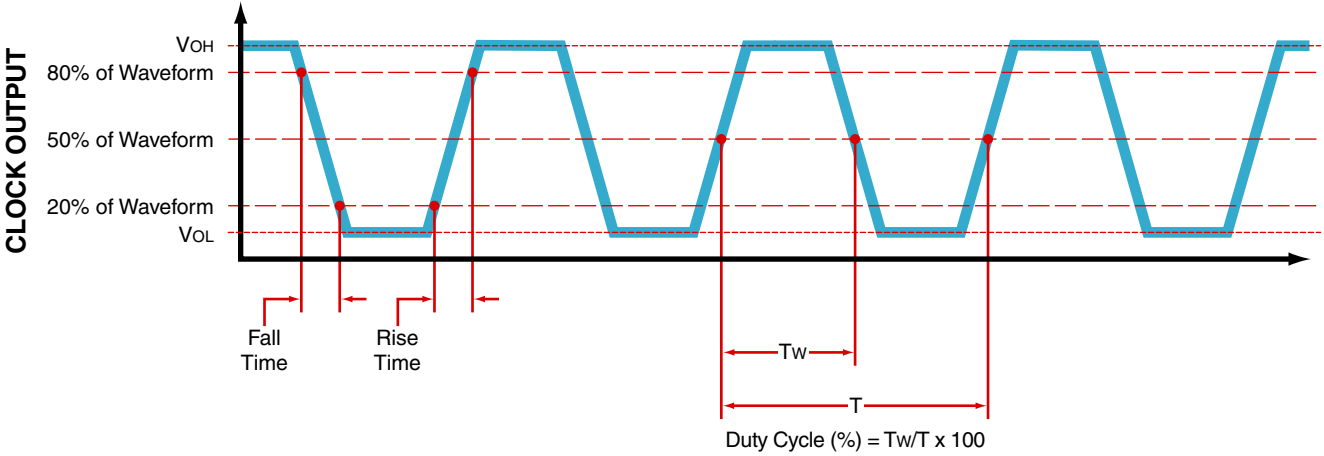
PIN	CONNECTION
1	Voltage Control
7	Case Ground
8	Output
14	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	8.1920M
3	XXXXXX XXXXXX=Ecliptek Manufacturing Identifier

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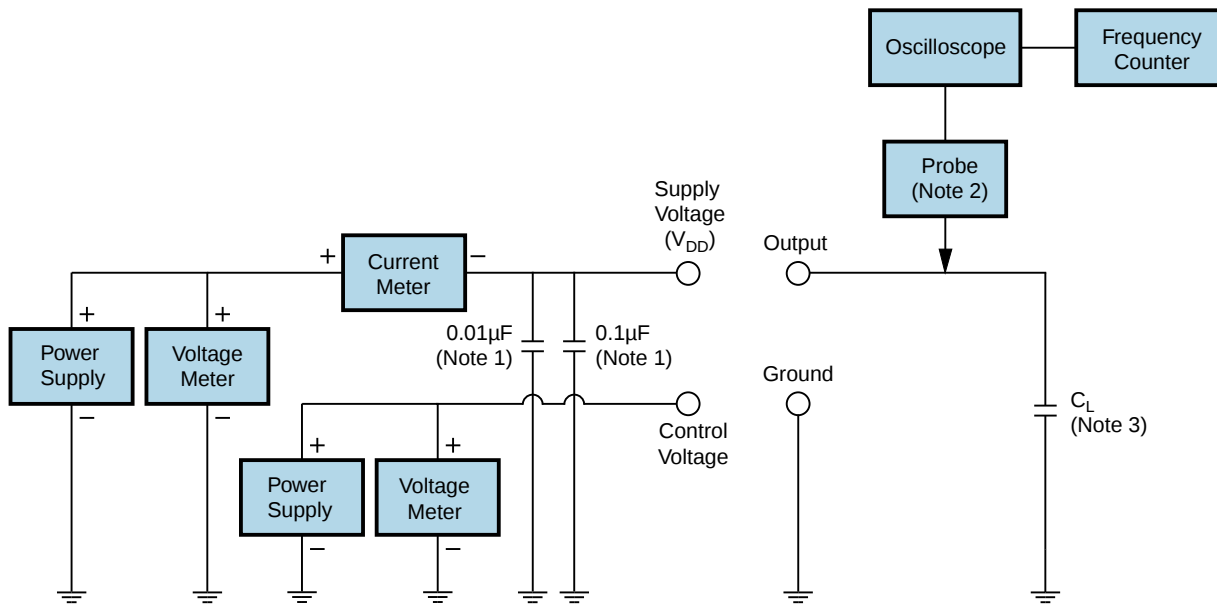
OUTPUT WAVEFORM



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Test Circuit for Voltage Control Option



Note 1: An external $0.01\mu\text{F}$ ceramic bypass capacitor in parallel with a $0.1\mu\text{F}$ high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>300\text{MHz}$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

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Recommended Solder Reflow Methods



Low Temperature Solder Bath (Wave Solder)

Ts MAX to Tl (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	N/A
- Temperature Typical (Ts TYP)	150°C
- Temperature Maximum (Ts MAX)	N/A
- Time (ts MIN)	30 - 60 Seconds
Ramp-up Rate (Tl to Tp)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (Tl)	150°C
- Time (tL)	200 Seconds Maximum
Peak Temperature (Tp)	245°C Maximum
Target Peak Temperature (Tp Target)	245°C Maximum 1 Time / 235°C Maximum 2 Times
Time within 5°C of actual peak (tp)	5 Seconds Maximum 1 Time / 15 Seconds Maximum 2 Times
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum.