TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

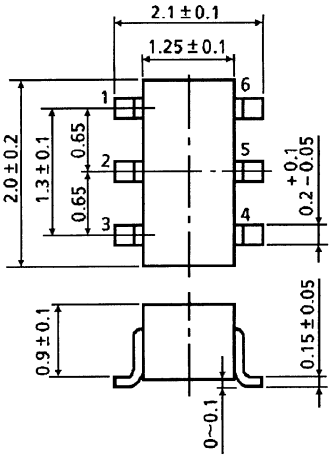
SSM6N7002FU

High Speed Switching Applications

Analog Switch Applications

- Small package
- Low ON resistance : R_{on} = 3.3 Ω (max) (@V_{GS} = 4.5 V)
  : R_{on} = 3.2 Ω (max) (@V_{GS} = 5 V)
  : R_{on} = 3.0 Ω (max) (@V_{GS} = 10 V)

Unit: mm



1.SOURCE1 4.SOURCE2
2.GATE1 5.GATE2
3.DRAIN2 6.DRAIN1

US6

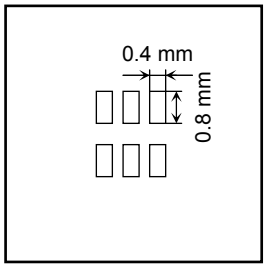
JEDEC	—
JEITA	—
TOSHIBA	2-2J1C

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

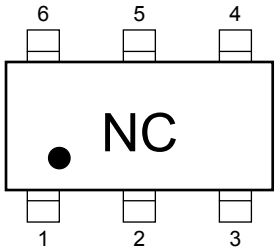
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	60	V
Gate-Source voltage		V_{GSS}	± 20	V
Drain current	DC	I_D	200	mA
	Pulse	I_{DP}	800	
Drain power dissipation (Ta = 25°C)		P_D (Note 1)	300	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

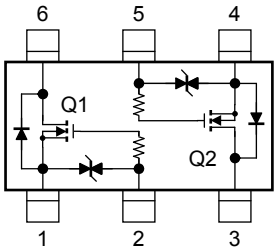
Note 1: Total rating, mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32mm^2 × 6)



Marking



Equivalent Circuit (top view)



Handling Precaution

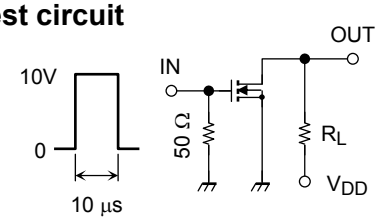
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Typ	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	—	± 10	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0	60	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 60 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 0.25 mA	1.0	—	2.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 200 mA	170	—	—	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 500 mA, V_{GS} = 10 V	—	2.0	3.0	Ω
			I_D = 100 mA, V_{GS} = 5 V	—	2.1	3.2	
			I_D = 100 mA, V_{GS} = 4.5 V	—	2.2	3.3	
Input capacitance		C_{iss}	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	—	17	—	pF
Reverse transfer capacitance		C_{rss}		—	1.4	—	pF
Output capacitance		C_{oss}		—	5.8	—	pF
Switching time	Turn-on delay time	$td_{(on)}$	V_{DD} = 30V, I_D = 200 mA, V_{GS} = 0 ~ 10V	—	2.4	4.0	ns
	Turn-off delay time	$td_{(off)}$		—	26	40	

Switching Time Test Circuit

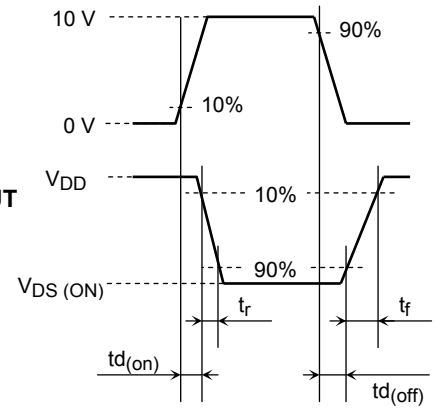
(a) Test circuit



V_{DD} = 30 V
Duty ≦ 1%
V_{IN}: t_r, t_f < 2 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}

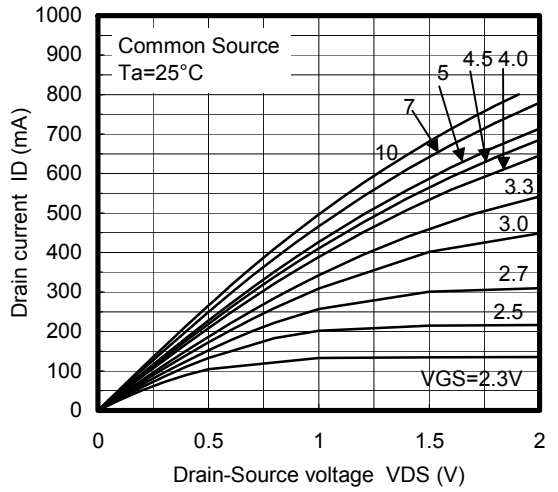


Precaution

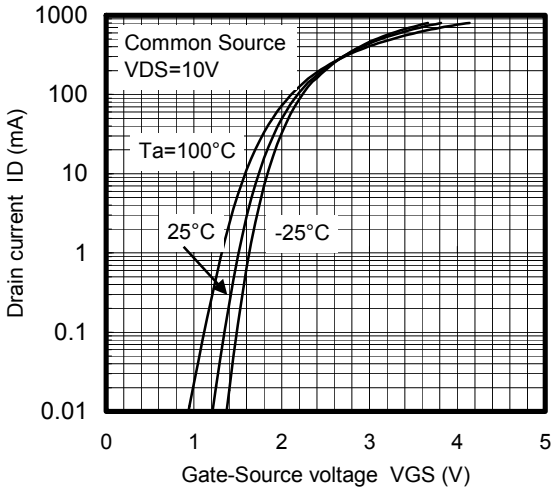
V_{th} can be expressed as voltage between gate and source when low operating current value is I_D =250 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th}. (Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

Please take this into consideration for using the device.

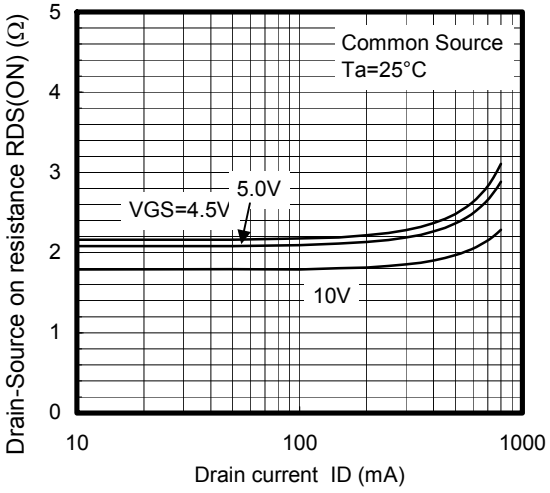
ID - VDS



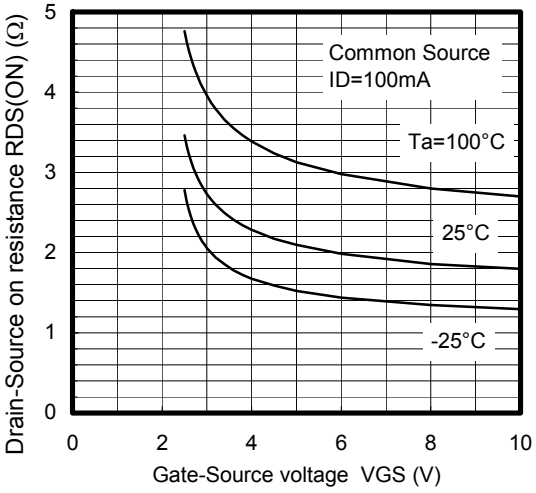
ID - VGS



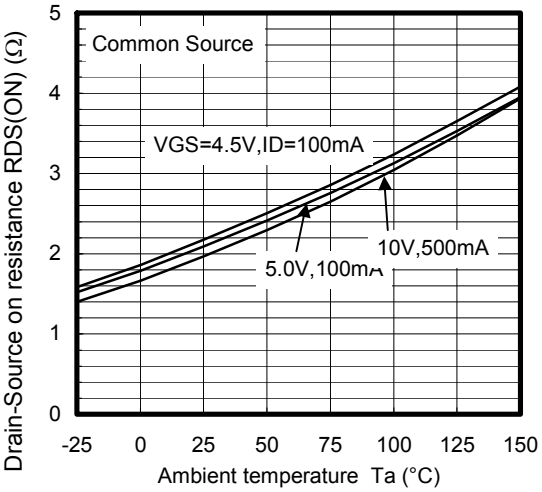
RDS(ON) - ID



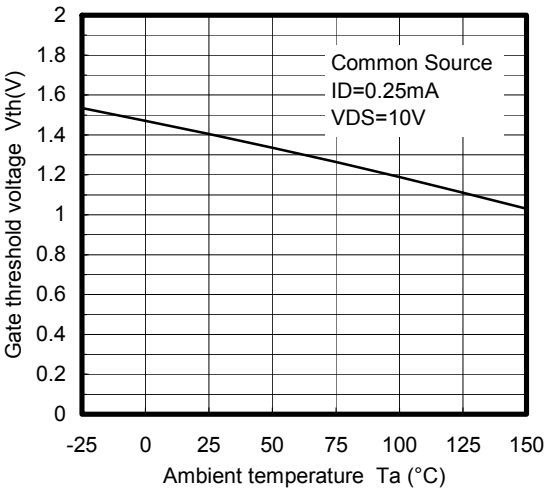
RDS(ON) - VGS



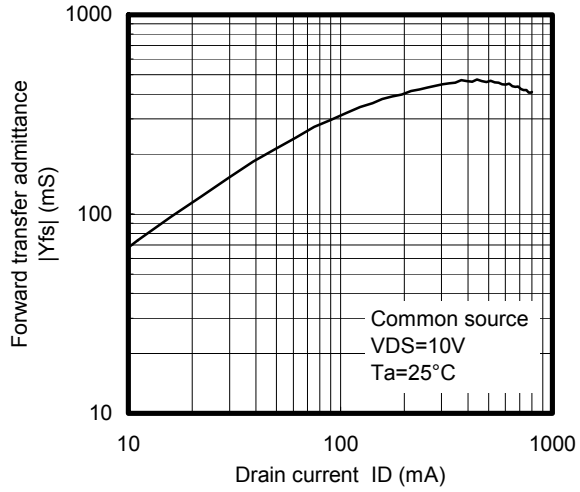
RDS(ON) - Ta



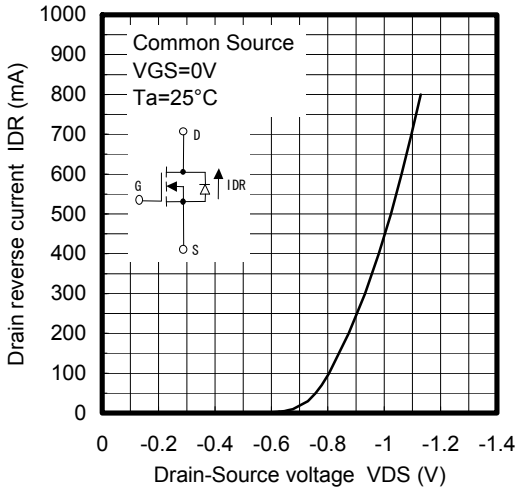
Vth - Ta



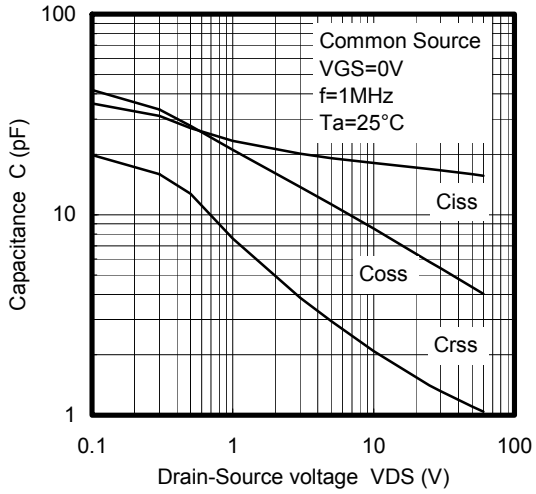
|Yfs| - ID



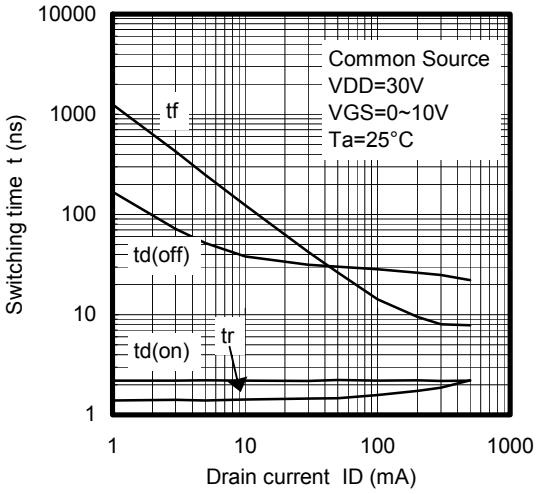
IDR - VDS



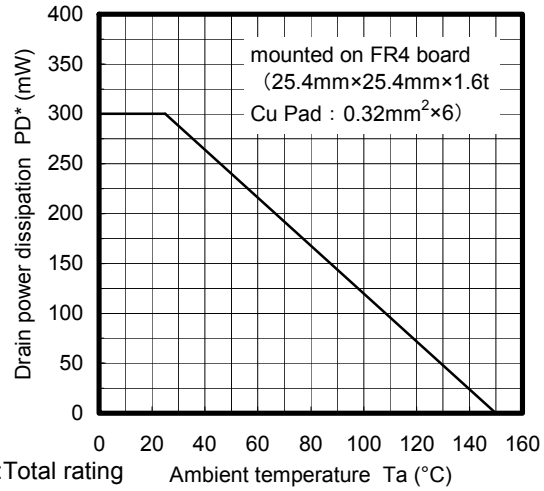
C - VDS



t - ID



PD* - Ta



* :Total rating

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