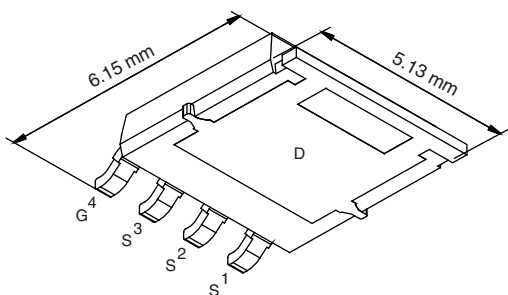


N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
40	0.0095 at $V_{GS} = 10$ V	20 ^a	16 nC
	0.0115 at $V_{GS} = 4.5$ V	20 ^a	

PowerPAK® SO-8L Single



Ordering Information: SiJ800DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

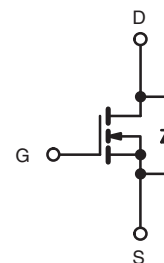
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Backlight Inverter
- High-Side Switch
- Server, VRM, POL
- DC/DC



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	80	mJ
Avalanche Current	I_{AS}	30	
Avalanche Energy	E_{AS}	45	
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	A
		$T_A = 25$ °C	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	25	30	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	2.9	3.5	

Notes:

a. Based on $T_C = 25$ °C. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 70 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 1.0 mA		44		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.9			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		3	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			5		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0078	0.0095	Ω	
		V _{GS} = 4.5 V, I _D = 15 A		0.0092	0.0115		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		70		S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		2400		pF	
Output Capacitance	C _{oss}			260			
Reverse Transfer Capacitance	C _{rss}			100			
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 20 A		37	56	nC	
Gate-Source Charge	Q _{gs}	V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 20 A		16	24		
Gate-Drain Charge	Q _{gd}			6.5			
Gate Resistance	R _g			4.5			
Turn-On Delay Time	t _{d(on)}	f = 1 MHz	1	5	10	Ω	
Rise Time	t _r		V _{DD} = 20 V, R _L = 20 Ω I _D ≅ 1.0 A, V _{GEN} = 4.5 V, R _g = 1.0 Ω		30	45	ns
Turn-Off Delay Time	t _{d(off)}				15	25	
Fall Time	t _f				45	70	
Turn-On Delay Time	t _{d(on)}			15	25		
Rise Time	t _r	V _{DD} = 20 V, R _L = 20 Ω I _D ≅ 1.0 A, V _{GEN} = 10 V, R _g = 1 Ω		9	15		
Turn-Off Delay Time	t _{d(off)}			5	10		
Fall Time	t _f			40	60		
				5	10		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			20	A	
Pulse Diode Forward Current	I _{SM}				80		
Body Diode Voltage	V _{SD}	I _S = 3.5 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20 A, dI/dt = 100 A/μs, T _J = 25 °C		22	35	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			14	25	nC	
Reverse Recovery Fall Time	t _a				11		ns
Reverse Recovery Rise Time	t _b				11		

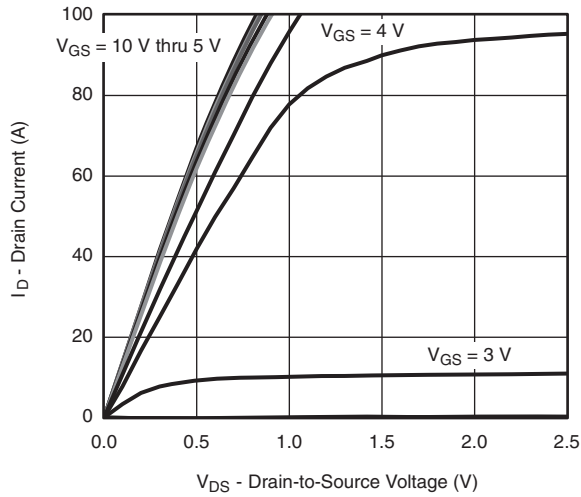
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

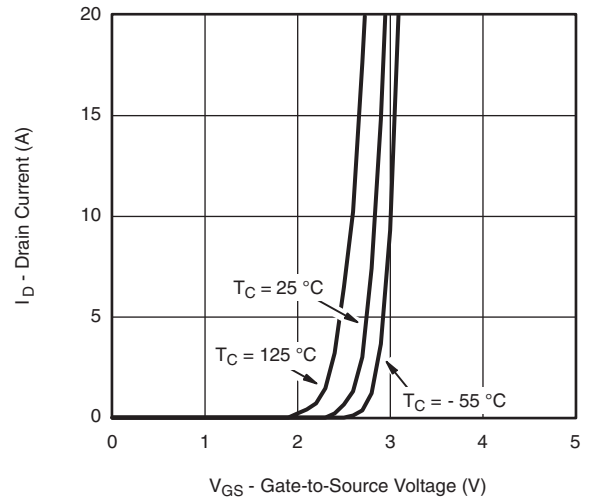
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

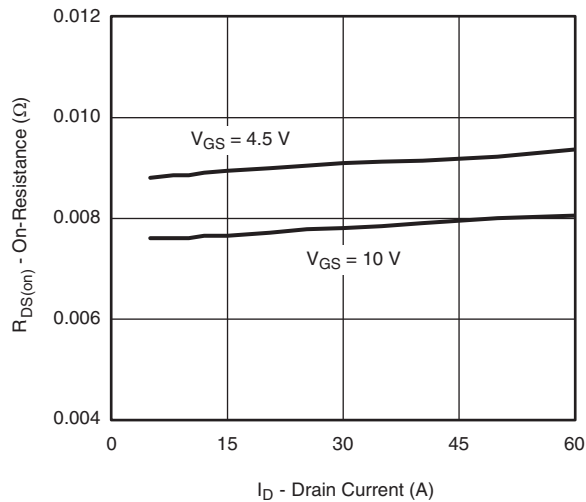
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



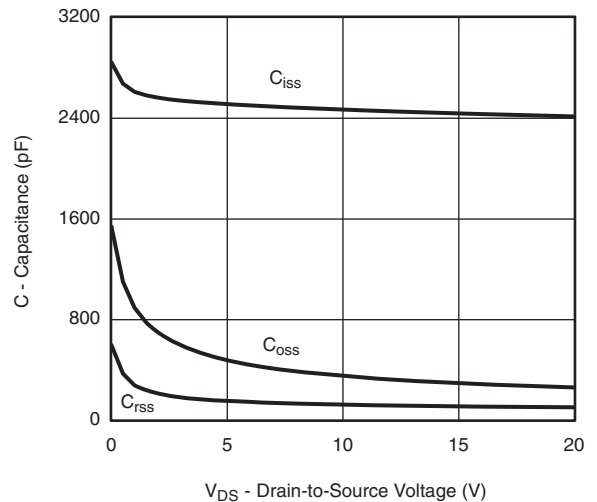
Output Characteristics



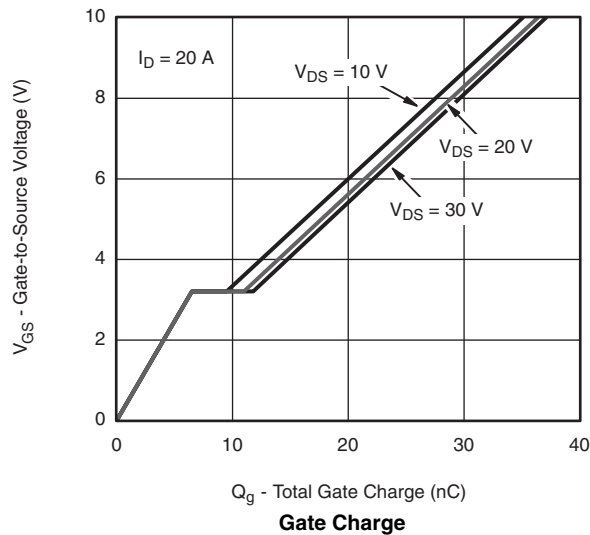
Transfer Characteristics



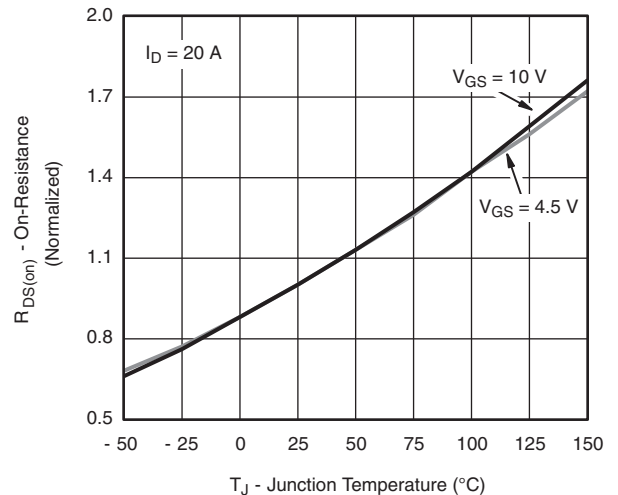
On-Resistance vs. Drain Current and Gate Voltage



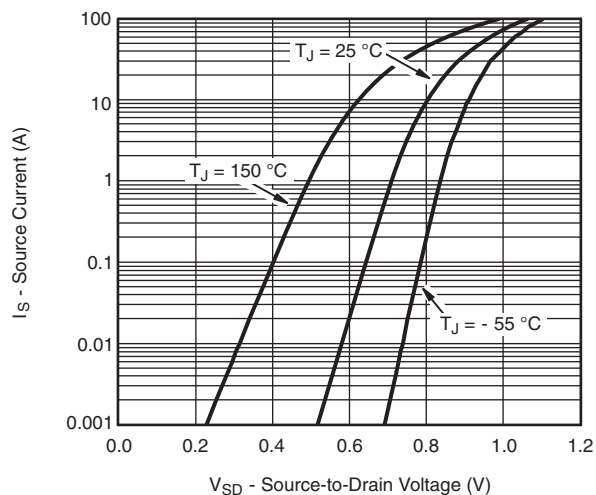
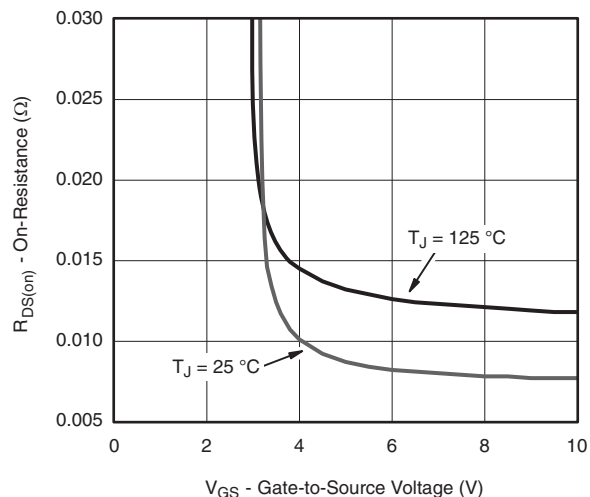
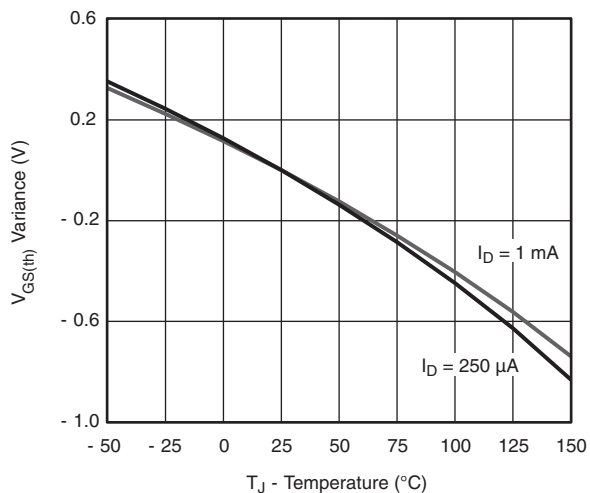
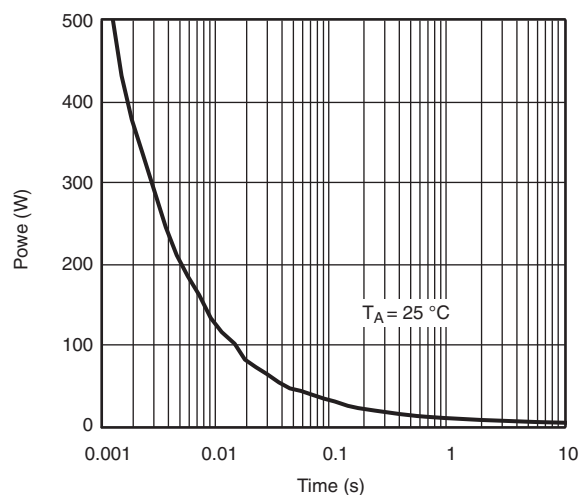
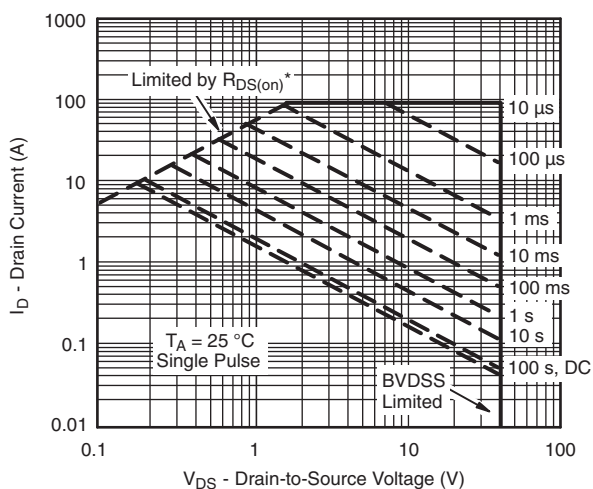
Capacitance



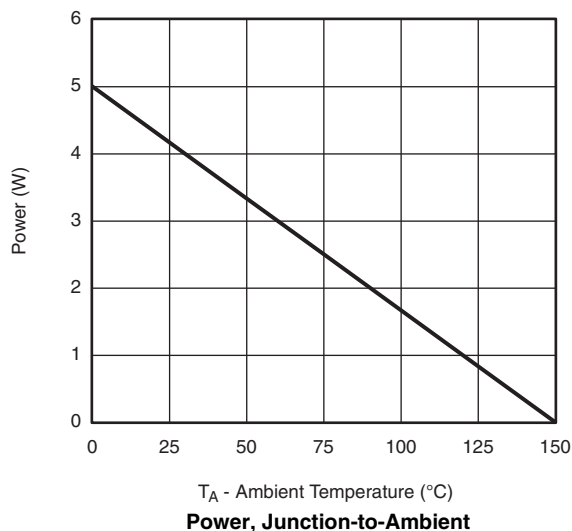
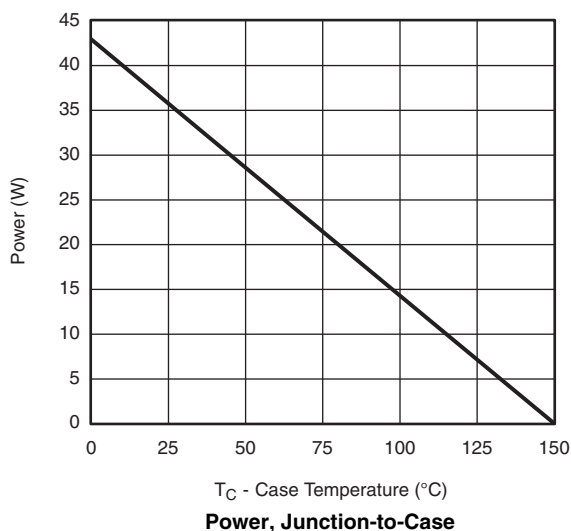
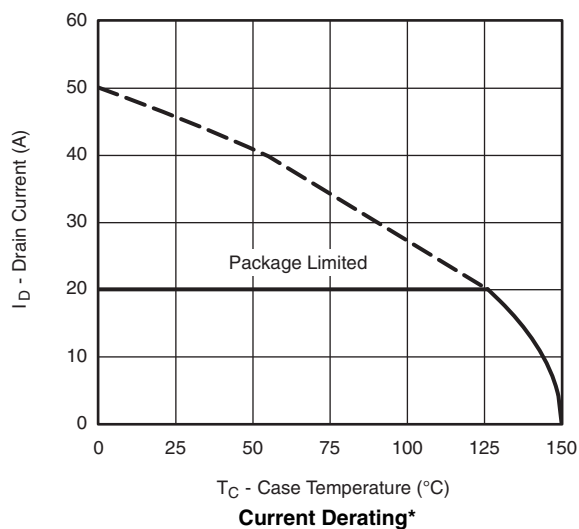
Gate Charge



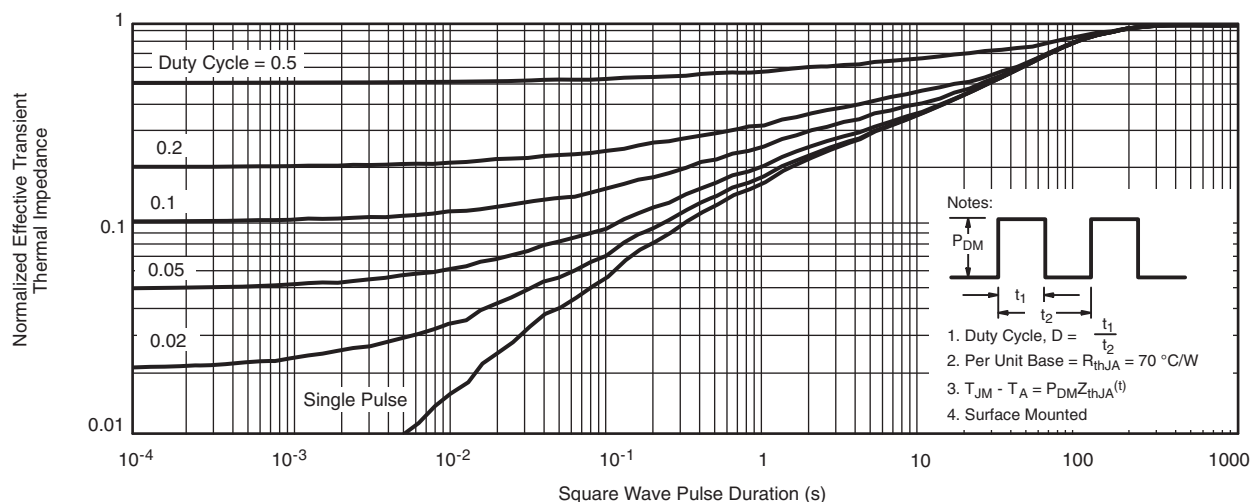
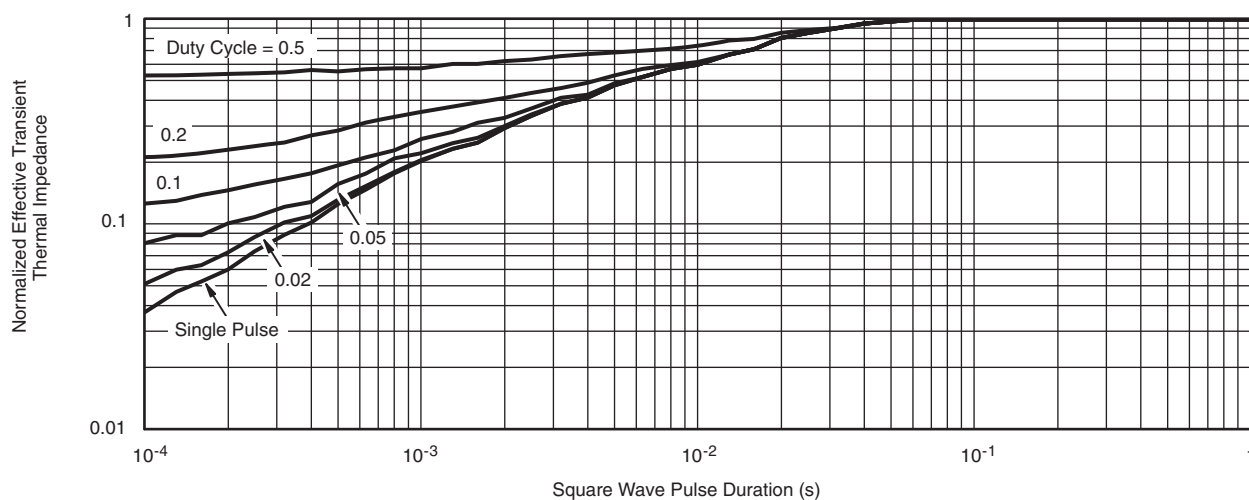
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

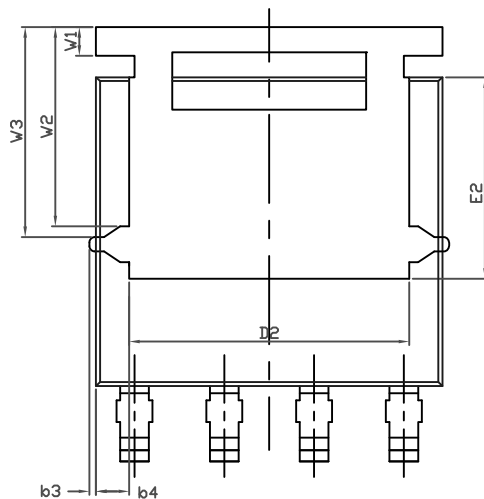
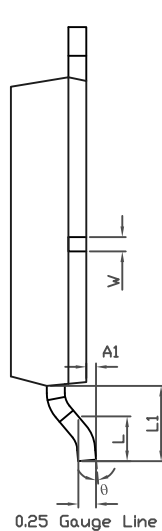
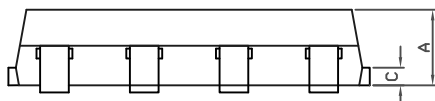
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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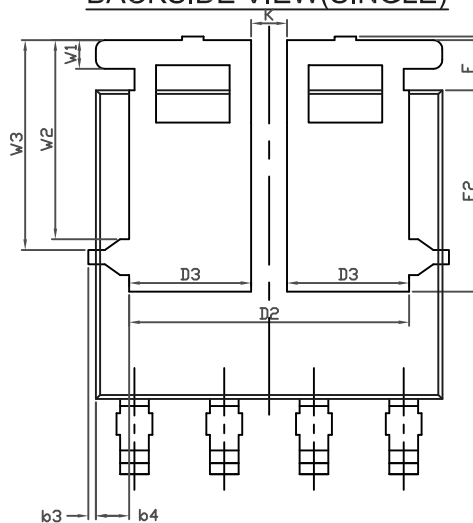
PowerPAK® SO-8L Case Outline



TOPSIDE VIEW



BACKSIDE VIEW(SINGLE)



BACKSIDE VIEW(DUAL)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2 (for AI product)	2.75	2.85	2.95	0.108	0.112	0.116
E2 (for other product)	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: C12-0026-Rev. B, 27-Aug-12 DWG: 5976						

Note

- Millimeters will govern



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