DATA SHEET
www.onsemi.com

Complementary Plastic Power Transistors

MJD200 (NPN), MJD210 (PNP)

NPN/PNP Silicon DPAK For Surface Mount Applications

Designed for Low Voltage, Low-power, High-Gain Audio amplifier applications.

Features

- High DC Current Gain
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Low Collector-Emitter Saturation Voltage
- High Current-Gain-Bandwidth Product
- Annular Construction for Low Leakage
- Epoxy Meets UL 94 V-0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

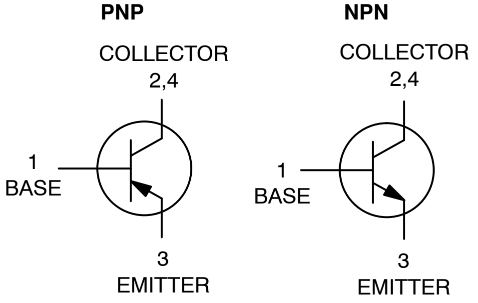
MAXIMUM RATINGS

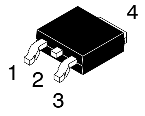
Rating	Symbol	Max	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter–Base Voltage	V_{EB}	8.0	Vdc
Collector Current-Continuous	I_C	5.0	Adc
Collector Current-Peak	I_{CM}	10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	 12.5 0.1	 W W/°C
Total Power Dissipation (Note 1) @ T_A = 25 °C Derate above 25 °C	P_D	 1.4 0.011	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C
ESD-Human Body Model	HBM	3B	V
ESD-Machine Model	MM	C	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

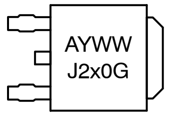
SILICON
POWER TRANSISTORS
5 AMPERES
25 VOLTS, 12.5 WATTS





DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
x = 1 or 0
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

October, 2025 − Rev. 15

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	10	°C/W
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	89.3	°C/W

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	– –	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
C Current Gain (Note 3), (I_C = 500 mAdc, V_{CE} = 1 Vdc) (I_C = 2 Adc, V_{CE} = 1 Vdc) (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	70 45 10	– 180 –	–
Collector−Emitter Saturation Voltage (Note 3) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 200 mAdc) (I_C = 5 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	– – –	0.3 0.75 1.8	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base−Emitter On Voltage (Note 3) (I_C = 2 Adc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	–	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain – Bandwidth Product (Note 4) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD200 MJD210, NJVMJD210T4G	C_{ob}	– –	80 120	pF

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
4. $f_T = |h_{fe}| \bullet f_{test}$.

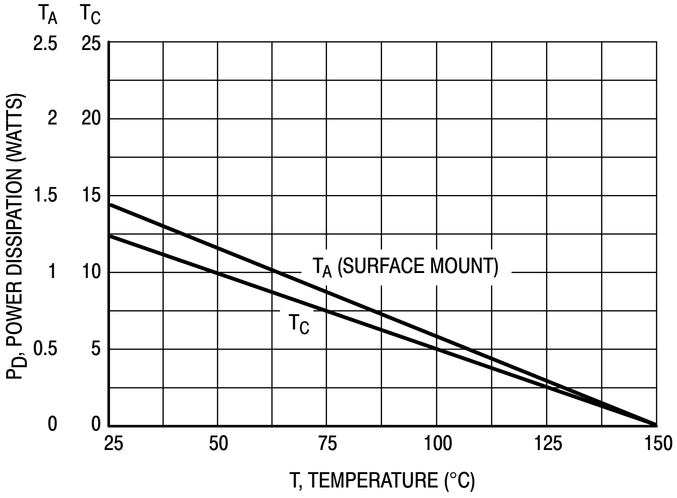
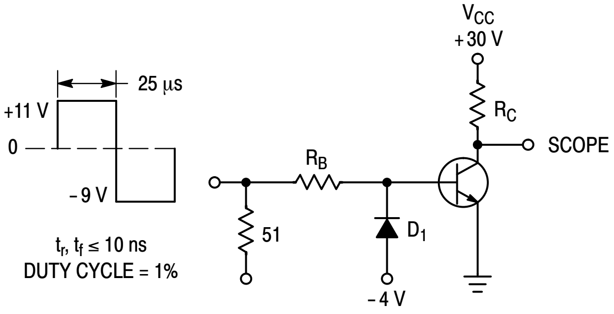


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

Figure 2. Switching Time Test Circuit

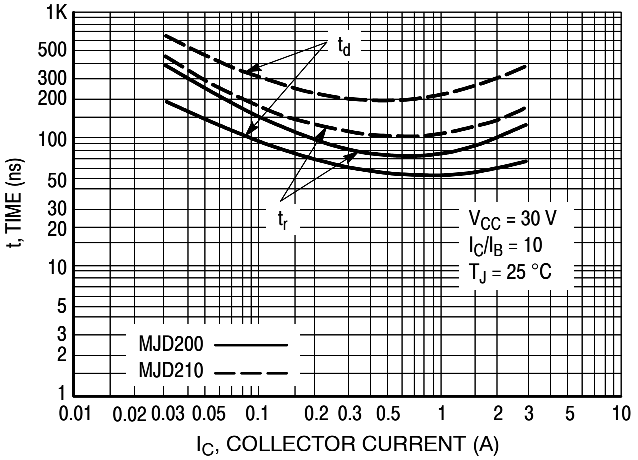


Figure 3. Turn−On Time

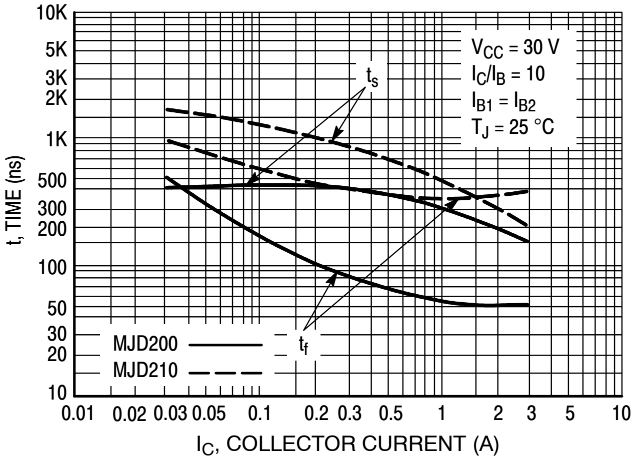


Figure 4. Turn−Off Time

NPN
MJD200

PNP
MJD210

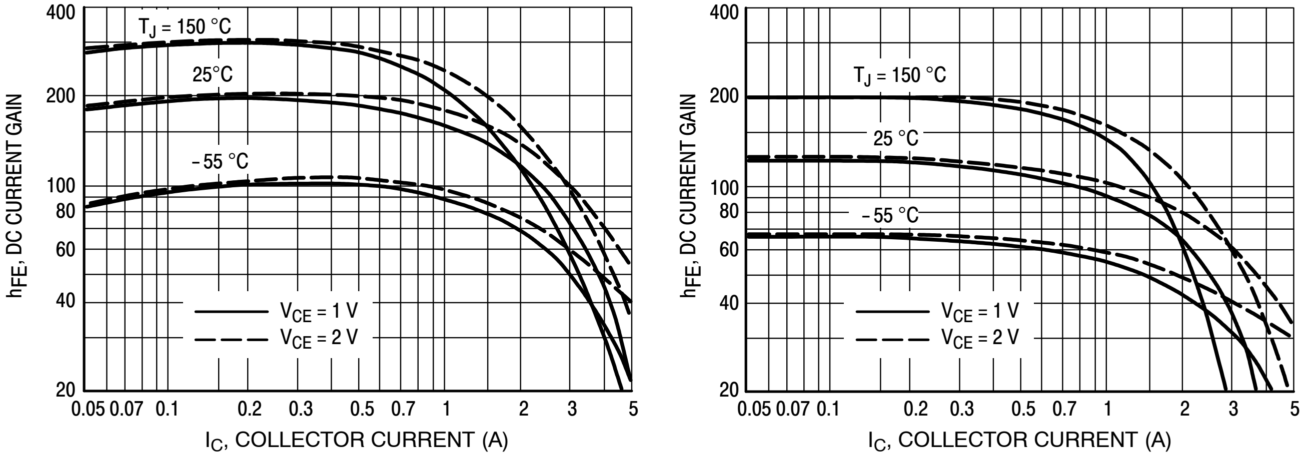


Figure 5. DC Current Gain

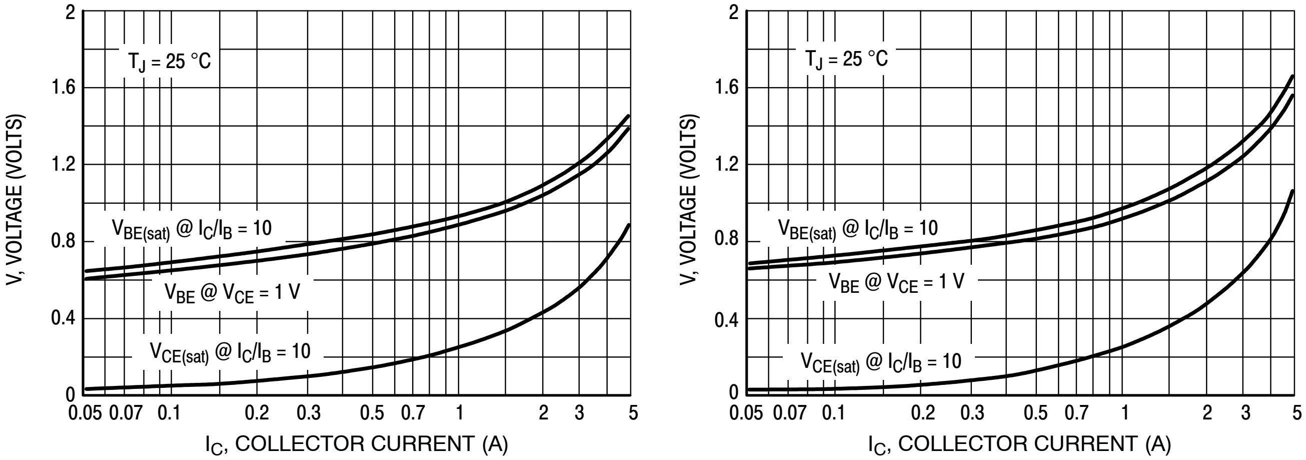


Figure 6. "On" Voltage

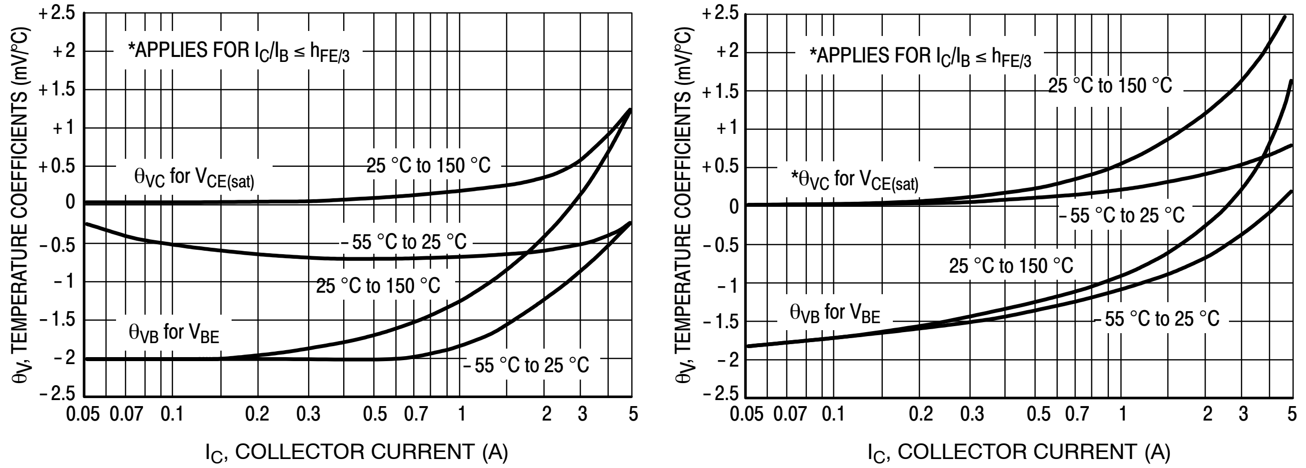


Figure 7. Temperature Coefficients

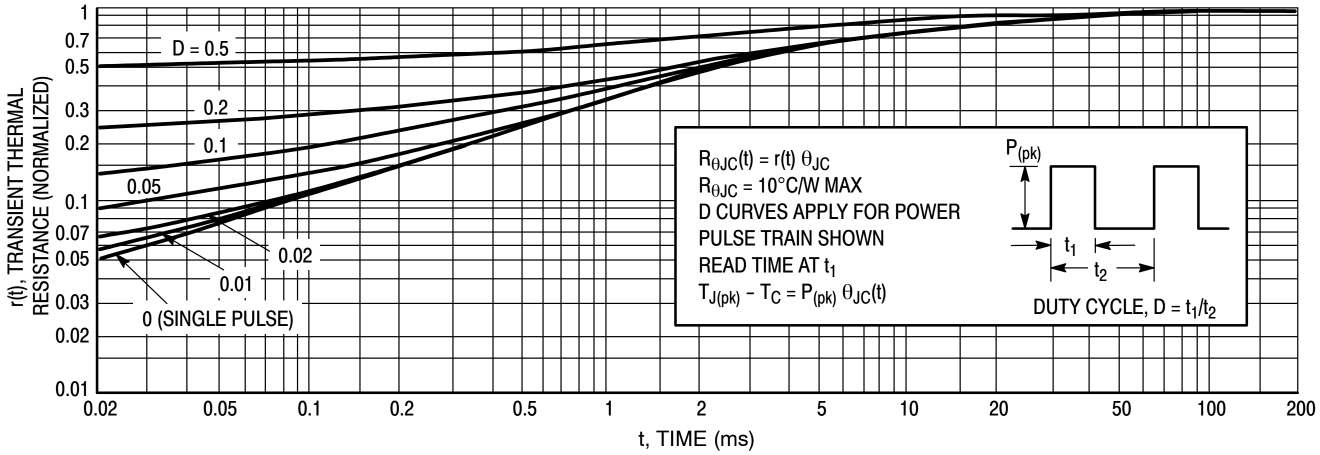


Figure 8. Thermal Response

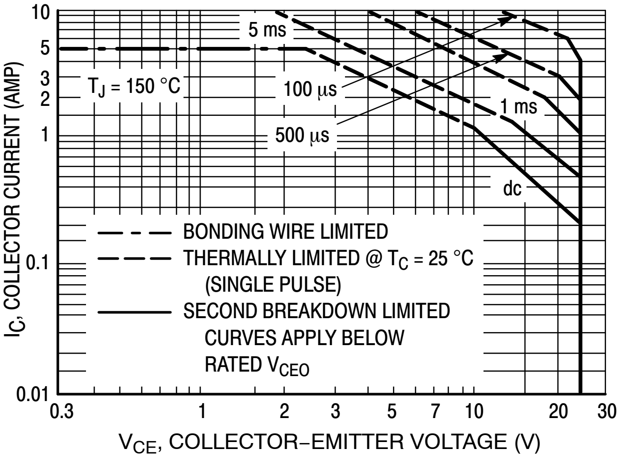


Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)}$ = 150 °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150$ °C. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

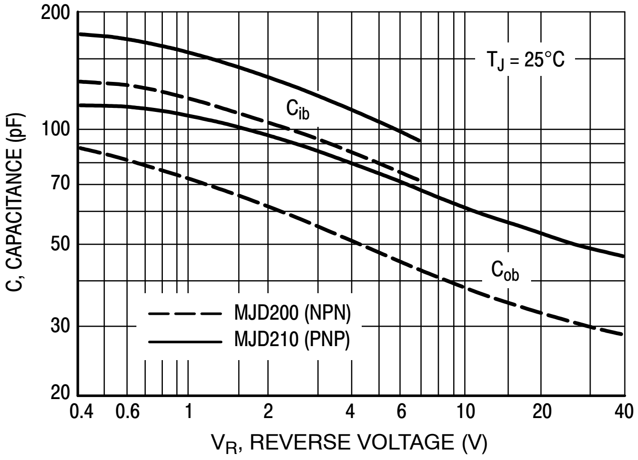


Figure 10. Capacitance

ORDERING INFORMATION

Device	Package Type	Shipping†
MJD200G	DPAK (Pb-Free)	75 Units / Rail
MJD200RLG	DPAK (Pb-Free)	1,800 / Tape & Reel
MJD200T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
MJD210G	DPAK (Pb-Free)	75 Units / Rail
MJD210RLG	DPAK (Pb-Free)	1,800 / Tape & Reel
MJD210T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
NJVMJD210T4G*	DPAK (Pb-Free)	2,500 / Tape & Reel

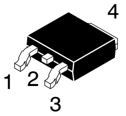
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

* NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

REVISION HISTORY

Revision	Description of Changes	Date
15	Rebranded the Data Sheet to **onsemi** format	10/8/2025

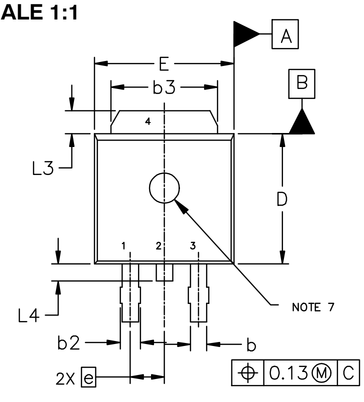
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



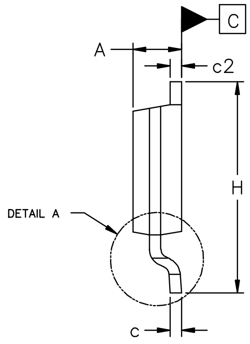
SCALE 1:1

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

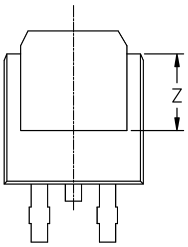


TOP VIEW

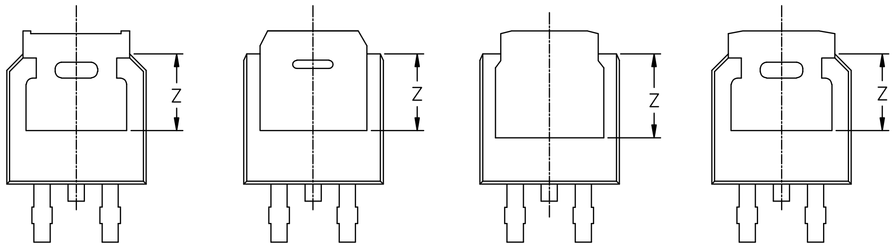


SIDE VIEW

DIM	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



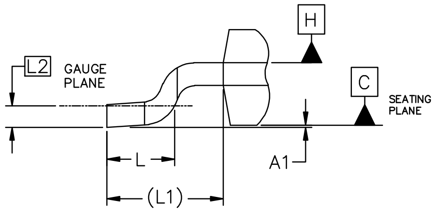
BOTTOM VIEW



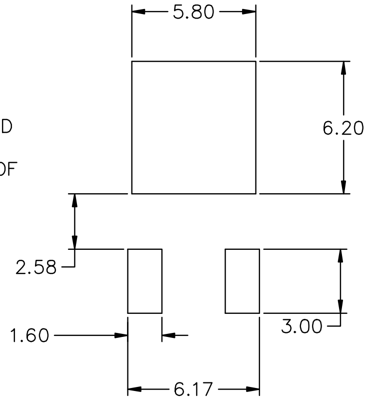
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

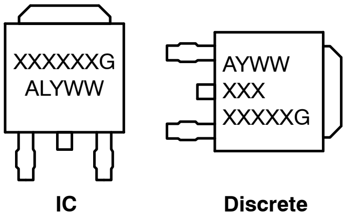
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

GENERIC MARKING DIAGRAM*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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