SG1842/2842/3842
SG1843/2843/3843

CURRENT-MODE PWM CONTROLLER

DESCRIPTION

The SG1842/43 family of control IC's provides all the necessary features to implement off-line fixed frequency, current mode switching power supplies with a minimum number of external components. Current mode architecture demonstrates improved line regulation, improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch.

The bandgap reference is trimmed to ±1% over temperature. Oscillator discharge current is trimmed to less than ±10%. The SG1842/43 has under-voltage lockout, current limiting circuitry and start-up current of less than 1 mA.

The totem pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N channel device.

The SG1842/43 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2842/43 is specified for the industrial range of -25°C to 85°C, and the SG3842/43 is designed for the commercial range of 0°C to 70°C.

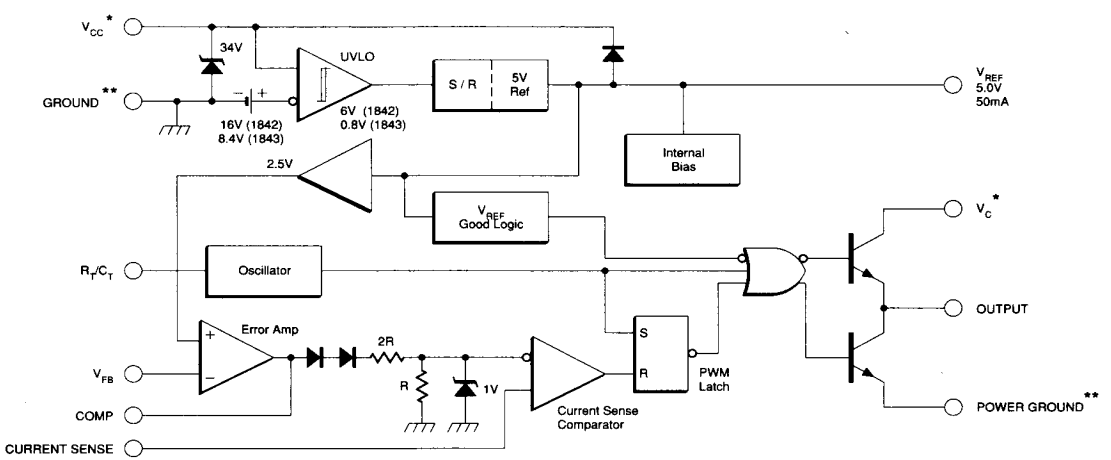
FEATURES

- **Optimized for off-line control**
- **Low start-up current (<1mA)**
- **Automatic feed forward compensation**
- **Trimmed oscillator discharge current**
- **Pulse-by-pulse current limiting**
- **Enhanced load response characteristics**
- **Under-voltage lockout with 6V hysteresis (SG1842 only)**
- **Double pulse suppression**
- **High current totem pole output (1Amp peak)**
- **Internally trimmed bandgap reference**
- **500 KHz operation**
- **Undervoltage lockout**
  SG1842 — 16 volts
  SG1843 — 8.4 volts
- **Low shoot-through current < 75mA over temperature**

HIGH RELIABILITY FEATURES - SG1842/ 1843

- **Available to MIL-STD-883 and DESC SMD**
- **Scheduled for MIL-M38510 QPL listing**
- **Radiation data available**
- **SG level "S" processing available**

BLOCK DIAGRAM



* - V_{CC} and V_C are internally connected for 8 pin packages.
** - POWER GROUND and GROUND are internally connected for 8 pin packages.

April 1990

See Application Notes for additional information.

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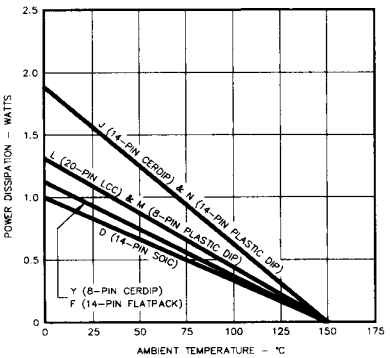
ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

Supply Voltage (I_{CC} < 30mA) ..... Self-limiting
Supply Voltage (Low Impedence Source) 30V
Output Current (peak) ..... ±1A
Output Current (continuous) 350mA
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pin 2, Pin 3) ..... -0.3V to 6.3V

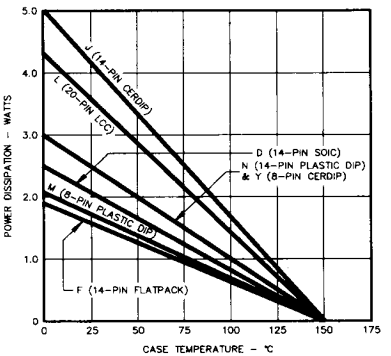
Error Amp Output Sink Current 10mA
Operating Junction Temperature
Hermetic (J, Y, F - Packages) ..... 150°C
Plastic (N, M, D - Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. All voltages are with respect to Pin 5. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage Range 30V
Output Current (peak) ..... ±1A
Output Current (continuous) 200mA
Analog Inputs (Pin 2, Pin 3) ..... 0V to 2.6V
Error Amp Output Sink Current 5mA
Oscillator Frequency Range ..... 100Hz to 500KHz

Oscillator Timing Resistor (R_T) ..... $520\Omega \le R_T \le 150k\Omega$
Oscillator Timing Capacitor (C_T) ..... $1000pF \le C_T \le 1\mu F$
Operating Ambient Temperature Range:
SG1842/43 ..... -55°C to 125°C
SG2842/43 ..... -25°C to 85°C
SG3842/43 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1842/SG1843 with $-55°C \le T_A \le 125°C$, SG2842/SG2843 with $-25°C \le T_A \le 85°C$, SG3842/SG3843 with $0°C \le T_A \le 70°C$, V_{CC} = 15V (Note 7), R_T = 10KΩ, and C_T = 3.3nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section											
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12V \le V_{IN} \le 25V$		6	20		6	20		6	20	mV
Load Regulation	$1 \le I_O \le 20mA$		6	25		6	25		6	25	mV
Temp. Stability (Note 4)			0.2	0.4		.02	0.4		0.2	0.4	mV/°C
Total Output Variation (Note 4)	Line, Load , Temp.	4.90		5.10	4.90		5.10	4.82		5.18	V
Output Noise Voltage (Note 4)	$10Hz \le f \le 10kHz$, T_J = 25°C		50			50			50		µV
Long Term Stability (Note 4)	T_A = 125°C, 1000 Hrs.		5	25		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	-30	-100	-180	mA
Oscillator Section											
Initial Accuracy	T_J = 25°C	47	52	57	47	52	57	47	52	57	kHz
Voltage Stability	$12 \le V_{CC} \le 25V$		.02	1		0.2	1		0.2	1	%
Temp. Stability (Note 4)	$T_{MIN} \le T_A \le T_{MAX}$		5			5			5		%
Amplitude	$V_{RT/CT}$ (peak to peak)		1.7			1.7			1.7		V
Discharge Current	T_J = 25°C	7.8	8.3	8.8	7.5	8.4	9.3	7.5	8.4	9.3	mA
	$T_{MIN} \le T_A \le T_{MAX}$	7.0		9.0	7.2		9.5	7.2		9.5	mA

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ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Error Amp Section											
Input Voltage	V_{COMP} = 2.5V	2.45	2.50	2.55	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	1		-0.3	-2	µA
Open Loop Gain (A_{VOL})	$2 \le V_O \le 4V$	65	90		65	90		65	90		dB
Unity Gain Bandwidth (Note 4)		0.7	1		0.7	1		0.7	1		MHz
PSRR	$12 \le V_{CC} \le 25V$	60	70		60	70		60	70		dB
Output Sink Current	V_{VFB} = 2.7V, V_{COMP} = 1.1V	2	6		2	6		2	6		mA
Output Source Current	V_{VFB} = 2.3V, V_{COMP} = 5V	-0.5	-0.8		-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	V_{VFB} = 2.3V, R_L = 15K to gnd	5	6		5	6		5	6		V
V_{OUT} Low	V_{VFB} = 2.7V, R_L = 15K to V_{REF}		0.7	1.1		0.7	1.1		0.7	1.1	V
Current Sense Section											
Gain (Notes 5 & 6)		2.85	3	3.15	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal (Note 5)	V_{COMP} = 5V	0.9	1	1.1	0.9	1	1.1	0.9	1	1.1	V
PSRR (Note 5)	$12 \le V_{CC} \le 25V$		70			70			70		dB
Input Bias Current			-2	-10		-2	-10		-2	-10	µA
Delay to Output (Note 4)			150	300		150	300		150	300	ns
Output Section											
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Under-Voltage Lockout Section											
Start Threshold (1842)		15	16	17	15	16	17	14.5	16	17.5	V
Min. Operating Voltage (1842)	After Turn On	9	10	11	9	10	11	8.5	10	11.5	V
Start Threshold (1843)		7.8	8.4	9.0	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage (1843)	After Turn On	7.0	7.6	8.2	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section											
Max. Duty Cycle		93	95	100	90	95	100	90	95	100	%
Min. Duty Cycle				0			0			0	%
Power Consumption Section											
Start-Up Current			0.5	1		0.5	1		0.5	1	mA
Operating Supply Current	V_{VFB} = V_{ISENSE} = 0V		11	17		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA		34			34			34		V

Notes: 4. These parameters, although guaranteed, are not 100% tested in production.

5. Parameter measured at trip point of latch with V_{VFB} = 0.

6. Gain defined as: $A = \frac{\Delta V_{COMP}}{\Delta V_{ISENSE}}$; $0 \le V_{ISENSE} \le 0.8V$.

7. Adjust V_{CC} above the start threshold before setting at 15V.

CHARACTERISTIC CURVES

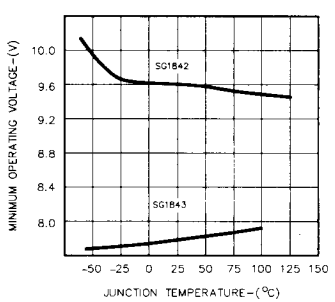

FIGURE 1.
DROPOUT VOLTAGE VS. TEMPERATURE

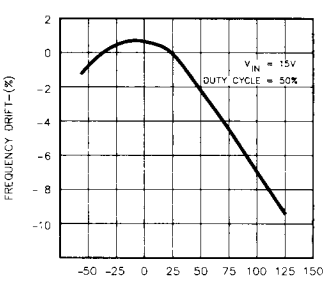

FIGURE 2.
OSCILLATOR TEMPERATURE STABILITY

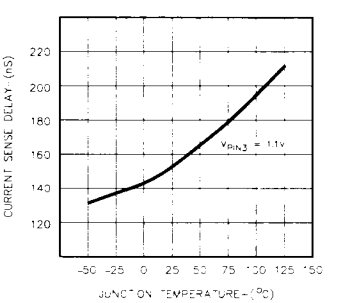

FIGURE 3.
CURRENT SENSE TO OUTPUT DELAY VS. TEMP.

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CHARACTERISTIC CURVES (continued)

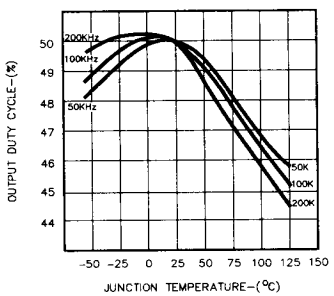

FIGURE 4.
OUTPUT DUTY CYCLE VS. TEMPERATURE

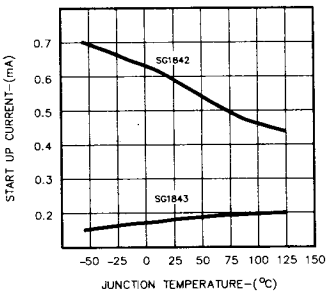

FIGURE 5.
START-UP CURRENT VS. TEMPERATURE

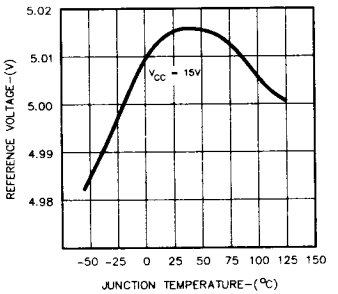

FIGURE 6.
REFERENCE VOLTAGE VS. TEMPERATURE

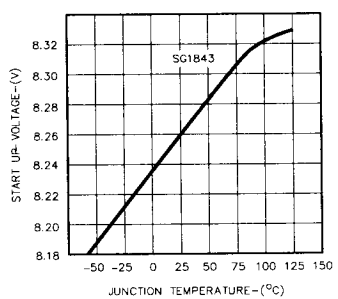

FIGURE 7.
START-UP VOLTAGE THRESHOLD
VS. TEMPERATURE

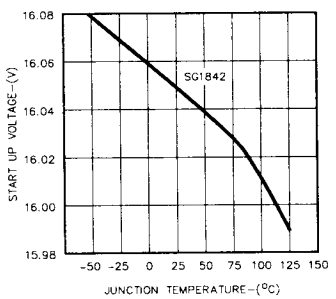

FIGURE 8.
START-UP VOLTAGE THRESHOLD
VS. TEMPERATURE

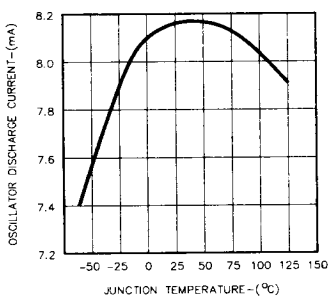

FIGURE 9.
OSCILLATOR DISCHARGE CURRENT
VS. TEMPERATURE

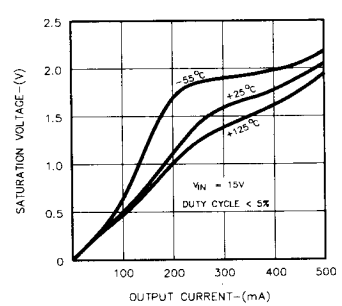

FIGURE 10.
OUTPUT SATURATION VOLTAGE VS. OUTPUT
CURRENT AND TEMPERATURE
(SINK TRANSISTOR)

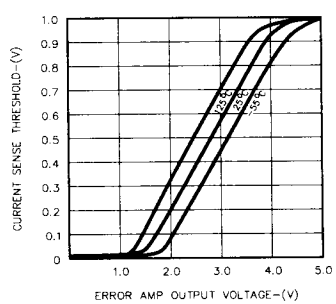

FIGURE 11.
CURRENT SENSE THRESHOLD VS. ERROR
AMPLIFIER OUTPUT

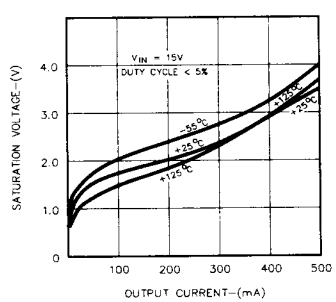

FIGURE 12.
OUTPUT SATURATION VOLTAGE VS. OUTPUT
CURRENT AND TEMPERATURE
(SOURCE TRANSISTOR)

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APPLICATION INFORMATION

OSCILLATOR:

The oscillator of the 1842/43 family of PWM's is designed such that many values of R_T & C_T will give the same oscillator frequency, but only one combination will yield a specific duty cycle at a given frequency.

A set of formulas are given to determine the values of R_T & C_T for a given frequency and maximum duty cycle. (Note: These formulas are less accurate for smaller duty cycles or higher frequencies. This will require trimming of R_T or C_T to correct for this error.)

GIVEN: Frequency ≡ f
Maximum Duty Cycle ≡ D_m

CALCULATE:

$$R_T = 267 \left[\frac{(1.76)^{1/D_m} - 1}{(1.76)^{(1-D_m)/D_m} - 1} \right] \quad (\Omega)$$

where $.3 < D_m < .95$

$$C_T = \frac{1.86 \times D_m}{f \times R_T} \quad (\mu F)$$

EXAMPLE:

A Flyback power supply requires a maximum of 45% duty-cycle at a switching frequency of 50KHz. What are the values of R_T and C_T?

GIVEN: f = 50KHz
$D_m = 0.45$

CALCULATE: $R_T = 267 \left[\frac{(1.76)^{1/.045} - 1}{(1.76)^{.55/.45} - 1} \right] = 674\Omega$

$$C_T = \frac{1.86 \times .45}{50000 \times 674} = .025\mu F$$

For Duty-Cycles above 95% use:

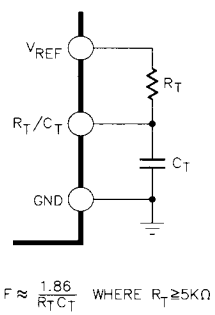

FIGURE 13 — OSCILLATOR TIMING CIRCUIT

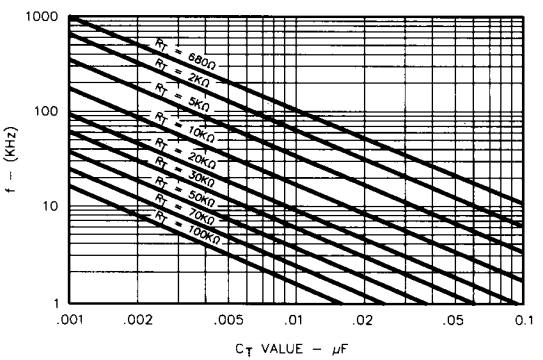

FIGURE 14 — OSCILLATOR FREQUENCY VS. R_T FOR VARIOUS C_T

APPLICATION CIRCUITS (Note 8)

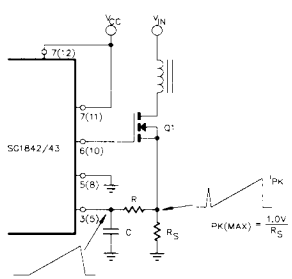

FIGURE 15 — CURRENT SENSE SPIKE SUPPRESSION

The RC low pass filter will eliminate the leading edge current spike caused by parasitics of Power MOSFET.

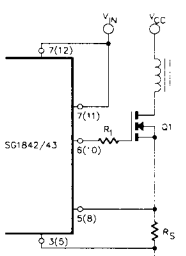

FIGURE 16 — MOSFET PARASITIC OSCILLATIONS

A resistor (R_1) in series with the MOSFET gate will reduce overshoot & ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

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APPLICATION CIRCUITS (continued)

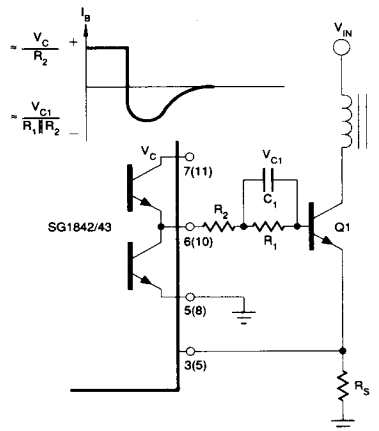

FIGURE 17 — BIPOLAR TRANSISTOR DRIVE

The 1842/43 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

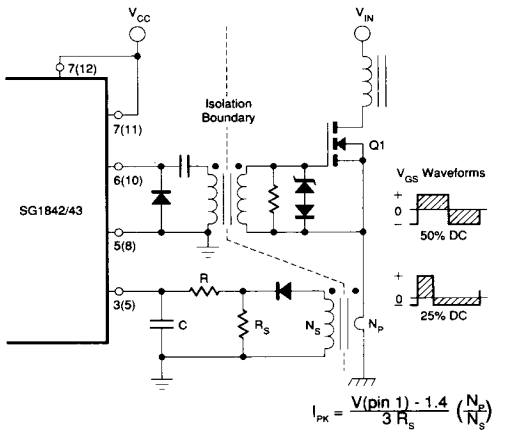

FIGURE 18 — ISOLATED MOSFET DRIVE

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

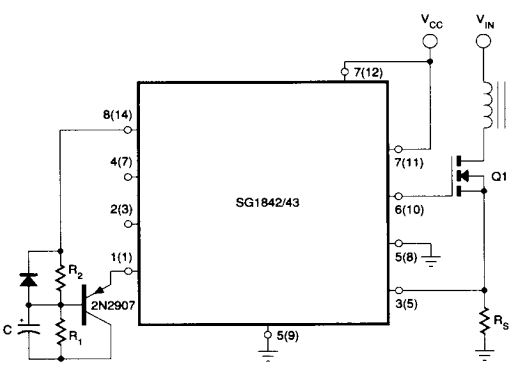

FIGURE 19 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

Soft start and adjustable peak current can be done with the external circuitry shown above.

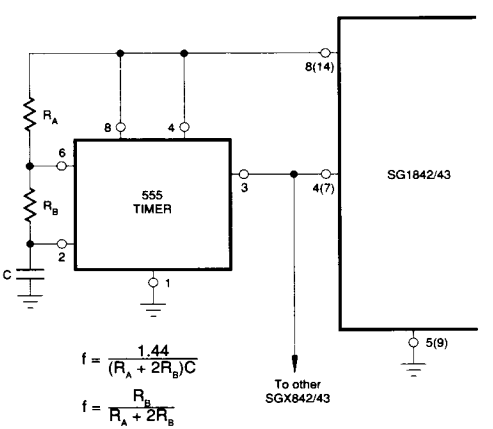

FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI-UNIT SYNCHRONIZATION

Precision duty cycle limiting as well as synchronizing several 1842/43's is possible with the above circuitry.

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APPLICATION CIRCUITS (continued)

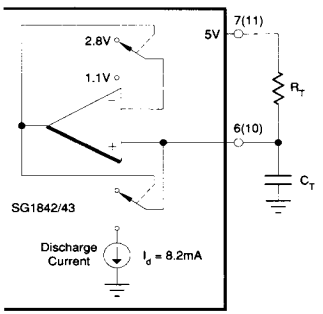

FIGURE 21 — OSCILLATOR CONNECTION

The oscillator is programmed by the values selected for the timing components R_T and C_T. Refer to application information for calculation of the component values.

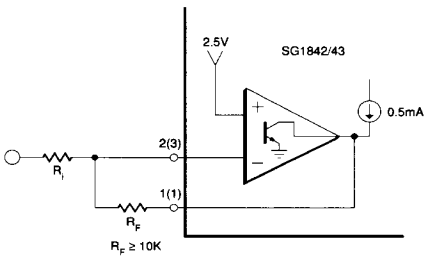

FIGURE 22 — ERROR AMPLIFIER CONNECTION

Error amplifier is capable of sourcing and sinking current up to 0.5mA.

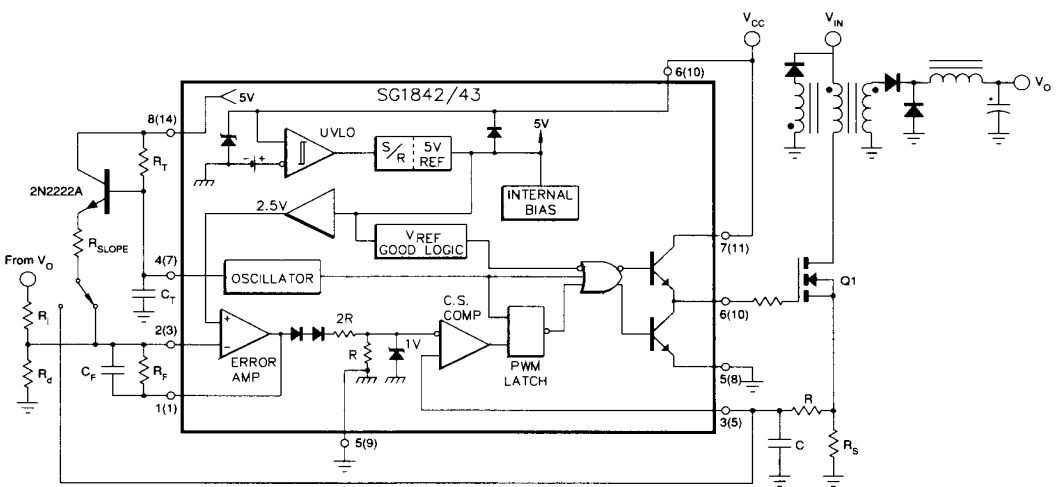

FIGURE 23 — SLOPE COMPENSATION

Due to inherent instability of current mode converters running above 50% duty cycle, a slope compensation should be added to either current sense pin or the error amplifier. Figure 23 shows a typical slope compensation technique.

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APPLICATION CIRCUITS (continued)

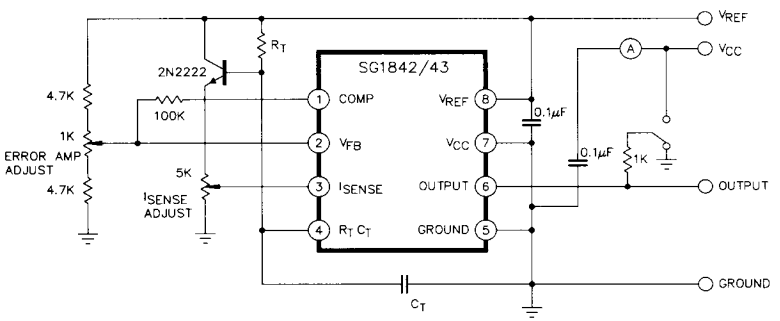

FIGURE 24 — OPEN LOOP LABORATORY FIXTURE

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and ypass capacitors should be connected to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

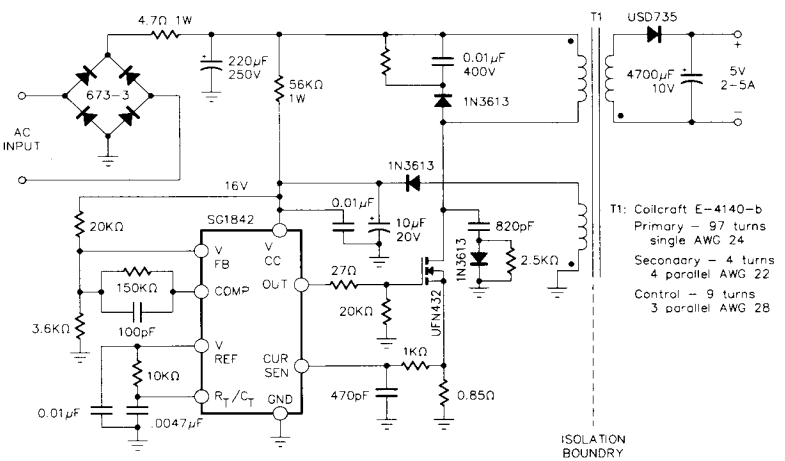

FIGURE 25 — OFF-LINE FLYBACK REGULATOR

SPECIFICATIONS

Input line voltage:	90VAC to 130VAC
Input frequency:	50 or 60Hz
Switching frequency:	40KHz ±10%
Output power:	25W maximum
Output voltage:	5V +5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 Watts,	
V_{IN} = 90VAC:	70%
V_{IN} = 130VAC:	65%
Output short-circuit current:	2.5Amp average

* This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the SG1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance.

Note 8. Pin numbers referenced are for 8 pin package and pin numbers in parenthesis are for 14 pin packages.

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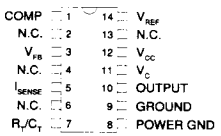
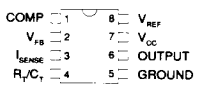
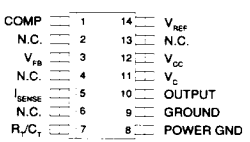
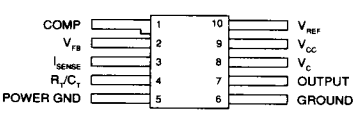
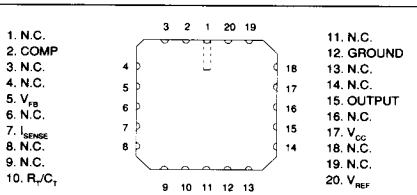
CONNECTION DIAGRAM & ORDERING INFORMATION (See notes below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1842J/883B	-55°C to 125°C	
	SG1842J	-55°C to 125°C	
	SG2842J	-25°C to 85°C	
	SG3842J	0°C to 70°C	
	SG1843J/883B	-55°C to 125°C	
	SG1843J	-55°C to 125°C	
	SG2843J	-25°C to 85°C	
	SG3843J	0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG2842N	-25°C to 85°C	
	SG3842N	0°C to 70°C	
	SG2843N	-25°C to 85°C	
	SG3843N	0°C to 70°C	
8-PIN CERAMIC DIP Y - PACKAGE	SG1842Y/883B	-55°C to 125°C	
	SG1842Y	-55°C to 125°C	
	SG2842Y	-25°C to 85°C	
	SG3842Y	0°C to 70°C	
	SG1843Y/883B	-55°C to 125°C	
	SG1843Y	-55°C to 125°C	
	SG2843Y	-25°C to 85°C	
	SG3843Y	0°C to 70°C	
8-PIN PLASTIC DIP M - PACKAGE	SG2842M	-25°C to 85°C	
	SG3842M	0°C to 70°C	
	SG2843M	-25°C to 85°C	
	SG3843M	0°C to 70°C	
14-PIN PLASTIC S.O.I.C. D - PACKAGE	SG2842D	-25°C to 85°C	
	SG3842D	0°C to 70°C	
	SG2843D	-25°C to 85°C	
	SG3843D	0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG1842F/883B	-55°C to 125°C	
	SG1842F	-55°C to 125°C	
	SG1843F/883B	-55°C to 125°C	
	SG1843F	-55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1842L/883B	-55°C to 125°C	
	SG1842L	-55°C to 125°C	
	SG1843L/883B	-55°C to 125°C	
	SG1843L	-55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All packages are viewed from the top.

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