



3.3V CMOS DUAL 1-TO-5 CLOCK DRIVER

IDT49FCT3805D/E

FEATURES:

- Advanced CMOS Technology
- Guaranteed low skew < 200ps (max.)
- Very low propagation delay < 2.5ns (max)
- Very low duty cycle distortion < 270ps (max)
- Very low CMOS power levels
- Operating frequency up to 166MHz
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- $V_{CC} = 3.3V \pm 0.3V$
- Available in SSOP and QSOP packages

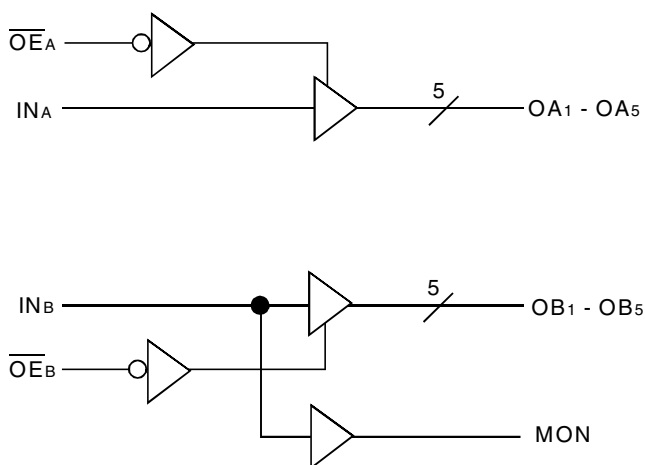
DESCRIPTION:

The FCT3805 is a 3.3 volt clock driver built using advanced CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The FCT3805 offers low capacitance inputs.

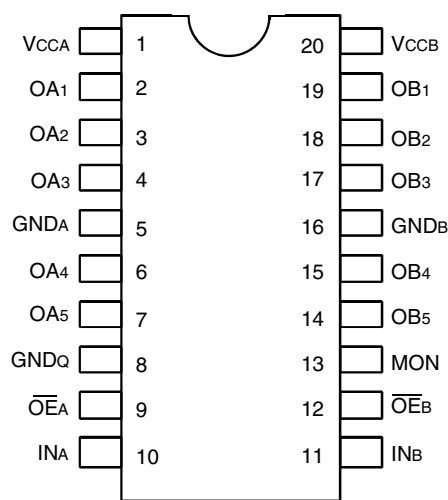
The FCT3805 is designed for high speed clock distribution where signal quality and skew are critical. The FCT3805 also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

For more information on using the FCT3805 with two different input frequencies on bank A and B, please see AN-236.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{CC}	Input Power Supply Voltage	−0.5 to +4.6	V
V _I	Input Voltage	−0.5 to +5.5	V
V _O	Output Voltage	−0.5 to V _{CC} +0.5	V
T _J	Junction Temperature	150	°C
T _{STG}	Storage Temperature	−65 to +165	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A, \overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN _A , IN _B	Clock Inputs
OA _n , OB _n	Clock Outputs
MON	Monitor Output

FUNCTION TABLE (1)

Inputs		Outputs	
$\overline{OE}_A, \overline{OE}_B$	IN _A , IN _B	OA _n , OB _n	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE:

- H = HIGH
L = LOW
Z = High-Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3	4	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	6	pF

NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified

Industrial: T_A = −40°C to +85°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level			2	—	5.5	V
V _{IL}	Input LOW Level			−0.5	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _I = 5.5V	—	—	±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _I = GND	—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Outputs Pins)	V _{CC} = Max.	V _O = V _{CC}	—	—	±1	
I _{OZL}			V _O = GND	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = −18mA		—	−0.7	−1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ^(3,4)		−45	−74	−180	mA
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ^(3,4)		50	90	200	mA
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ^(3,4)		−60	−135	−240	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = −12mA	2.4 ⁽⁵⁾	3	—	V
			I _{OH} = −8mA	2.4 ⁽⁵⁾	3	—	
			I _{OH} = −100μA	V _{CC} − 0.2	—	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12mA	—	0.3	0.4	V
			I _{OL} = 8mA	—	0.2	0.4	
			I _{OL} = 100μA	—	—	0.2	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, 25°C ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} − 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC} I _{CC} H I _{CC} Z	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}		—	0.1	30	μA
ΔI _{CC}	Power Supply Current per Input HIGH	V _{CC} = Max. V _{IN} = V _{CC} - 0.6V		—	45	300	μA
I _{CCD}	Dynamic Power Supply Current per Output ⁽³⁾	V _{CC} = Max. C _L = 15pF All Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	80	120	μA/MHz
I _C	Total Power Supply Current ⁽⁴⁾	V _{CC} = Max. C _L = 15pF All Outputs Toggling f _i = 133MHz	V _{IN} = V _{CC} V _{IN} = GND	—	125	150	mA
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	125	150	
		V _{CC} = Max. C _L = 15pF All Outputs Toggling f _i = 166MHz	V _{IN} = V _{CC} V _{IN} = GND	—	155	195	
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	160	195	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$
I_{CC} = Quiescent Current (I_{CC}L, I_{CC}H and I_{CC}Z)
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} - 0.6V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_o = Output Frequency
N_o = Number of Outputs at f_o

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 3805D (3,4)

Symbol	Parameter	Conditions ⁽¹⁾	Min. ⁽²⁾	Max.	Unit
t _{PLH}	Propagation Delay	C _L = 15pF f ≤ 133MHz	1	3	ns
t _{PHL}	IN _A to O _{AN} , IN _B to O _{BN}				
t _R	Output Rise Time (0.8V to 2V)		—	1.5	ns
t _F	Output Fall Time (2V to 0.8V)		—	1.5	ns
tsk(O)	Same device output pin to pin skew ⁽⁵⁾		—	270	ps
tsk(P)	Pulse skew ^(6,9)		—	270	ps
tsk(PP)	Part to part skew ⁽⁷⁾		—	550	ps
t _{PZL}	Output Enable Time		—	5.2	ns
t _{PZH}	$\overline{OE}_A$ to O _{AN} , $\overline{OE}_B$ to O _{BN}				
t _{PLZ}	Output Disable Time		—	5.2	ns
t _{PHZ}	$\overline{OE}_A$ to O _{AN} , $\overline{OE}_B$ to O _{BN}				
f _{MAX}	Input Frequency		—	133	MHz

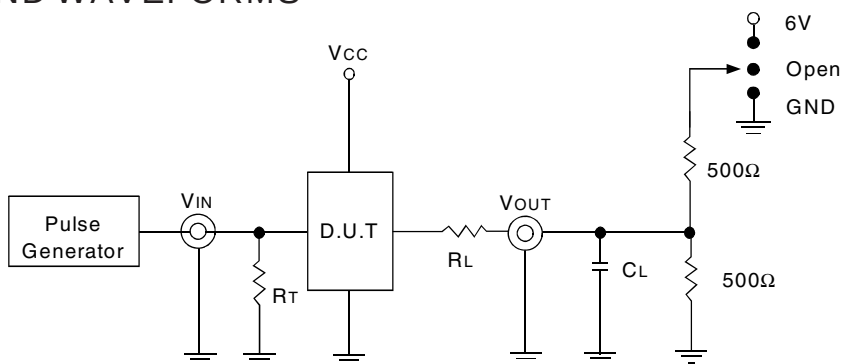
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 3805E (3,4)

Symbol	Parameter	Conditions ^(1,8)	Min. ⁽²⁾	Max.	Unit
t _{PLH}	Propagation Delay	C _L = 15pF f ≤ 166MHz	0.5	2.5	ns
t _{PHL}	IN _A to O _{AN} , IN _B to O _{BN}				
t _R	Output Rise Time (0.8V to 2V)		—	1	ns
t _F	Output Fall Time (2V to 0.8V)		—	1	ns
tsk(O)	Same device output pin to pin skew ⁽⁵⁾		—	200	ps
tsk(P)	Pulse skew ^(6,9)		—	270	ps
tsk(PP)	Part to part skew ⁽⁷⁾		—	550	ps
t _{PZL}	Output Enable Time		—	5.2	ns
t _{PZH}	$\overline{OE}_A$ to O _{AN} , $\overline{OE}_B$ to O _{BN}				
t _{PLZ}	Output Disable Time		—	5.2	ns
t _{PHZ}	$\overline{OE}_A$ to O _{AN} , $\overline{OE}_B$ to O _{BN}				
f _{MAX}	Input Frequency		—	166	MHz

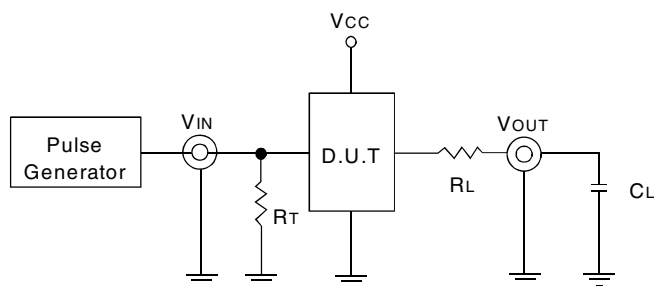
NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- t_{PLH}, t_{PHL}, tsk(P), and tsk(O) are production tested. All other parameters guaranteed but not production tested.
- Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.
- Skew measured between all outputs under identical transitions and load conditions.
- Skew measured is difference between propagation delay times t_{PHL} and t_{PLH} of same outputs under identical load conditions.
- Part to part skew for all outputs given identical transitions and load conditions at identical V_{CC} levels and temperature.
- Airflow of 1m/s is recommended for frequencies above 133MHz.
- This parameter is measured using f = 1MHz.

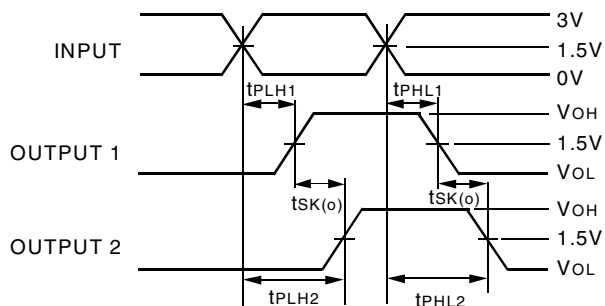
TEST CIRCUITS AND WAVEFORMS



Enable and Disable Time Circuit



$C_L = 15pF$ Test Circuit



$$t_{SK(O)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Output Skew - $t_{SK(O)}$

SWITCH POSITION

Test	Switch
Disable Low Enable Low	6V
Disable High Enable High	GND

TEST CONDITIONS

Symbol	$V_{CC} = 3.3V \pm 0.3V$	Unit
C_L	15	pF
R_T	Z_{OUT} of pulse generator	Ω
R_L	33	Ω
t_R / t_F	1 (0V to 3V or 3V to 0V)	ns

DEFINITIONS:

C_L = Load capacitance; includes jig and probe capacitance.

R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

t_R / t_F = Rise/Fall time of the input stimulus from the Pulse Generator.

The diagram illustrates the timing characteristics of the 74VHC123 during ENABLE and DISABLE transitions. The CONTROL INPUT is shown as a square wave. The OUTPUT NORMALLY LOW (SWITCH CLOSED) and OUTPUT NORMALLY HIGH (SWITCH OPEN) waveforms show the output voltage response. Key timing parameters are labeled: t_{pZL} (output delay to low), t_{pZH} (output delay to high), t_{PLZ} (propagation delay to low), and t_{PHZ} (propagation delay to high). Voltage levels are marked at 3V, 1.5V, and 0V. Output levels are also marked at V_{OH} and V_{OL} with 0.3V margins.

The diagram shows three signals over time: INPUT, PACKAGE 1 OUTPUT, and PACKAGE 2 OUTPUT. The INPUT signal is a square wave with levels 3V, 1.5V, and 0V. PACKAGE 1 OUTPUT has levels V_{OH}, 1.5V, and V_{OL}. PACKAGE 2 OUTPUT has levels V_{OH}, 1.5V, and V_{OL}. The timing parameters are defined as follows:

- t_{PLH1} : Propagation delay from the rising edge of the INPUT to the rising edge of PACKAGE 1 OUTPUT.
- t_{PLH2} : Propagation delay from the rising edge of the INPUT to the rising edge of PACKAGE 2 OUTPUT.
- $t_{SK(PP)}$: Skew between the rising edges of PACKAGE 1 OUTPUT and PACKAGE 2 OUTPUT.

The formula for skew is given as:

$$t_{SK(PP)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PLH2} - t_{PHL1}|$$

Timing diagram illustrating the relationship between Input and Output signals. The Input signal is shown as a square wave with levels 3V, 1.5V, and 0V. The Output signal is shown as a square wave with levels V_{OH} , 1.5V, and V_{OL} . The diagram highlights the setup time (t_{PLH}) and hold time (t_{PHL}) intervals. The total setup and hold time is given by the equation:

$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

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ORDERING INFORMATION

49FCT	XXXX	X	X		
	Device Type	Package	Process		
				I	-40°C to +85°C (Industrial)
				PY	Shrink Small Outline IC
				PYG	SSOP - Green
				Q	Quarter-size Small Outline IC
				QG	QSOP - Green
				3805D	3.3V CMOS Dual 1-to-5 Clock Driver
				3805E	



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