MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Document order number: MC33794/D
Rev 7.0, 04/2004

Advance Information

33794

Electric Field Imaging Device

ELECTRIC FIELD IMAGING DEVICE

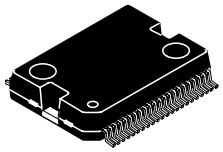
The 33794 is intended for applications where noncontact sensing of objects is desired. When connected to external electrodes, an electric field is created.

The 33794 is intended for use in detecting objects in this electric field. The IC generates a low-frequency sine wave. The frequency is adjustable by using an external resistor and is optimized for 120 kHz. The sine wave has very low harmonic content to reduce harmonic interference.

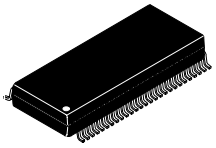
The 33794 also contains support circuits for a microcontroller unit (MCU) to allow the construction of a two-chip E-field system.

Features

- Supports up to 9 Electrodes and 2 References
- Shield Driver for Driving Remote Electrodes Through Coaxial Cables
- +5.0 V Regulator to Power External Circuit
- ISO-9141 Physical Layer Interface
- Lamp Driver Output
- Watchdog and Power-ON Reset Timer
- Critical Internal Nodes Scaled and Selectable for Measurement
- High-Purity Sine Wave Generator Tunable with External Resistor



DH SUFFIX
CASE 1291-01
44-LEAD HSOP

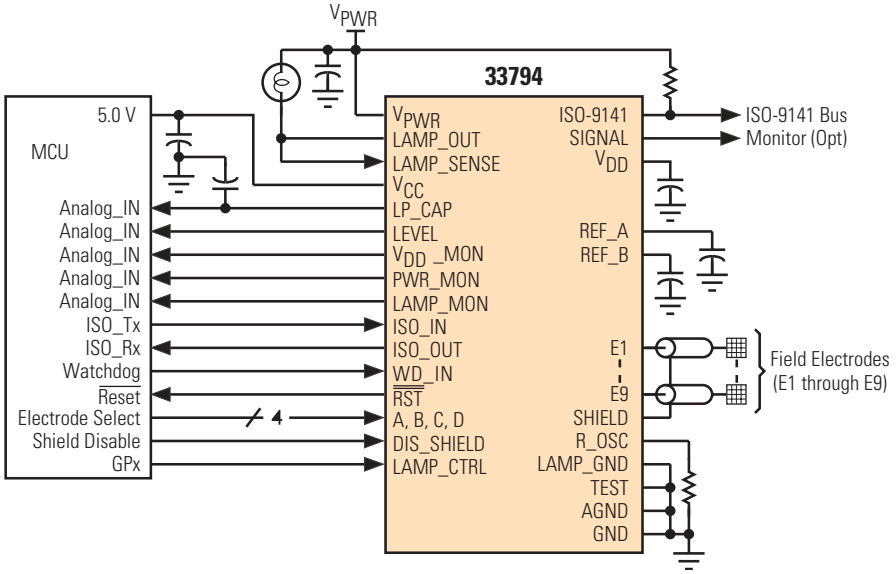


DWB SUFFIX
CASE 1390-01
54-LEAD SOICW-EP

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33794DH/R2	-40°C to 85°C	44 HSOP
MC33794DWB/R2		54 SOICW-EP

33794 Simplified Application Diagram



This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

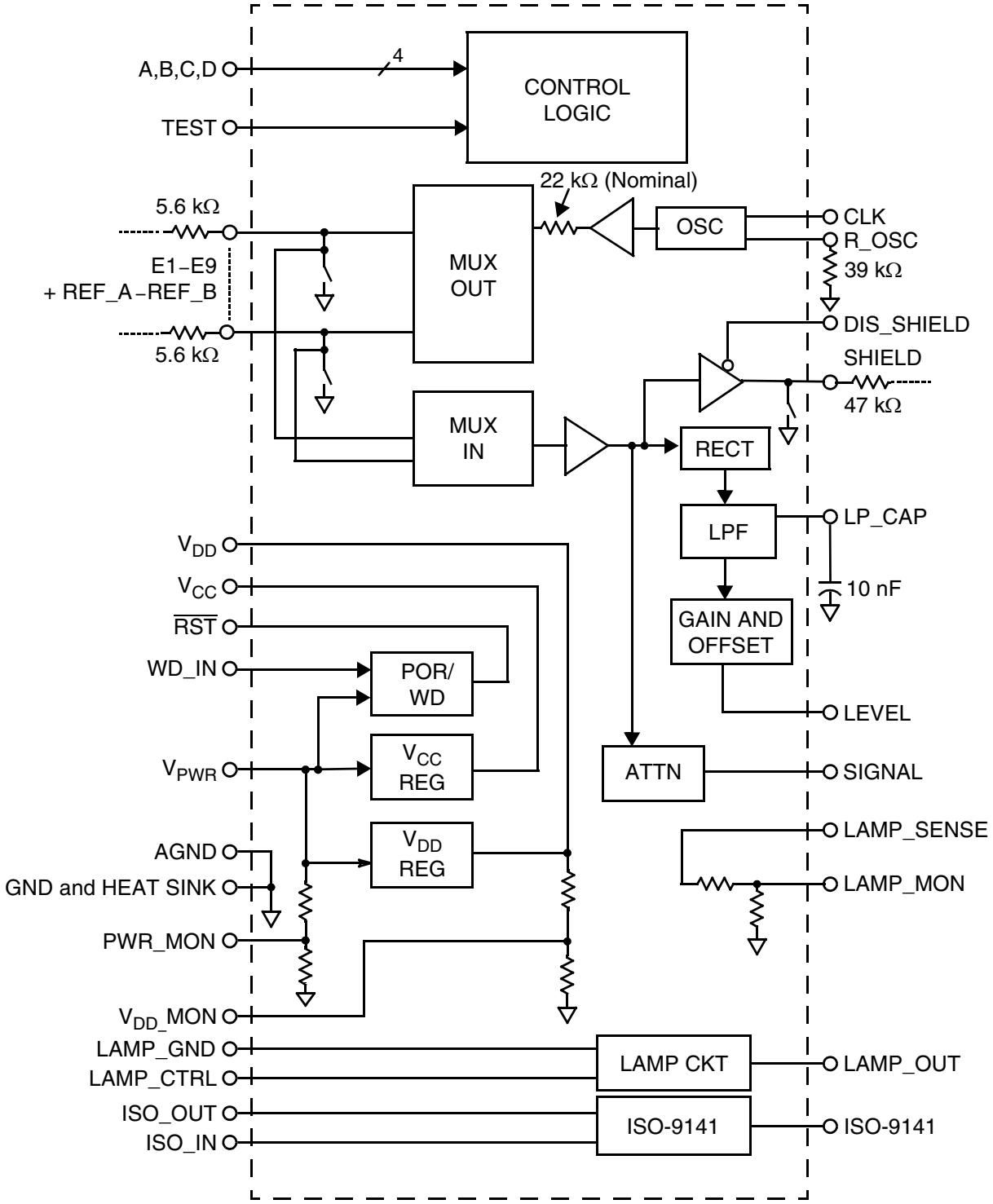
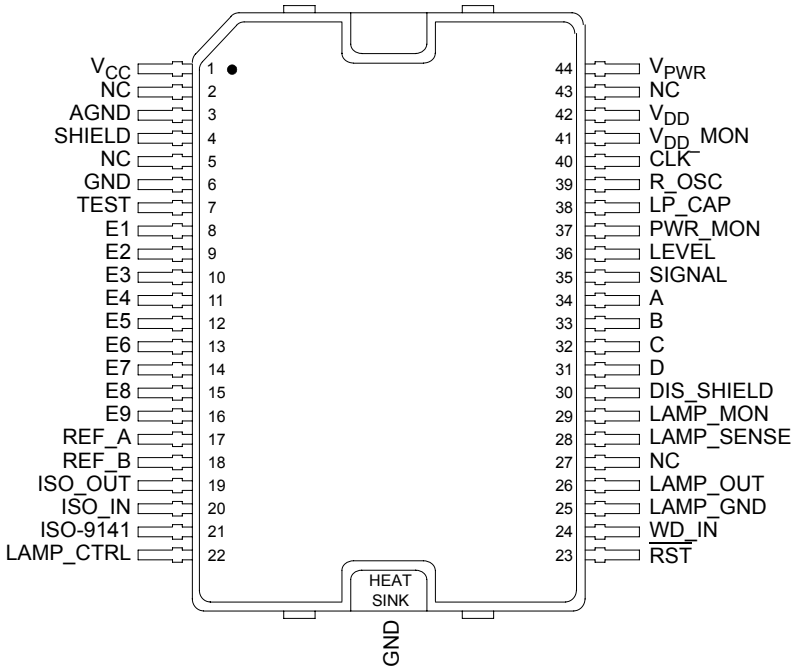


Figure 1. 33794 Simplified Internal Block Diagram



HSOP PIN FUNCTION DESCRIPTION

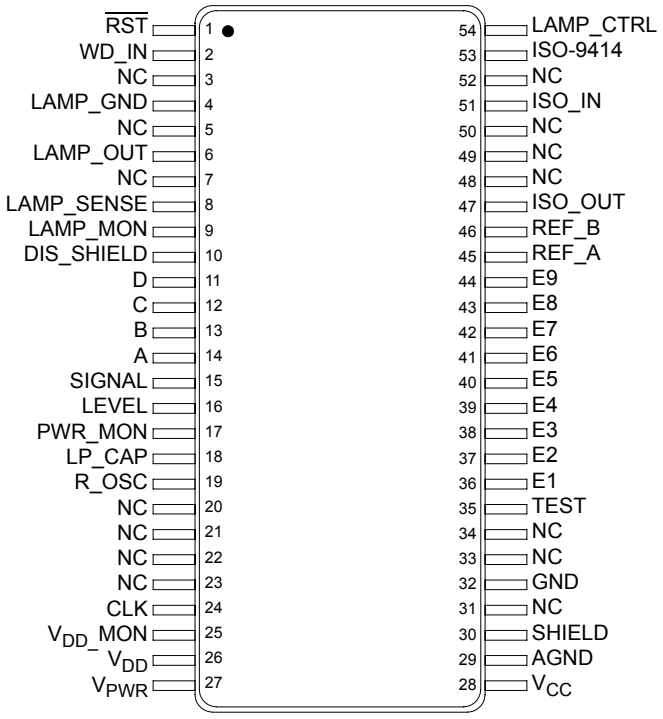
Pin	Pin Name	Formal Name	Definition
1	V_{CC}	5.0 V Regulator Output	This output pin requires a 47 μF capacitor and provides a regulated 5.0 V for the MCU and for internal needs of the 33794.
2, 5, 27, 43	NC	No connect	These pins may be used at some future date and should be left open.
3	AGND	Analog Ground	This pin is connected to the ground return of the analog circuitry. This ground should be kept free of transient electrical noise like that from logic switching. Its path to the electrical current return point should be kept separate from the return for GND.
4	SHIELD	Shield Driver	This pin connects to cable shields to cancel cable capacitance.
6, Heat Sink	GND	Ground	This pin and metal backing is the IC power return and thermal radiator/conductor.
7	TEST	Test Mode Control	This pin is normally connected to circuit ground. There are special operating modes associated with this pin when it is not at ground.
8–16	E1–E9	Electrode Connections	These are the electrode pins. They are connected either directly or through coaxial cables to the electrodes for measurements. One of these electrodes can be selected at a time for capacitance measurement. All of the other unselected electrodes are grounded by an internal switch. The signal at the selected electrode pin is routed to the shield driver amplifier by an internal switch. All of the coaxial cable shields should be isolated from ground and connected SHIELD.
17, 18	REF_A, REF_B	Reference Connections	These pins can be individually selected like E1 through E9. Unlike E1 through E9, these pins are not grounded when not selected. The purpose of these pins is to allow known capacitors to be measured. By using capacitors at the low and high end of the expected range, absolute values for the capacitance on the electrodes can be computed.
19	ISO_OUT	ISO-9141 Output	This pin translates ISO-9141 receive levels to 5.0 V logic levels for the MCU.
20	ISO_IN	ISO-9141 Input	This pin accepts data from the MCU to be sent over the ISO-9141 communications interface. It translates the 5.0 V logic levels from the MCU to transmit levels on the ISO-9141 bus.

HSOP PIN FUNCTION DESCRIPTION (continued)

Pin	Pin Name	Formal Name	Definition
21	ISO-9141	ISO-9141 Bus	This pin connects to the ISO-9141 bus. It provides the drive and detects signaling on the bus and translates it from the bus level to logic levels for the MCU.
22	LAMP_CTRL	Lamp Control	This signal is used to control the lamp driver. A high logic level turns on the lamp
23	$\overline{RST}$	Reset	This output is intended to generate the reset function of a typical MCU. It has a delay for Power-ON Reset, level detectors to force a reset when V_{CC} is out-of-range high or low, and a watchdog timer that will force a reset if WD_IN is not asserted at regular intervals. Timing is derived from the oscillator and will change with changes in the resistor attached to R_OSC.
24	WD_IN	Watchdog Input	This pin must be asserted and deasserted at regular interval in order to prevent $\overline{RST}$ from being asserted. By having the MCU program perform this operation more often the allowed time, a check that the MCU is running and executing its program is assured. If this doesn't occur, the MCU will be reset. If the watchdog function is not desired, this pin may be connected to CLK to prevent a reset from being issued.
25	LAMP_GND	Lamp Ground	This is the ground for the current from the lamp. The current into LAMP_OUT flows out through this pin.
26	LAMP_OUT	Lamp Driver	This is an active low output capable of sinking current of a typical indicator lamp. One end of the lamp should be connected to a positive supply (for example, battery voltage) and the other side to this pin. The current is limited to prevent damage to the IC in the case of a short or surge during lamp turn-on or burn-out.
28	LAMP_SENSE	Lamp Sense	This pin is normally connected to the LAMP_OUT pin. The voltage at this pin is reduced and sent to LAMP_MON so the voltage at the lamp pin is brought into the range of the analog-to-digital converter (ADC) in the MCU.
29	LAMP_MON	Lamp Monitor	This pin is connected through a voltage divider to the LAMP_SENSE pin. The voltage divider scales the voltage at this pin so that battery voltage present when the lamp is off is scaled to the range of the MCU ADC. With the lamp off, this pin will be very close to battery voltage if the lamp is not burned out and the pin is not shorted to ground. This is useful as a lamp check.
30	DIS_SHIELD	Shield Driver Disable	This pin is used to turn off the shield signal. The purpose of doing this is to be able to detect that the shield signal is not working or the connection to the coax shields is broken. If either of these conditions exists, there will be little or no change in the capacitance measured when the DIS_SHIELD is asserted. If the SHIELD output is working and properly connected, the capacitance of the coax will not be cancelled when this pin is asserted and the measured capacitance will appear to change by approximately the capacitance between the center conductor and the shield in the coax.
34–31	A, B, C, D	Selector Inputs	These input pins control which electrode or reference is active. Selection values are shown in Table 1, Electrode Selection, page 14.
35	SIGNAL	Undetected Signal	This is the undetected signal being applied to the detector. It has a DC level with the low radio frequency signal superimposed on it. Care must be taken to minimize DC loading of this signal. A shift of DC will change the center point of the signal and adversely affect the detection of the signal.
36	LEVEL	Detected Level	This is the detected, amplified, and offset representation of the signal voltage on the selected electrode. Filtering of the rectified signal is performed by a capacitor attached to LP_CAP.
37	PWR_MON	Power Monitor	This is connected through a voltage divider to V_{PWR}. It allows reduction of the voltage so it will fall within the range of the ADC on the MCU.
38	LP_CAP	Low-Pass Filter Capacitor	A capacitor on this pin forms a low pass filter with the internal series resistance from the detector to this pin. This pin can be used to determine the detected level before amplification or offset is applied. A 10 nF capacitor connected to this pin will smooth the rectified signal. More capacitance will increase the response time unnecessarily.

HSOP PIN FUNCTION DESCRIPTION (continued)

Pin	Pin Name	Formal Name	Definition
39	R_OSC	Oscillator Resistor	A resistor from this pin to circuit ground determines the operating frequency of the oscillator. The 33794 is optimized for operation around 120 kHz.
40	CLK	Clock	This pin provides a square wave output at the same frequency as the internal oscillator. The edges of the square wave coincide with the peaks (positive and negative) of the sine wave.
41	V_{DD}_MON	V_{DD} Monitor	This is connected through a voltage divider to V_{DD}. It allows reduction of the voltage so it will fall within the range of the ADC on the MCU.
42	V_{DD}	V_{DD} Capacitor	A capacitor is connected to this pin to filter the internal analog regulated supply. This supply is derived from V_{PWR}.
44	V_{PWR}	Positive Power Supply Input	12 V power applied to this pin will be converted to the regulated voltages needed to operate the part. It is also converted to 5.0 V (V_{CC}) and 8.5 V (V_{DD}) to power the MCU and external devices.



SOICW-EP PIN FUNCTION DESCRIPTION

Pin	Pin Name	Formal Name	Definition
1	$\overline{\text{RST}}$	Reset	This output is intended to generate the reset function of a typical MCU. It has a delay for Power-ON Reset, level detectors to force a reset when V_{CC} is out-of-range high or low, and a watchdog timer that will force a reset if WD_IN is not asserted at regular intervals. Timing is derived from the oscillator and will change with changes in the resistor attached to R_OSC.
2	WD_IN	Watchdog In	This pin must be asserted and deasserted at regular interval in order to prevent $\overline{\text{RST}}$ from being asserted. By having the MCU program perform this operation more often the allowed time, a check that the MCU is running and executing its program is assured. If this doesn't occur, the MCU will be reset. If the watchdog function is not desired, this pin may be connected to CLK to prevent a reset from being issued.
3, 5, 7, 20–23, 31, 33, 34, 48–50, 52	NC	No connect	These pins may be used at some future date and should be left open.
4	LAMP_GND	Lamp Ground	This is the ground for the current from the lamp. The current into LAMP_OUT flows out through this pin.
6	LAMP_OUT	Lamp Driver	This is an active low output capable of sinking current of a typical indicator lamp. One end of the lamp should be connected to a positive supply (for example, battery voltage) and the other side to this pin. The current is limited to prevent damage to the IC in the case of a short or surge during lamp turn-on or burn-out.
8	LAMP_SENSE	Lamp Sense	This pin is normally connected to the LAMP_OUT pin. The voltage at this pin is reduced and sent to LAMP_MON so the voltage at the lamp pin is brought into the range of the analog-to-digital converter (ADC) in the MCU.
9	LAMP_MON	Lamp Monitor	This pin is connected through a voltage divider to the LAMP_SENSE pin. The voltage divider scales the voltage at this pin so that battery voltage present when the lamp is off is scaled to the range of the MCU ADC. With the lamp off, this pin will be very close to battery voltage if the lamp is not burned out and the pin is not shorted to ground. This is useful as a lamp check.

SOICW-EP PIN FUNCTION DESCRIPTION (continued)

Pin	Pin Name	Formal Name	Definition
10	DIS_SHIELD	Shield Driver	This pin is used to turn off the shield signal. The purpose of doing this is to be able to detect that the shield signal is not working or the connection to the coax shields is broken. If either of these conditions exists, there will be little or no change in the capacitance measured when the DIS_SHIELD is asserted. If the SHIELD output is working and properly connected, the capacitance of the coax will not be cancelled when this pin is asserted and the measured capacitance will appear to change by approximately the capacitance between the center conductor and the shield in the coax.
14–11	A, B, C, D	Selector Inputs	These input pins control which electrode or reference is active. Selection values are shown in Table 1, Electrode Selection, page 14.
15	SIGNAL	Undetected Signal	This is the undetected signal being applied to the detector. It has a DC level with the low radio frequency signal superimposed on it. Care must be taken to minimize DC loading of this signal. A shift of DC will change the center point of the signal and adversely affect the detection of the signal.
16	LEVEL	Detected Level	This is the detected, amplified, and offset representation of the signal voltage on the selected electrode. Filtering of the rectified signal is performed by a capacitor attached to LP_CAP.
17	PWR_MON	Power Monitor	This is connected through a voltage divider to V_{PWR}. It allows reduction of the voltage so it will fall within the range of the ADC on the MCU.
18	LP_CAP	Low-Pass Filter Capacitor	A capacitor on this pin forms a low pass filter with the internal series resistance from the detector to this pin. This pin can be used to determine the detected level before amplification or offset is applied. A 10 nF capacitor connected to this pin will smooth the rectified signal. More capacitance will increase the response time unnecessarily.
19	R_OSC	Oscillator Resistor	A resistor from this pin to circuit ground determines the operating frequency of the oscillator. The 33794 is optimized for operation around 120 kHz.
24	CLK	Clock	This pin provides a square wave output at the same frequency as the internal oscillator. The edges of the square wave coincide with the peaks (positive and negative) of the sine wave.
25	V_{DD}_MON	V_{DD} Monitor	This is connected through a voltage divider to V_{DD}. It allows reduction of the voltage so it will fall within the range of the ADC on the MCU.
26	V_{DD}	V_{DD} Capacitor	A capacitor is connected to this pin to filter the internal analog regulated supply. This supply is derived from V_{PWR}.
27	V_{PWR}	Positive Power Supply	12 V power applied to this pin will be converted to the regulated voltages needed to operate the part. It is also converted to 5.0 V (V_{CC}) and 8.5 V (V_{DD}) to power the MCU and external devices.
28	V_{CC}	5.0 V Regulator Output	This output pin requires a 47 μF capacitor and provides a regulated 5.0 V for the MCU and for internal needs of the 33794.
29	AGND	Analog Ground	This pin is connected to the ground return of the analog circuitry. This ground should be kept free of transient electrical noise like that from logic switching. Its path to the electrical current return point should be kept separate from the return for GND.
30	SHIELD	Shield Driver	This pin connects to cable shields to cancel cable capacitance.
32	GND	Ground	This pin and metal backing is the IC power return and thermal radiator/conductor.
35	TEST	Test Mode Control	This pin is normally connected to circuit ground. There are special operating modes associated with this pin when it is not at ground.

SOICW-EP PIN FUNCTION DESCRIPTION (continued)

Pin	Pin Name	Formal Name	Definition
36–44	E1–E9	Electrode Connections	These are the electrode pins. They are connected either directly or through coaxial cables to the electrodes for measurements. One of these electrodes can be selected at a time for capacitance measurement. All of the other unselected electrodes are grounded by an internal switch. The signal at the selected electrode pin is routed to the shield driver amplifier by an internal switch. All of the coaxial cable shields should be isolated from ground and connected SHIELD.
45, 46	REF_A, REF_B	Reference Connections	These pins can be individually selected like E1 through E9. Unlike E1 through E9, these pins are not grounded when not selected. The purpose of these pins is to allow known capacitors to be measured. By using capacitors at the low and high end of the expected range, absolute values for the capacitance on the electrodes can be computed.
47	ISO_OUT	ISO-9141 Output	This pin translates ISO-9141 receive levels to 5.0 V logic levels for the MCU.
51	ISO_IN	ISO-9141 Input	This pin accepts data from the MCU to be sent over the ISO-9141 communications interface. It translates the 5.0 V logic levels from the MCU to transmit levels on the ISO-9141 bus.
53	ISO-9141	ISO-9141 Bus	This pin connects to the ISO-9141 bus. It provides the drive and detects signaling on the bus and translates it from the bus level to logic levels for the MCU.
54	LAMP_CTRL	Lamp Control	This signal is used to control the lamp driver. A high logic level turns on the lamp.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Peak V_{PWR} Voltage	V_{PWRPK}	40	V
Double Battery 1 Minute Maximum T_A = 30°C	V_{DBLBAT}	 26.5	V
ESD Voltage Human Body Model (Note 1) Machine Model (Note 2)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Ambient Temperature	T_A	-40 to 85	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Thermal Resistance Junction-to-Ambient (Note 3) Junction-to-Case (Note 4) Junction-to-Board (Note 5)	 $R_{\theta J-A}$ $R_{\theta J-C}$ $R_{\theta J-B}$	 41 0.2 3.0	°C/W
Lead Soldering Temperature (for 10 Seconds)	T_{SOLDER}	260	°C

Notes

1. ESD1 performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
2. ESD2 performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. In accordance with SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MILSPEC 883 Method 1012.1) with the cold plate temperature used for the case temperature.
5. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under condition -40°C ≤ T_J ≤ 150°C. Voltages are relative to GND unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATORS					
5.0 V Regulator Voltage 7.0 V ≤ V_{PWR} ≤ 18 V, 1.0 mA ≤ I_L ≤ 75 mA, C_{FILT} = 47 μF	V_{CC}	4.75	5.0	5.25	V
Analog Regulator Voltage 9.0 V ≤ V_{PWR} ≤ 18 V, C_{FILT} = 47 μF	V_{ANALOG}	8.075	8.5	8.925	V
V_{CC} OUT-OF-RANGE VOLTAGE DETECTOR					
5.0 V Low Voltage Detector	V_{LV5}	4.0	4.52	4.72	V
5.0 V High Voltage Detector	V_{HV5}	5.26	5.55	5.83	V
5.0 V Out-of-Range Voltage Detector Hysteresis	V_{HYS5}	–	0.05	–	V
ISO-9141 COMMUNICATIONS INTERFACE					
Input Low Level (Note 6)	VIF_{INLO}	0.30	0.33	–	V/V
Input High Level (Note 6)	VIF_{INHI}	–	0.53	0.7	V/V
Input Hysteresis (Note 6)	VIF_{INHYS}	–	0.2	–	V/V
Output Low (Note 6)	VIF_{OLO}	–	–	0.2	V/V
Output High (Note 6)	VIF_{OHI}	0.8	–	–	V/V
Output Breakdown I_{OUT} = 20 mA	VIF_Z	40	–	–	V
Output Resistance I_{OUT} = 40 mA	RIF_{ON}	–	58	–	Ω
Current Limit Sinking Current with V_{OUT} < 0.3 $V_{PWR\ IN}$	IIF_{LIM}	60	90	120	mA
Output Propagation Delay Out to ISO-9141, C_{LOAD} = 20 pF	TIF_{DLY}	–	–	8.0	μs
ISO IN					
Logic Output Low I_{SINK} = 1.0 mA	VIF_{OLO}	–	–	1.0	V
Logic Output Pull-Up Current V_{OUT} = 0 V	IIF_{PU}	100	–	–	μA
Input to Output Propagation Delay ISO-9141 to ISO_IN, R_L = 10 kΩ, C_L = 470 pF, 7.0 V ≤ V_{PWR} ≤ 18 V	TIF_{DLY}	–	–	5.4	μs

Notes

6. Ratio to V_{PWR}.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under condition -40°C ≤ T_J ≤ 150°C. Voltages are relative to GND unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ELECTRODE SIGNALS					
Total Variance Between Electrode Measurements (Note 7) All C_{LOAD} = 15 pF	ELV_{VAR}	–	–	3.0	%
Electrode Maximum Harmonic Level Below Fundamental (Note 8) 5.0 pF ≤ C_{LOAD} ≤ 100 pF	EL_{HARM}	–	-20	–	dB
Electrode Transmit Output Range 5.0 pF ≤ C_{LOAD} ≤ 100 pF	EL_{TXV}	1.0	–	8.0	V
Receive Input Voltage Range	RX_V	0	–	9.0	V
Grounding Switch on Voltage I_{SW} = 1.0 mA	SW_{VON}	–	–	5.0	V
SHIELD DRIVER					
Shield Driver Output Level 0 pF ≤ C_{LOAD} ≤ 500 pF	SD_{TXV}	1.0	–	8.0	V
Shield Driver Input Range	SD_{IN}	0	–	9.0	V
Grounding Switch on Voltage (Note 9)	SW_{VON}	–	–	1.5	V
LOGIC I/O					
CMOS Logic Input Low Threshold	V_{THL}	0.3	–	–	V_{CC}
Logic Input High Threshold	V_{THH}	–	–	0.7	V_{CC}
Voltage Hysteresis	V_{HYS}	–	0.06	–	V_{CC}
Input Current V_{IN} = V_{CC} V_{IN} = 0 V	I_{IN}	10 -5.0	– –	50 5.0	μA
SIGNAL DETECTOR					
Detector Output Resistance	DET_{RO}	–	50	–	kΩ
LP_CAP to LEVEL Gain	A_{REC}	3.6	4.0	4.4	A_V
LP_CAP to LEVEL Offset	V_{RECOFF}	-3.3	-3.0	-2.7	V

Notes

7. Verified by design. Not tested in production.
8. Verified by design and characterization. Not tested in production.
9. Current into grounded pin under test = 1.0 mA.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under condition -40°C ≤ T_J ≤ 150°C. Voltages are relative to GND unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LAMP DRIVER					
On Resistance I_{IN} = 400 mA	RLD_{DSON}	–	1.75	3.5	Ω
Current Limit V_{OUT} = 1.0 V	ILD_{LIM}	0.7	–	1.7	A
On-Voltage I_{OUT} = 400 mA	VLD_{ON}	–	–	1.4	V
Breakdown Voltage I_{OUT} = 100 μA, Lamp Off	VLD_Z	40	–	–	V
VOLTAGE MONITORS					
LAMP_MON to LAMP_SENSE Ratio	LMP_{MON}	0.1950	0.20524	0.2155	V/V
PWR_MON to V_{PWR} Ratio	PWR_{MON}	0.2200	0.2444	0.2688	V/V
V_{DD}_MON to V_{DD} Ratio	V_{DDMON}	0.45	0.5	0.55	V/V

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under condition -40°C ≤ T_J ≤ 150°C. Voltages are relative to GND unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OSC					
OSC Frequency Stability (Note 10), (Note 11)	f_{STAB}	–	–	10	%
OSC Center Frequency R_OSC = 39 kΩ	f_{OSC}	– –	120 –	–	kHz
Harmonic Content (Note 10) 2nd through 4th Harmonic Level 5th and Higher	$OSCH_{ARM}$	– –	– –	-20 -60	dB
SHIELD DRIVER					
Shield Driver Maximum Harmonic level below Fundamental (Note 10) 10 pF ≤ C_{LOAD} ≤ 500 pF	SD_{HARM}	–	-20	–	dB
Shield Driver Gain Bandwidth Product (Note 10) Measured at 120 kHz	SD_{GBW}	–	4.5	–	MHz
POR					
POR Time-Out Period	t_{PER}	9.0	–	50	ms
WATCHDOG					
Watchdog Time-Out Period	t_{WDPER}	50	68	250	ms
Watchdog Reset Hold Time	t_{WDHLD}	9.0	–	50	ms
LAMP DRIVER					
Short Circuit to Battery Survival Time	t_{SCB}	3.0	–	–	ms

Notes

10. Verified by design and characterization. Not tested in production.
11. Does not include errors in external reference parts.

Table 1. Electrode Selection

PIN/SIGNAL	D	C	B	A
Source (internal)	0	0	0	0
E1	0	0	0	1
E2	0	0	1	0
E3	0	0	1	1
E4	0	1	0	0
E5	0	1	0	1
E6	0	1	1	0
E7	0	1	1	1
E8	1	0	0	0
E9	1	0	0	1
REF_A	1	0	1	0
REF_B	1	0	1	1
Internal OSC	1	1	0	0
Internal OSC after 22 kΩ	1	1	0	1
Internal Ground	1	1	1	0
Reserved	1	1	1	1

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33794 is intended for use in detecting objects using an electric field. The IC generates a low radio frequency sine wave. The frequency is set by an external resistor and is optimized for 120 kHz. The sine wave has very low harmonic content to reduce potential interference at higher harmonically related frequencies. The internal generator produces a nominal 5.0 V peak-to-peak output that is passed through an internal resistor of about 22 kΩ. An internal multiplexer routes the signal to one of 11 pins under control of the ABCD input pins. A receiver multiplexer simultaneously connected to the selected electrode routes its signal to a detector, which converts the sine wave to a DC level. This DC level is filtered by an external capacitor and is multiplied and offset to increase sensitivity. All of the unselected electrode outputs are grounded by the device. The current flowing between the selected electrode and the other grounded electrodes plus other grounded objects around the electrode causes a voltage drop across the internal resistance. Objects brought into or out of the electric field change the current and resulting voltage at the IC pin, which in turn reduces the voltage at LP_CAP and LEVEL.

A shield driver is included to minimize the effect of capacitance caused by using coaxial cables to connect to remote electrodes. By driving the coax shield with this signal, the shield voltage follows that of the center conductor, significantly reducing the effective capacitance of the coax and maintaining sensitivity to the capacitance at the electrode.

The 33794 is made to work with and support a microcontroller. It provides two voltage regulators, a Power-ON-reset/out-of-range voltage detector, watchdog circuit, lamp driver and sense circuit, and a physical layer ISO-9141 communications interface.

BLOCK DIAGRAM COMPONENTS

Refer to Figure 1, 33794 Internal Block Diagram, page 2, for a graphic representation of the block diagram information in this section.

OSC

This section generates a high purity sine wave. The center frequency is controlled by a resistor attached to R_OSC. The normal operating frequency is around 120 kHz. A square wave version of the frequency output is available at CLK. Timing for the Power-ON Reset and watchdog (POR/WD) circuit are derived from this oscillator's frequency.

MUX OUT

This circuit directs the output of the sine wave to one of nine possible electrode outputs or two reference pins. All unused pins are automatically grounded. The selected output is controlled by the ABCD inputs.

MUX IN

This circuit connects the selected electrode, reference, or one of two internal nodes to an amplifier/detector. The selection is controlled by the ABCD inputs and follows the driven electrode/reference when one is selected.

RECT

The rectifier circuit detects the level from MUX IN by offsetting the midpoint of the sine wave to zero volts and inverting the waveform when it is below the midpoint. It is important to avoid DC loading of the signal, which would cause a shift in the midpoint voltage of the signal from the MUX IN.

LPF

The rectified sine wave is filtered by a low pass function in the LPF formed by an internal resistance and an external capacitance attached to LP_CAP. The nominal value of the internal resistance is 50 kΩ. The value of the external capacitor is selected to provide filtering of noise while still allowing the desired settling time for the detector output. A 10 nF capacitor would allow 99% settling in less than 5.0 ms.

GAIN and OFFSET

This circuit multiplies the detected and filtered signal by a gain and offsets the result by a DC level. This results in an output range that covers 1.0 V to 4.0 V for capacitive loading of the field in the range of 10 pF to 100 pF. This allows higher sensitivity for a digital-to-analog converter with a 0 V-to-5.0 V input range.

ATTN

This circuit passes the undetected signal to SIGNAL for external use.

LAMP CKT

This section controls the operation of the LAMP_OUT pin. When LAMP_CTRL is asserted, LAMP_OUT is pulled to LAMP_GND. If one side of an indicator lamp or LED (with appropriate current setting resistor) is connected to a positive voltage source and the other is connected to LAMP_OUT, and LAMP_GND is connected to ground, the lamp will light. This circuit provides current limiting to prevent damage to itself in the case of a shorted lamp or during a high-surge condition typical of an incandescent lamp burnout.

ISO-9141

This circuit connects to an ISO-9141 bus to allow remote communications. ISO_IN is data from the bus to the MCU and ISO_OUT is data to drive onto the bus from the MCU.

POR/WD

This circuit is a combined Power-ON Reset and watchdog timer. The $\overline{RST}$ output is held low until a certain amount of time after the V_{CC} output has remained above a minimum operating threshold. If V_{CC} falls below the level at any time, $\overline{RST}$ is pulled low again and held until the required time after V_{CC} has returned high. An overvoltage circuit is also included, which will force a reset if V_{CC} rises above a maximum voltage. The watchdog function also can force $\overline{RST}$ low if too long an interval is allowed to pass between positive transitions on WD_IN.

V_{CC} REG

This circuit converts an unregulated voltage from VIN to a regulated 5.0 V source, which is used internally and available for other components requiring a regulated voltage source.

V_{DD} REG

This is a regulator for analog devices that require more than 5.0 V. This is used by the device and some current is available to operate op-amps and other devices. By having this higher voltage available, some applications can avoid the need for a rail-to-rail output amplifier and still achieve the 0 V-to-5.0 V output for a digital-to-analog converter input. V_{DDMON} is a divided output from V_{DD}, which allows a 0 V-to-5.0 V ADC to measure V_{DD}.

CONTROL LOGIC

This contains the logic that decodes and controls the MUXes and some of the test modes.

APPLICATION INFORMATION

The 33794 is intended to be used where an object's size and proximity are to be determined. This is done by placing electrodes in the area where the object will be. The proximity of an object to an electrode can be determined by the increase in effective capacitance as the object gets closer to the electrode and modifies the electric field between the electrode and surrounding electrically common objects. The shape and size of an object can be determined by using multiple electrodes over an area and observing the capacitance change on each of the electrodes. Those that don't change have nothing near them, and those that do change have part of the object near them.

The voltage measured is an inverse function of the capacitance between the electrode being measured and the surrounding electrodes and other objects in the electric field surrounding the electrode. Increasing capacitance results in decreasing voltage. The value of series resistance (22 kΩ) was chosen to provide a nearly linear relationship at 120 kHz over a range of 10 pF to 100 pF.

The measured value will change with any change in frequency, series resistance, driving voltage, or detector sensitivity. These can change with temperature and time. The proper use of REF_A and REF_B will allow much of the changes to be compensated for.

A typical measurement algorithm would start by measuring the voltage for two known value capacitors (attached to REF_A and REF_B). The value of these capacitors would be chosen to be near the minimum and maximum values of capacitance expected to be seen at the electrodes. These reference voltages and the known capacitance values are then used with the electrode measurement voltage to determine the capacitance seen by the electrode. This method can be used to detect short- and long-term changes due to objects in the electric field and significantly reduce the effect of temperature- and time-induced changes.

The 33794 does not contain an ADC. It is intended to be used with an MCU that contains one. Offset and gain have been added to the 33794 to maximize the sensitivity over the range of 0 pF to 100 pF. An 8-bit ADC can resolve around 0.4 pF of change and a 10-bit converter around 0.1 pF. Higher resolution results in more distant detection of smaller objects.

DC loading on the electrodes should be avoided. The signal is generated with a DC offset that is more than half the peak-to-peak level. This keeps the signal positive above ground at all times. The detector uses this voltage level as the midpoint for detection. All signals below this level are inverted and added to all signals above this level. Loading of the DC level will cause some of the positive half of the signal to be inverted and added and will change the measurement.

If it is not possible to assure that the electrodes will always have a high DC resistance to ground or a voltage source, a series capacitor of about 10 nF should be connected between the IC electrode pins and the electrodes.

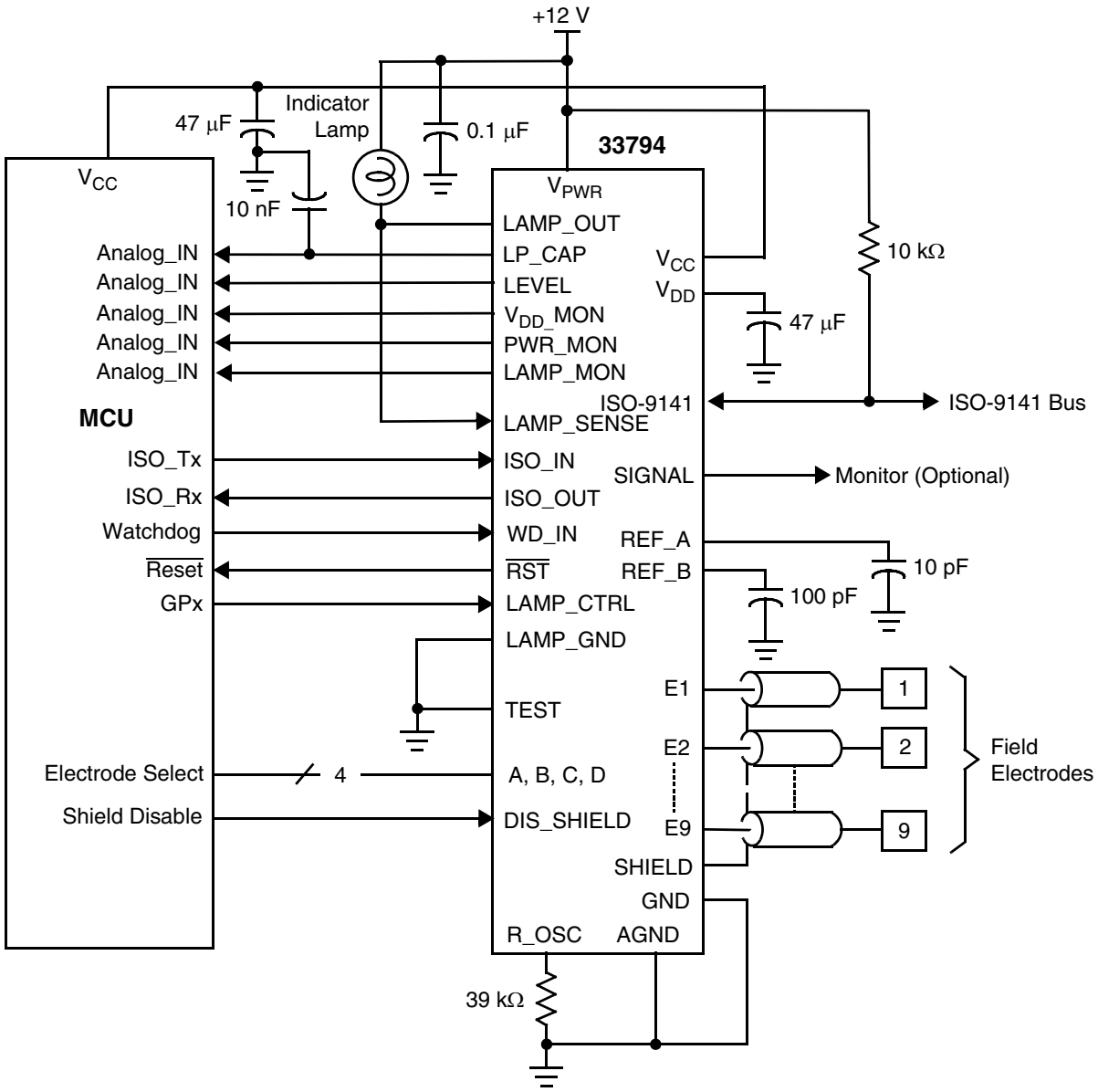
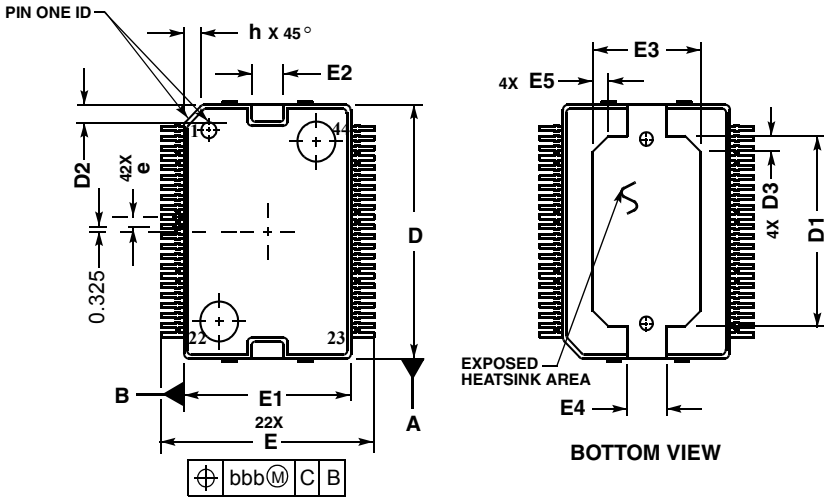
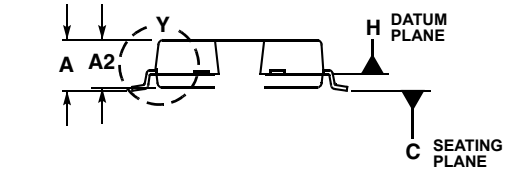


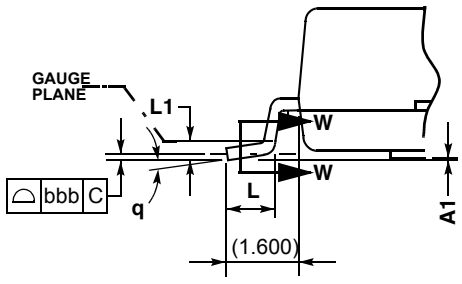
Figure 2. Typical Application Diagram

PACKAGE DIMENSIONS

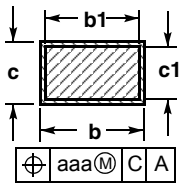
DH SUFFIX
44-LEAD HSOP
PLASTIC PACKAGE
CASE 1291-01
ISSUE O







DETAIL Y

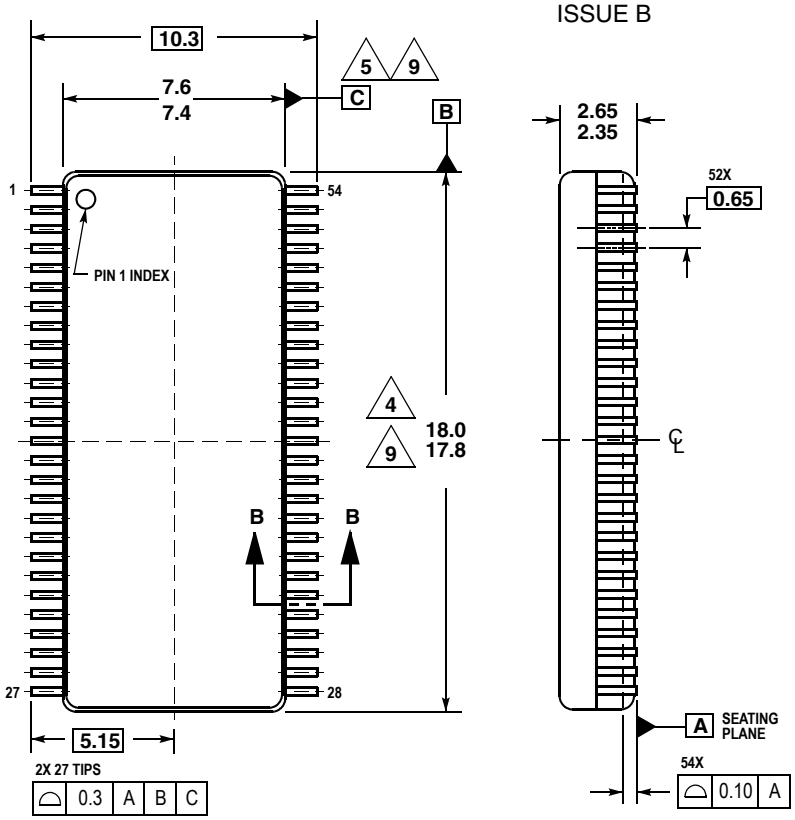


SECTION W-W

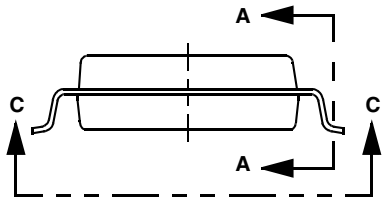
NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

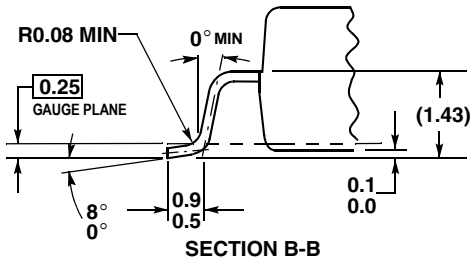
	MILLIMETERS	
DIM	MIN	MAX
A	3.000	3.400
A1	0.025	0.125
A2	2.900	3.100
D	15.800	16.000
D1	11.700	12.600
D2	0.900	1.100
D3	---	1.000
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	6.400	7.300
E4	2.700	2.900
E5	---	1.000
L	0.840	1.100
L1	0.350 BSC	
b	0.220	0.350
b1	0.220	0.320
c	0.230	0.320
c1	0.230	0.280
e	0.650 BSC	
h	---	0.800
q	0°	8°
aaa	0.200	
bbb	0.100	

DWB SUFFIX
54-LEAD SOICW-EP
PLASTIC PACKAGE
CASE 1390-01
ISSUE B

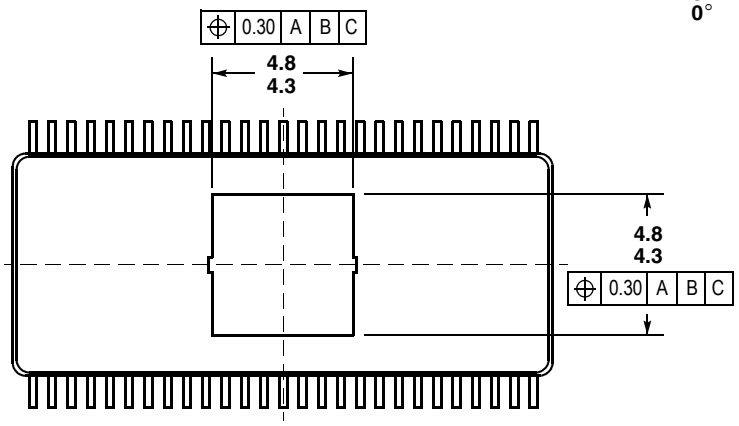


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

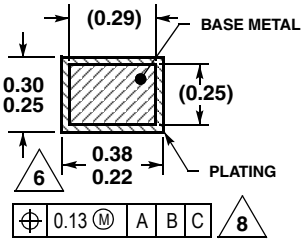




SECTION B-B



VIEW C-C



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