LP3982 Micropower, Ultra Low-Dropout, Low-Noise, 300 mA CMOS Regulator

Check for Samples: LP3982

FEATURES

- **MAX8860 Pin, Package and Spec. Compatible**
- **WSON Space Saving Package**
- **300 mA Output Current**
- **120 mV Typical Dropout @ 300 mA**
- **90 µA Typical Quiescent Current**
- **1 nA Typical Shutdown Mode**
- **60 dB Typical PSRR**
- **2.5V to 6V Input Range**
- **120µs Typical Turn-on Time**
- **Stable with Small Ceramic Output Capacitors**
- **37 µV RMS Output Voltage Noise (10 Hz to 100 kHz)**
- **Over-Temperature/Over-Current Protection**
- **±2% Output Voltage Tolerance**

APPLICATIONS

- **Wireless Handsets**
- **DSP Core Power**
- **Battery Powered Electronics**
- **Portable Information Appliances**

DESCRIPTION

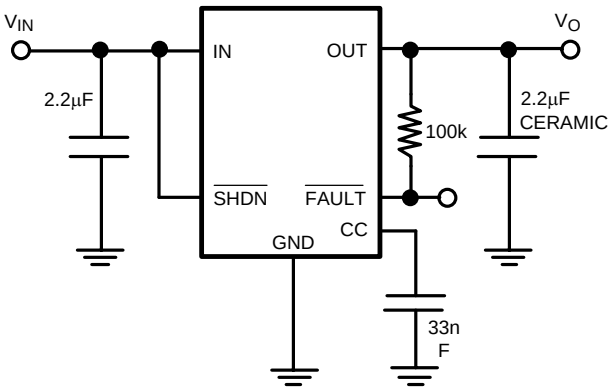
The LP3982 low-dropout (LDO) CMOS linear regulator is available in 1.8V, 2.5V, 2.77V, 2.82V, 3.0V, 3.3V, and adjustable versions. They deliver 300 mA of output current. Packaged in an 8-Pin VSSOP, the LP3982 is pin and package compatible with Maxim's MAX8860. The LM3982 is also available in the small footprint WSON package.

The LP3982 suits battery-powered applications because of its shutdown mode (1nA typ), low quiescent current (90 µA typ), and LDO voltage (120 mV typ). The low dropout voltage allows for more utilization of a battery's available energy by operating closer to its end-of-life voltage. The LP3982's PMOS output transistor consumes relatively no drive current compared to PNP LDO regulators.

This PMOS regulator is stable with small ceramic capacitive loads (2.2 µF typ).

These devices also include regulation fault detection, a bandgap voltage reference, constant current limiting and thermal overload protection.

Application Circuit



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

V_{IN}, V_{OUT}, $V_{\overline{SHDN}}$, V_{SET}, V_{CC}, $V_{\overline{FAULT}}$		−0.3V to 6.5V
Fault Sink Current		20mA
Power Dissipation		See(4)
Storage Temperature Range		−65°C to 160°C
Junction Temperature (T_J)		150°C
Lead Temperature (10 sec.)		260°C
ESD Rating	Human Body Model(5)	2kV
	Machine Model	200V
Thermal Resistance (θ_{JA})	8-Pin VSSOP	223°C/W
	8-Pin WSON	See(4)

(1) Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the ground pin.
(3) If Military/Aerospace specified devices are required, please contact Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Maximum Power dissipation for the device is calculated using the following equations: $P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$ where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. For example, for the VSSOP-8 package θ_{JA} = 223°C/W, $T_{J(MAX)}$ = 150°C and using T_A = 25°C; the maximum power dissipation is found to be 561 mW. The derating factor ($-1/\theta_{JA}$) = −4.5 mW/°C, thus below 25°C the power dissipation figure can be increased by 4.5 mW per degree, and similarity decreased by this factor for temperatures above 25°C. The value of the θ_{JA} for the WSON package is specifically dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 SNOA401.
(5) Human body model: 1.5 kΩ in series with 100 pF.

RECOMMENDED OPERATING CONDITIONS(1)(2)

Temperature Range	−40°C to 85°C
Supply Voltage	2.5V to 6.0V

(1) Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the ground pin.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for $V_{IN} = V_O + 0.5V$(1), $V_{\overline{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$. **Boldface** limits apply for the operating temperature extremes: −40°C and 85°C.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{IN}	Input Voltage		**2.5**		**6.0**	V
ΔV_O	Output Voltage Tolerance	100 µA ≤ I_{OUT} ≤ 300 mA $V_{IN} = V_O + 0.5V$(1) SET = OUT for the Adjust Versions	−2		+2	% of V_{OUT} (NOM)
			−3		**+3**	
V_O	Output Adjust Range	Adjust Version Only	**1.25**		**6**	V
I_O	Maximum Output Current	Average DC Current Rating	**300**			mA
I_{LIMIT}	Output Current Limit		**330**	770		mA
I_Q	Supply Current	I_{OUT} = 0mA		90	**270**	µA
		I_{OUT} = 300 mA		225		
	Shutdown Supply Current	V_O = 0V, $\overline{SHDN}$ = GND		0.001	1	µA

(1) Condition does not apply to input voltages below 2.5V since this is the minimum input operating voltage.
(2) All limits are verified by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits specified for $V_{IN} = V_O + 0.5V$[1], $V_{\overline{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$. **Boldface** limits apply for the operating temperature extremes: −40°C and 85°C.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{DO}	Dropout Voltage[1][4]	I_{OUT} = 1 mA		0.4		mV
		I_{OUT} = 200 mA		80	**220**	
		I_{OUT} = 300 mA		120		
ΔV_O	Line Regulation	I_{OUT} = 1 mA, $(V_O + 0.5V) \le V_I \le 6V$[1]	**−0.1**	0.01	**0.1**	%/V
	Load Regulation	100 µA ≤ I_{OUT} ≤ 300 mA		0.002		%/mA
e_n	Output Voltage Noise	I_{OUT} = 10 mA, 10 Hz ≤ f ≤ 100 kHz		37		μV_{RMS}
	Output Voltage Noise Density	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 10 µF		190		$nV/\sqrt{Hz}$
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold	V_{IH}, $(V_O + 0.5V) \le V_I \le 6V$[1]	**2**			V
		V_{IL}, $(V_O + 0.5V) \le V_I \le 6V$[1]			**0.4**	
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or IN		0.1	100	nA
I_{SET}	SET Input Leakage	SET = 1.3V, Adjust Version Only[5]		0.1	2.5	nA
$V_{\overline{FAULT}}$	$\overline{FAULT}$Detection Voltage	$V_O \ge 2.5V$, I_{OUT} = 200 mA[6]		120	**280**	mV
	$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 2 mA		0.115	**0.25**	V
$I_{\overline{FAULT}}$	$\overline{FAULT}$ Off-Leakage Current	$\overline{FAULT}$ = 3.6V, $\overline{SHDN}$ = 0V		0.1	100	nA
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			10		
T_{ON}	Start-Up Time	C_{OUT} = 10 µF, V_O at 90% of Final Value		120		µs

(4) Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its nominal value at $V_{IN} - V_O = 0.5V$. Dropout Voltage does not apply to the 1.8 version.
(5) The SET pin is not externally connected for the fixed versions.
(6) The $\overline{FAULT}$ detection voltage is specified for the input to output voltage differential at which the $\overline{FAULT}$ pin goes active low.

FUNCTIONAL BLOCK DIAGRAM

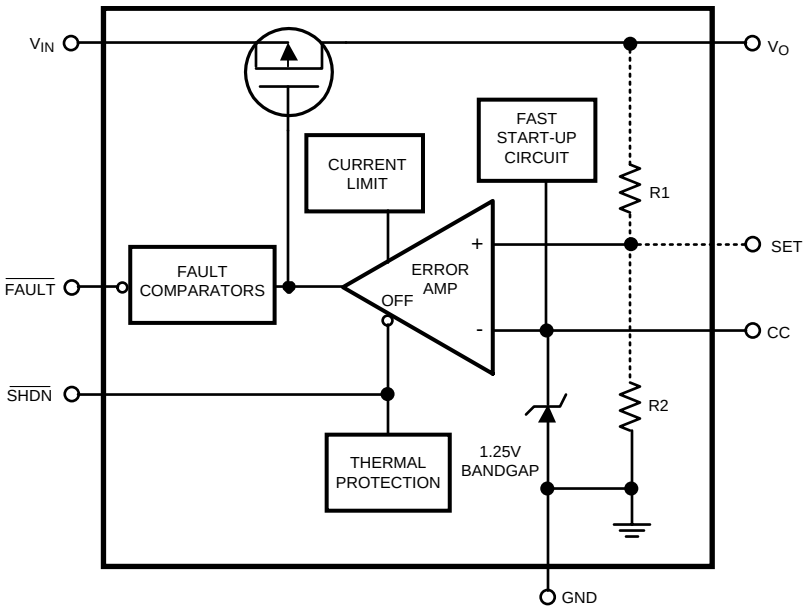


Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $V_{IN} = V_O + 0.5V$, $C_{IN} = C_{OUT} = 2.2\ \mu F$, $C_{CC} = 33$ nF, $T_J = 25°C$, $V_{\overline{SHDN}} = V_{IN}$.

Dropout Voltage vs. Load Current (For Different Output Voltages)

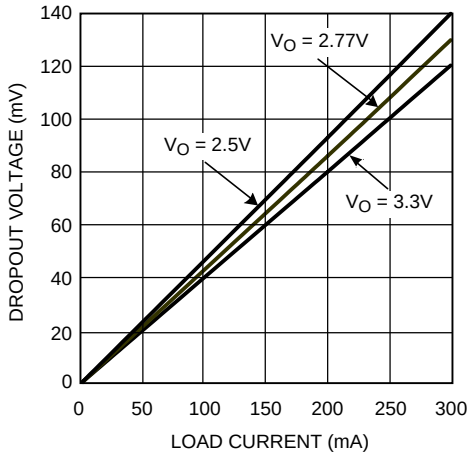


Figure 2.

Dropout Voltage vs. Load Current (For Different Output Temperatures)

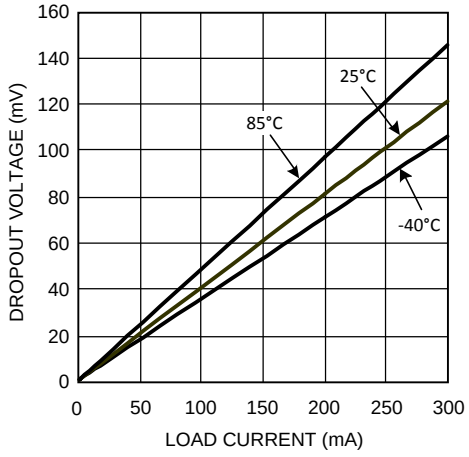


Figure 3.

$\overline{FAULT}$ Detect Threshold vs. Load Current

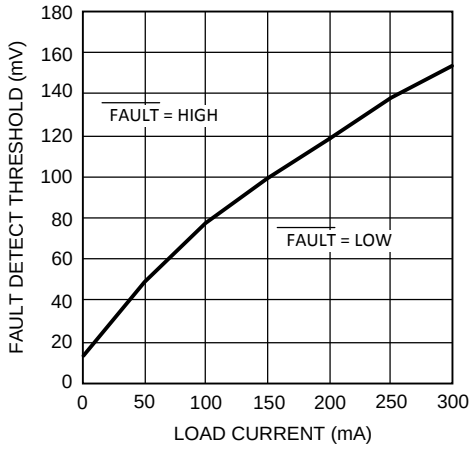


Figure 4.

Supply Current vs. Input Voltage

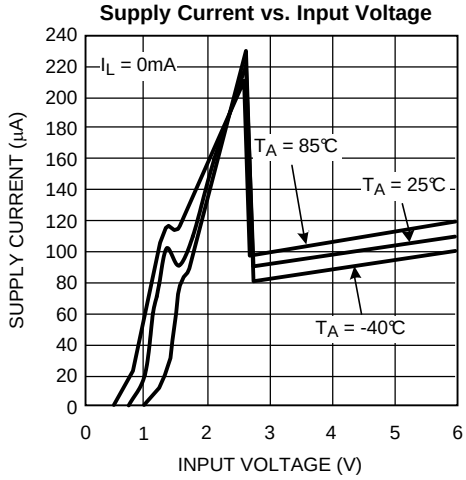


Figure 5.

Supply Current vs. Load Current

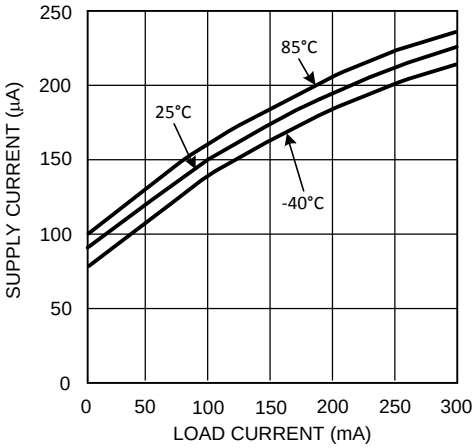


Figure 6.

Power Supply Rejection Ratio vs. Frequency

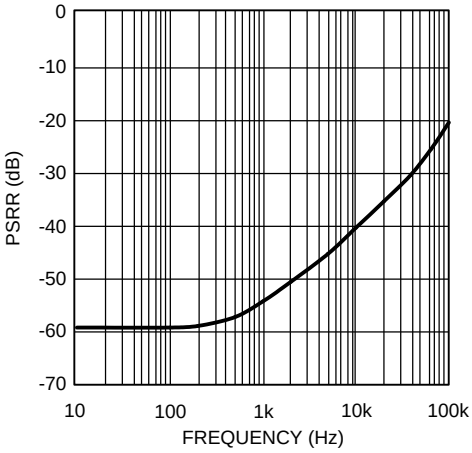


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_O + 0.5V$, $C_{IN} = C_{OUT} = 2.2\ \mu F$, $C_{CC} = 33$ nF, $T_J = 25°C$, $V_{\overline{SHDN}} = V_{IN}$.

Output Noise Spectral Density

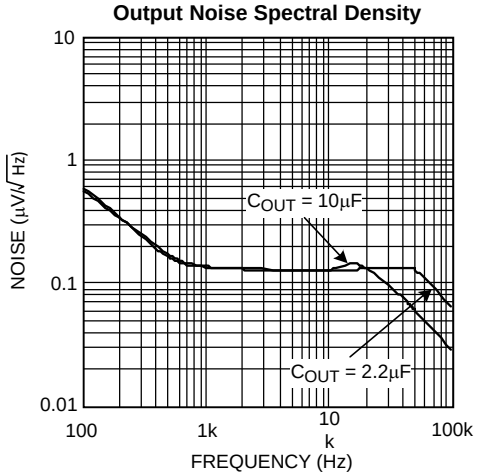


Figure 8.

Output Noise (10Hz to 100kHz)

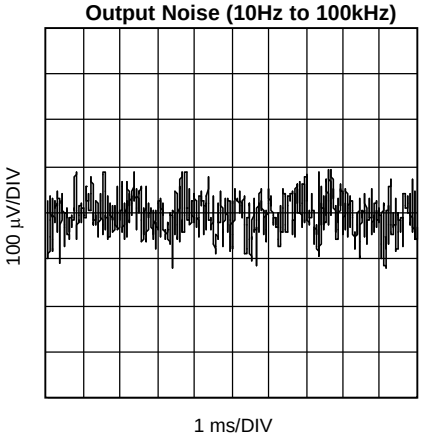


Figure 9.

Output Impedance vs. Frequency

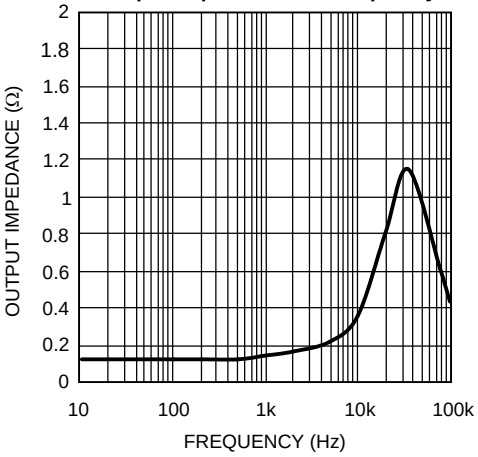


Figure 10.

Line Transient Response

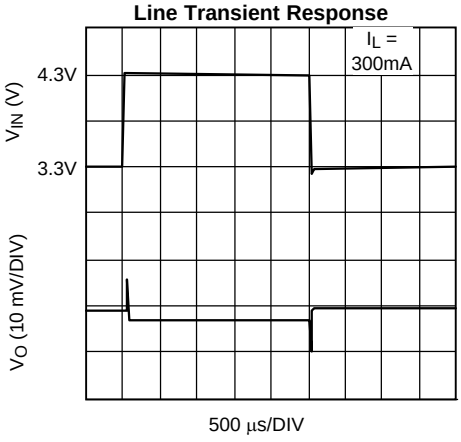


Figure 11.

Load Transient

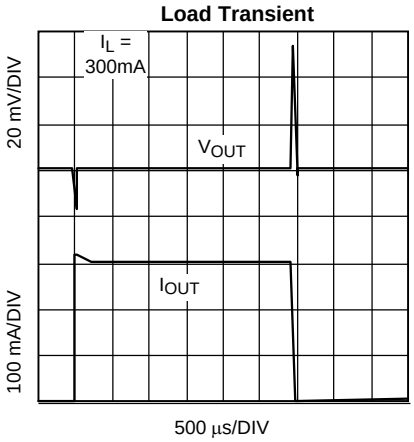


Figure 12.

Shutdown Response

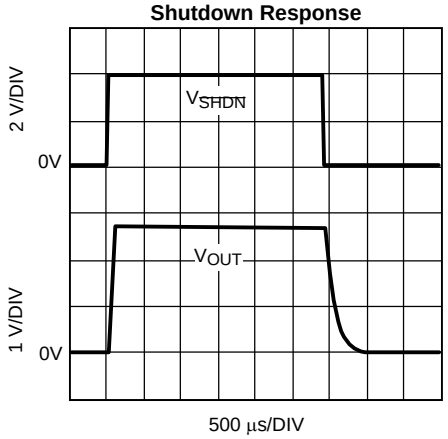


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_O + 0.5V$, $C_{IN} = C_{OUT} = 2.2\ \mu F$, $C_{CC} = 33\ nF$, $T_J = 25°C$, $V_{\overline{SHDN}} = V_{IN}$.

Power-Up Response

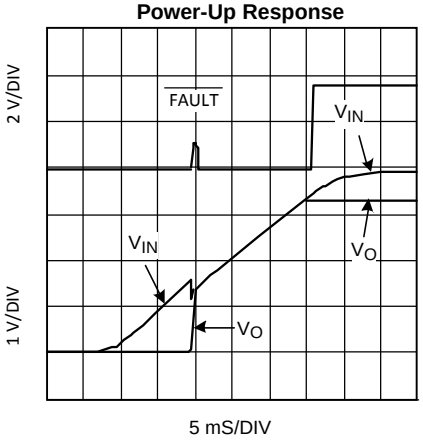


Figure 14.

Power-Down Response

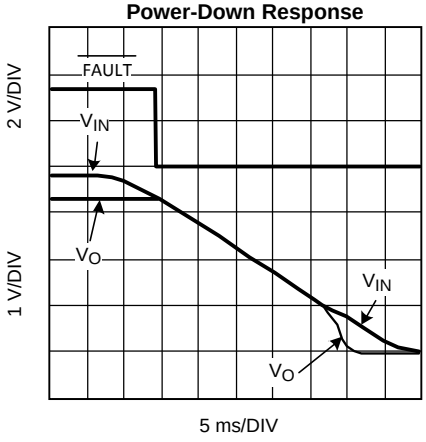


Figure 15.

APPLICATION INFORMATION

General Information

The LP3982 is package, pin and performance compatible with Maxim's MAX8860 excluding reverse battery protection and Dual Mode function (fixed and adjustable combined).

Figure 16 shows the functional block diagram for the LP3982. A 1.25V bandgap reference, an error amplifier and a PMOS pass transistor perform voltage regulation while being supported by shutdown, fault, and the usual Temperature and current protection circuitry

The regulator's topology is the classic type with negative feedback from the output to one of the inputs of the error amplifier. Feedback resistors R_1 and R_2 are either internal or external to the IC, depending on whether it is the fixed voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amplifier to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier provides the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal. In short, the error amplifier keeps the output voltage constant in order to keep its inputs equal.

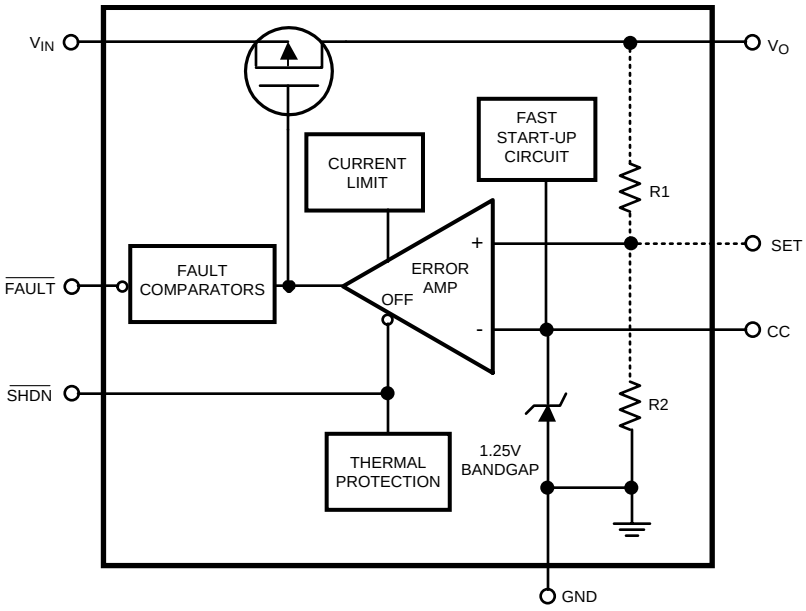


Figure 16. Functional Block Diagram for the LP3982

Output Voltage Setting (Adj Version Only)

The output voltage is set according to the amount of negative feedback (Note that the pass transistor inverts the feedback signal.) Figure 17 simplifies the topology of the LP3982. This type of regulator can be represented as an op amp configured as non-inverting amplifier and a fixed DC Voltage (V_{REF}) for its input signal. The special characteristic of this op amp is its extra-large output transistor that only sources current. In terms of its non-inverting configuration, the output voltage equals V_{REF} times the closed loop gain:

$$V_O = V_{REF}\left[\frac{R_1}{R_2} + 1\right] \quad (1)$$

Utilize the following equation for adjusting the output to a particular voltage:

$$R_1 = R_2\left[\frac{V_O}{1.25V} - 1\right] \quad (2)$$

Choose R_2 = 100k to optimize accuracy, power supply rejection, noise and power consumption.

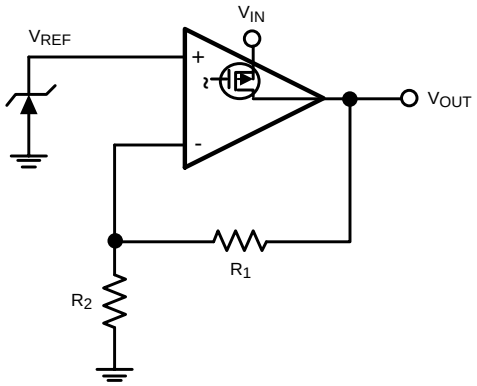


Figure 17. Regulator Topology Simplified

Similarity in the output capabilities exists between op amps and linear regulators. Just as rail-to-rail output op amps allow their output voltage to approach the supply voltage, low dropout regulators (LDOs) allow their output voltage to operate close to the input voltage. Both achieve this by the configuration of their output transistors. Standard op amps and regulator outputs are at the source (or emitter) of the output transistor. Rail-to-rail op amp and LDO regulator outputs are at the drain (or collector) of the output transistor. This replaces the threshold (or diode drop) limitations on the output with the less restrictive source-to-drain (or V_{SAT}) limitations. There is a trade-off, of course. The output impedance become significantly higher, thus providing a critically lower pole when combined with the capacitive load. That's why rail-to-rail op amps are usually poor at driving capacitive loads and recommend a series output resistor when doing so. LDOs require the same series resistance except that the internal resistance of the output capacitor will usually suffice. Refer to the Output Capacitance section for more information.

Output Capacitance

The LP3982 is specifically designed to employ ceramic output capacitors as low as 2.2 µF. Ceramic capacitors below 10µF offer significant cost and space savings, along with high frequency noise filtering. Higher values and other types and of capacitor may be used, but their equivalent series resistance (ESR) should be maintained below 0.5Ω

Ceramic capacitor of the value required by the LP3982 are available in the following dielectric types: Z5U, Y5V, X5R and X7R. The Z5U and Y5V types exhibit a 50% or more drop in capacitance value as their temperature increases from 25°C, an important consideration. The X5R generally maintain their capacitance value within ±20%. The X7R type are desirable for their tighter tolerance of 10% over temperature.

Ceramic capacitors pose a challenge because of their relatively low ESR. Like most other LDOs, the LP3982 relies on a zero in the frequency response to compensate against excessive phase shift in the regulator's feedback loop. If the phase shift reaches 360° (i.e.; becomes positive), the regulator will oscillate. This compensation usually resides in the zero generated by the combination of the output capacitor with its equivalent series resistance (ESR). The zero is intended to cancel the effects of the pole generated by the load capacitance (C_L) combined with the parallel combination of the load resistance (R_L) and the output resistance (R_O) of the regulator. The challenge posed by low ESR capacitors is that the zero it generates can be too high in frequency for the pole that it's intended to compensate. The LP3982 overcomes this challenge by internally generating a strategically placed zero.

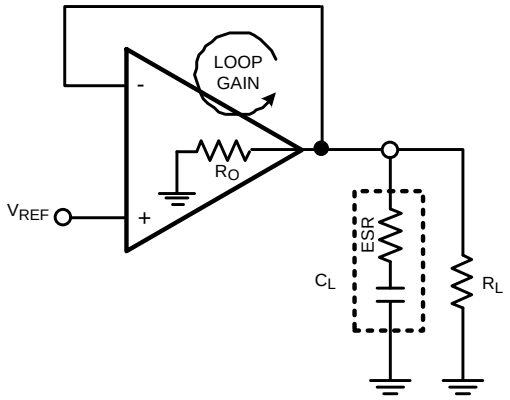


Figure 18. Simplified Model of Regulator Loop Gain Components

Figure 18 shows a basic model for the linear regulator that helps describe what happens to the output signal as it is processed through its feedback loop; that is, describe its loop gain (LG). The LG includes two main transfer functions: the error amplifier and the load. The error amplifier provides voltage gain and a dominant pole, while the load provides a zero and a pole. The LG of the model in Figure 18 is described by the following equation:

$$LG(j\omega) = \frac{A_O}{1 + j\left[\frac{\omega}{\omega_{POLE}}\right]} * \frac{1 + j\omega\,(ESR \times C_L)}{1 + j\omega\,((ESR + R_O \,//\, R_L)\,C_L)} \quad (3)$$

The first term of the above equation expresses the voltage gain (numerator) and a single pole role-off (denominator) of the error amplifier. The second term expresses the zero (numerator) and pole (denominator) of the load in combination with the R_O of the regulator.

Figure 19 shows a Bode plot that represents a case where the zero contributed by the load is too high to cancel the effect of the pole contributed by the load and R_O. The solid line illustrates the loop gain while the dashed line illustrates the corresponding phase shift. Notice that the phase shift at unity gain is a total 360° -the criteria for oscillation.

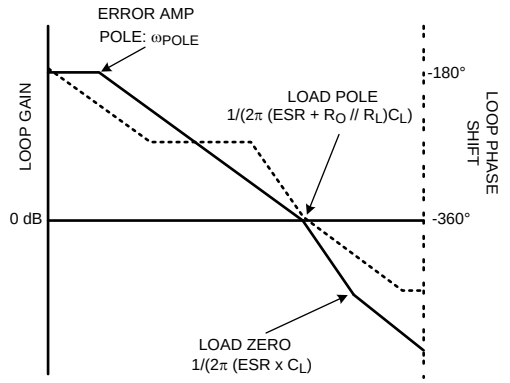


Figure 19. Loop Gain Bode Plot Illustrating Inadequately High Zero for Stability Compensation

The LP3982 generates an internal zero that makes up for the inadequately high zero of the low ESR ceramic output capacitor. This internally generated zero is strategically placed to provide positive phase shift near unity gain, thus providing a stable phase margin.

No-Load Stability

The LP3982 remains stable during no-load conditions, a necessary feature for CMOS RAM keep-alive applications.

Input Capacitor

The LP3982 requires a minimum input capacitance of about 1µF. The value may be increased indefinitely. The type is not critical to stability. However, instability may occur with bench set-ups where long supply leads are used, particularly at near dropout and high current conditions. This is attributed to the lead inductance coupling to the output through the gate oxide of the pass transistor; thus, forming a pseudo LCR network within the Loop-gain. A 10 µF tantalum input capacitor remedies this non-situ condition; its larger ESR acts to dampen the pseudo LCR network. This may only be necessary for some bench setups. 1 µF ceramic input capacitor are fine for most end-use applications.

If a tantalum input capacitor is intended for the final application, it is important to consider their tendency to fail in short circuit mode, thus potentially damaging the part.

Noise Bypass Capacitor

The noise bypass capacitor (CC) significantly reduces output noise of the LP3982. It connects between pin 6 and ground. The optimum value for CC is 33 nF.

Pin 6 directly connects to the high impedance output of the bandgap. The DC leakage of the CC capacitor should be considered; loading down the reference will reduce the output voltage. NPO and COG ceramic capacitors typically offer very low leakage. Polypropylene and polycarbonate film carbonate capacitor offer even lower leakage currents.

CC does not affect the transient response; however, it does affect turn-on time. The smaller the CC value, the quicker the turn-on time.

Power Dissipation

Power dissipation refers to the part's ability to radiate heat away from the silicon, with packaging being a key factor. A reasonable analogy is the packaging a human being might wear, a jacket for example. A jacket keeps a person comfortable on a cold day, but not so comfortable on a hot day. It would be even worse if the person was exerting power (exercising). This is because the jacket has resistance to heat flow to the outside ambient air, like the IC package has a thermal resistance from its junctions to the ambient (θ_{JA}).

θ_{JA} has a unit of temperature per power and can be used to calculate the IC's junction temperature as follows:

$$T_J = \theta_{JA} (PD) + T_A \quad (4)$$

- T_J is the junction temperature of the IC
- θ_{JA} is the thermal resistance from the junction to the ambient air outside the package
- PD is the power exerted by the IC
- T_A is the ambient temperature

PD is calculated as follows:

$$PD = I_{OUT} (V_{IN} - V_O) \quad (5)$$

- θ_{JA} for the LP3982 package (VSSOP-8) is 223°C/W with no forced air flow
- 182°C/W with 225 linear feet per minute (LFPM) of air flow
- 163°C/W with 500 LFPM of air flow
- 149°C/W with 900 LFPM of air flow

θ_{JA} can also be decreased (improved) by considering the layout of the PC board: heavy traces (particularly at V_{IN} and the two V_{OUT} pins), large planes, through-holes, etc.

Improvements and absolute measurements of the θ_{JA} can be estimated by utilizing the thermal shutdown circuitry that is internal to the IC. The thermal shutdown turns off the pass transistor of the device when its junction temperature reaches 160°C (Typical). The pass transistor doesn't turn on again until the junction temperature drops about 10°C (hysteresis).

Using the thermal shutdown circuit to estimate , θ_{JA} can be done as follows: With a low input to output voltage differential, set the load current to 300 mA. Increase the input voltage until the thermal shutdown begins to cycle on and off. Then slowly decrease V_{IN} (100 mV increments) until the part stays on. Record the resulting voltage differential (V_D) and use it in the following equation:

$$\theta_{JA} = \frac{(160 - T_A)}{(0.300 \times V_D)} \quad (6)$$

Fault Detection

The LP3982 provides a $\overline{\text{FAULT}}$ pin that goes low during out of regulation conditions like current limit and thermal shutdown, or when it approaches dropout. The latter monitors the input-to-output voltage differential and compares it against a threshold that is slightly above the dropout voltage. This threshold also tracks the dropout voltage as it varies with load current. Refer to Figure 4 in the typical characteristics section.

The $\overline{\text{FAULT}}$ pin requires a pull-up resistor since it is an open-drain output. This resistor should be large in value to reduce energy drain. A 100 kΩ pull-up resistor works well for most applications.

Figure 20 shows the LP3985 with delay added to the $\overline{\text{FAULT}}$ pin for the reset pin of a microprocessor. The output of the comparator stays low for a preset amount of time after the regulator comes out of a fault condition.

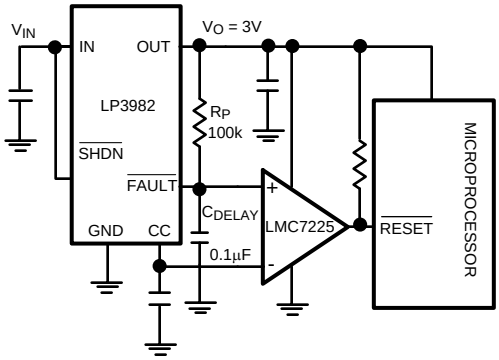


Figure 20. Power on Delayed Reset Application

The delay time for the application of Figure 20 is set as follows:

$$C_{DELAY} = \frac{-t}{R_P \ln\left[1 - \frac{V_{REF}}{V_O}\right]} \quad (7)$$

The application is set for a reset delay time of 8.8 ms. Note that the comparator should have high impedance inputs so as to not load down the V_{REF} at the CC pin of the LP3982.

Shutdown

The LP3982 goes into sleep mode when the $\overline{\text{SHDN}}$ pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to 1 nA typical. The maximum voltage for a logic low at the $\overline{\text{SHDN}}$ pin is 0.4V. A minimum voltage of 2V at the $\overline{\text{SHDN}}$ pin will turn the LP3982 back on. The $\overline{\text{SHDN}}$ pin may be directly tied to V_{IN} to keep the part on. The $\overline{\text{SHDN}}$ pin may exceed V_{IN} but not the ABS MAX of 6.5V.

Figure 21 shows an application that uses the $\overline{\text{SHDN}}$ pin. It detects when the battery is too low and disconnects the load by turning off the regulator. A micropower comparator (LMC7215) and reference (LM385) are combined with resistors to set the minimum battery voltage. At the minimum battery voltage, the comparator output goes low and tuns off the LP3982 and corresponding load. Hysteresis is added to the minimum battery threshold to prevent the battery's recovery voltage from falsely indicating an above minimum condition. When the load is disconnected from the battery, it automatically increases in terminal voltage because of the reduced IR drop across its internal resistance. The Minimum battery detector of Figure 21 has a low detection threshold (V_{LT}) of 3.6V that corresponds to the minimum battery voltage. The upper threshold (V_{UT}) is set for 4.6V in order to exceed the recovery voltage of the battery.

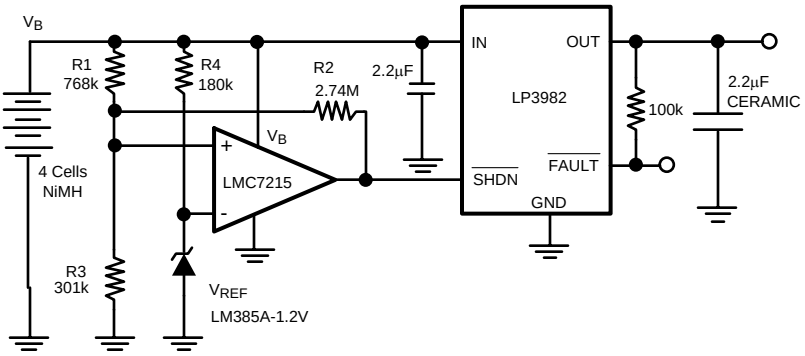


Figure 21. Minimum Battery Detector that Disconnects the Load Via the $\overline{\text{SHDN}}$ Pin of the LP3982

Resistor value for V_{UT} and V_{LT} are determined as follows:

$$G_T = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$V_{UT} = R_1 (V_{REF})\, G_T$$

$$V_{LT} = R_1 // R_2 (V_{REF})\, G_T \quad (8)$$

(The application of Figure 21 used a G_T of 5µ mho)

$$R_1 = \frac{V_{UT1}}{V_{REF}(G_T)} \quad (9)$$

$$R_2 = \frac{1}{\frac{V_{REF}(G_T)}{V_{LT}} - \frac{1}{R_1}} \quad (10)$$

$$R_3 = \frac{1}{G_T - \left[\frac{1}{R_1} + \frac{1}{R_2}\right]} \quad (11)$$

The above procedure assumes a rail-to-rail output comparator. Essentially, R_2 is in parallel with R_1 prior to reaching the lower threshold, then R_2 becomes parallel with R_3 for the upper threshold. Note that the application requires rail-to-rail input as well.

The resistor values shown in Figure 21 are the closest practical to calculated values.

Fast Start-Up

The LP3982 provides fast start-up time for better system efficiency. The start-up speed is maintained when using the optional noise bypass capacitor. An internal 500 µA current source charges the capacitor until it reaches about 90% of its final value.

Connection Diagram

The set pin is internally disconnected for the fixed versions.

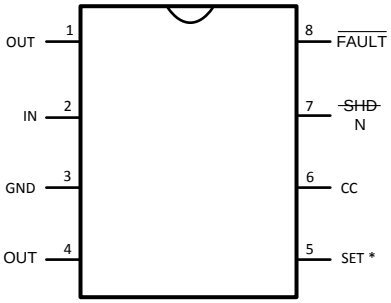


Figure 22. 8-Pin VSSOP
Top View

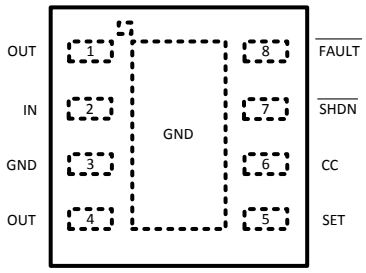


Figure 23. 8-Pin WSON Surface Mount
Top View

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3982ILD-1.8	NRND	WSON	NGM	8	1000	TBD	Call TI	Call TI	-40 to 85	LNB	
LP3982ILD-1.8/NOPB	ACTIVE	WSON	NGM	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LNB	Samples
LP3982ILD-2.5/NOPB	ACTIVE	WSON	NGM	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LPB	Samples
LP3982ILD-3.0/NOPB	ACTIVE	WSON	NGM	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LTB	Samples
LP3982ILD-3.3/NOPB	ACTIVE	WSON	NGM	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LUB	Samples
LP3982ILD-ADJ/NOPB	ACTIVE	WSON	NGM	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LVB	Samples
LP3982ILDX-1.8/NOPB	ACTIVE	WSON	NGM	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LNB	Samples
LP3982ILDX-3.0/NOPB	ACTIVE	WSON	NGM	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LTB	Samples
LP3982ILDX-3.3/NOPB	ACTIVE	WSON	NGM	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LUB	Samples
LP3982ILDX-ADJ/NOPB	ACTIVE	WSON	NGM	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LVB	Samples
LP3982IMM-1.8	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	LENB	
LP3982IMM-1.8/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LENB	Samples
LP3982IMM-2.5	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	LEPB	
LP3982IMM-2.5/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LEPB	Samples
LP3982IMM-3.0	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	LETB	
LP3982IMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LETB	Samples
LP3982IMM-3.3	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	LEUB	
LP3982IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LEUB	Samples
LP3982IMM-ADJ	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	LEVB	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3982IMM-ADJ/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LEVB	Samples
LP3982IMMX-1.8/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LENB	Samples
LP3982IMMX-2.5/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LEPB	Samples
LP3982IMMX-2.82/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LESB	Samples
LP3982IMMX-ADJ	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	LEVB	
LP3982IMMX-ADJ/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LEVB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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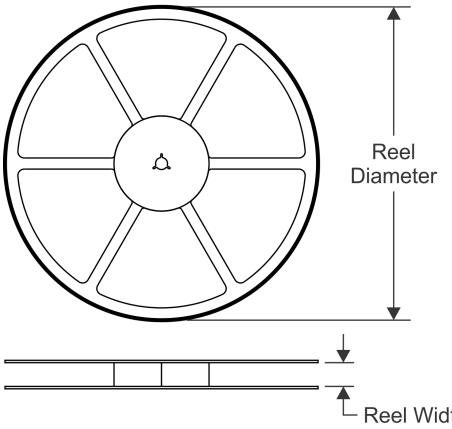
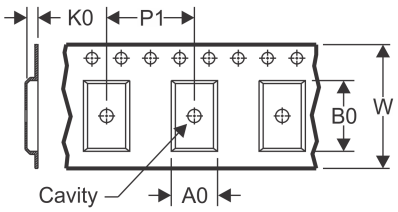
REEL DIMENSIONS

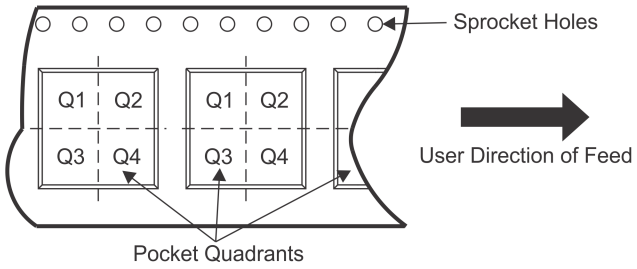


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

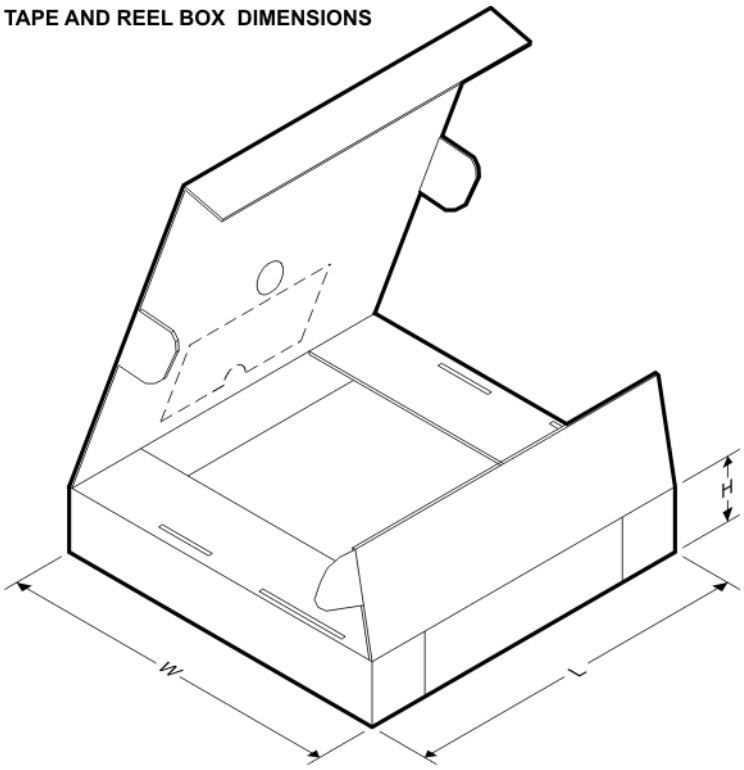


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3982ILD-1.8	WSON	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-1.8/NOPB	WSON	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-2.5/NOPB	WSON	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-3.0/NOPB	WSON	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-3.3/NOPB	WSON	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILD-ADJ/NOPB	WSON	NGM	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILDX-1.8/NOPB	WSON	NGM	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILDX-3.0/NOPB	WSON	NGM	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILDX-3.3/NOPB	WSON	NGM	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982ILDX-ADJ/NOPB	WSON	NGM	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP3982IMM-1.8	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-1.8/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-2.5	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-2.5/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-3.0	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-3.3	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3982IMM-ADJ	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMM-ADJ/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-1.8/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-2.5/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-2.82/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-ADJ	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3982IMMX-ADJ/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

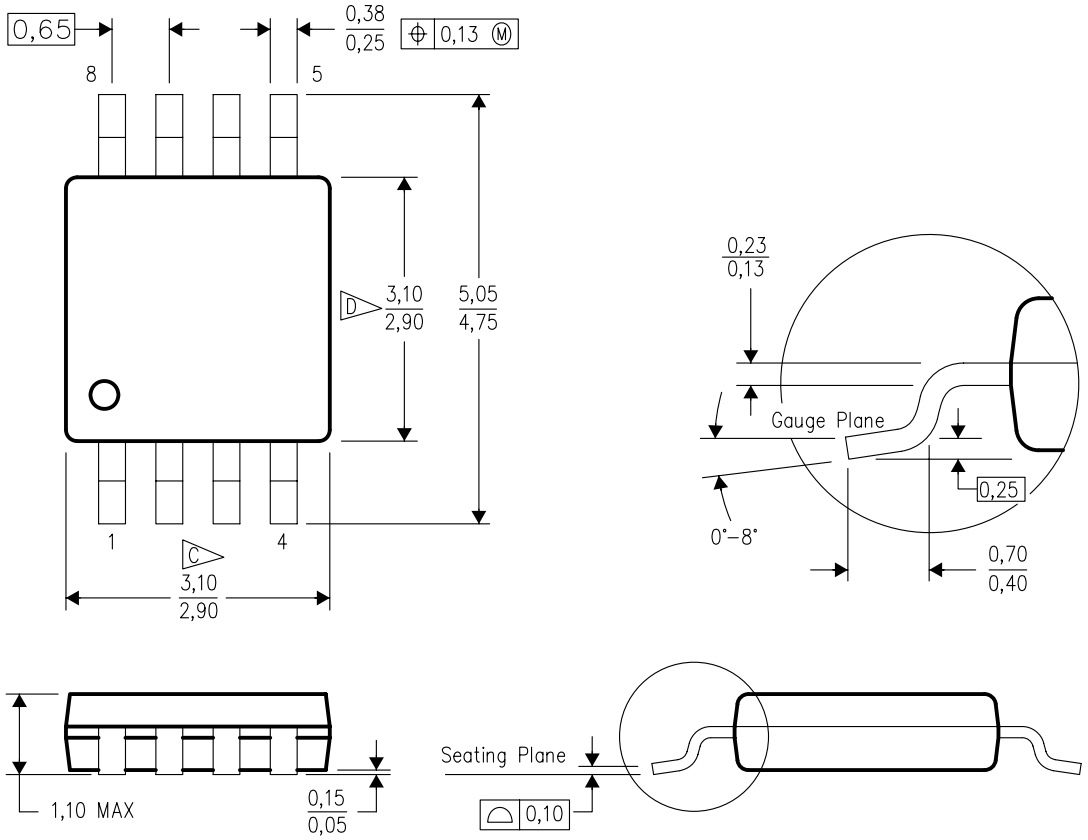


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3982ILD-1.8	WSON	NGM	8	1000	210.0	185.0	35.0
LP3982ILD-1.8/NOPB	WSON	NGM	8	1000	213.0	191.0	55.0
LP3982ILD-2.5/NOPB	WSON	NGM	8	1000	213.0	191.0	55.0
LP3982ILD-3.0/NOPB	WSON	NGM	8	1000	213.0	191.0	55.0
LP3982ILD-3.3/NOPB	WSON	NGM	8	1000	213.0	191.0	55.0
LP3982ILD-ADJ/NOPB	WSON	NGM	8	1000	213.0	191.0	55.0
LP3982ILDX-1.8/NOPB	WSON	NGM	8	4500	367.0	367.0	35.0
LP3982ILDX-3.0/NOPB	WSON	NGM	8	4500	367.0	367.0	35.0
LP3982ILDX-3.3/NOPB	WSON	NGM	8	4500	367.0	367.0	35.0
LP3982ILDX-ADJ/NOPB	WSON	NGM	8	4500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3982IMM-1.8	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-1.8/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-2.5	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-2.5/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-3.0	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-3.3	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-ADJ	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMM-ADJ/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3982IMMX-1.8/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3982IMMX-2.5/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3982IMMX-2.82/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3982IMMX-ADJ	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3982IMMX-ADJ/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

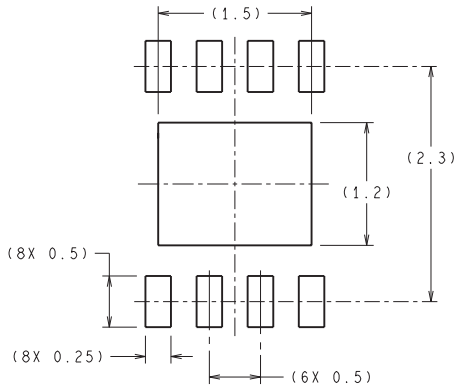
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

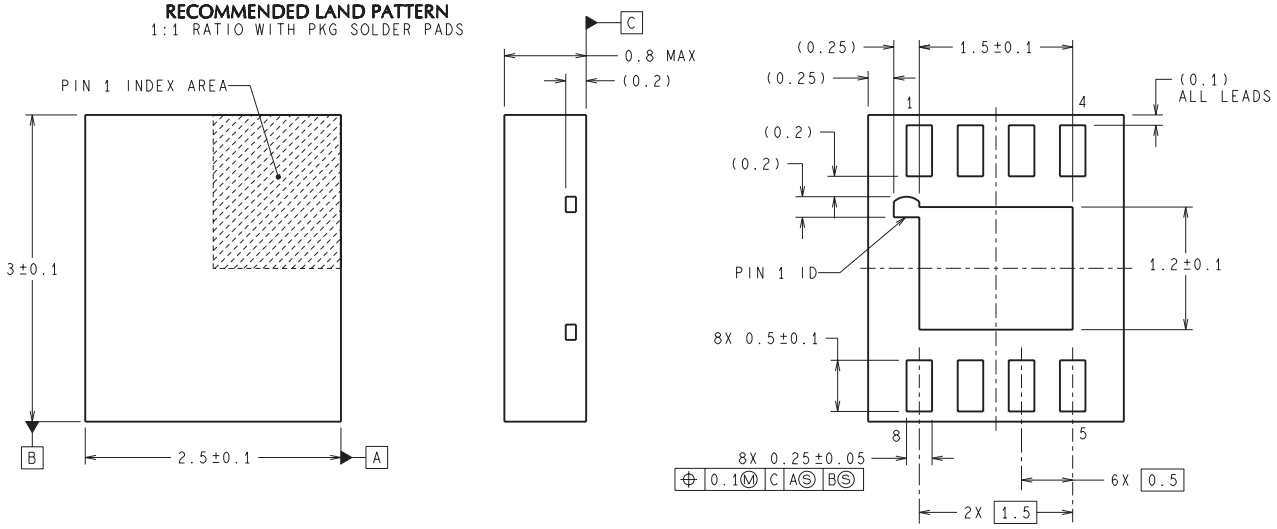
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

NGM0008C



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



LDA08C (Rev B)

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