Crystal-to-LVDS PCI Express™ Clock Synthesizer w/Spread Spectrum

ICS844202-245

PRELIMINARY DATA SHEET

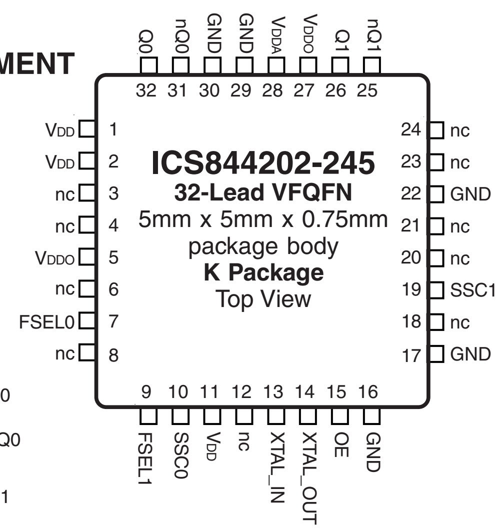
General Description

The ICS844202-245 is a 2 output PCI Express™ clock synthesizer optimized to generate low jitter PCIe reference clocks with or without spread spectrum modulation. Spread type and amount can be configured via the SSC control pins. Using a 25MHz, 18pF parallel resonant crystal, the device will generate LVDS clocks at either 25MHz, 100MHz, 125MHz or 250MHz. The ICS844202-245 uses a low jitter VCO that easily meets PCI Express jitter requirements and is packaged in a 32-pin VFQFN package.

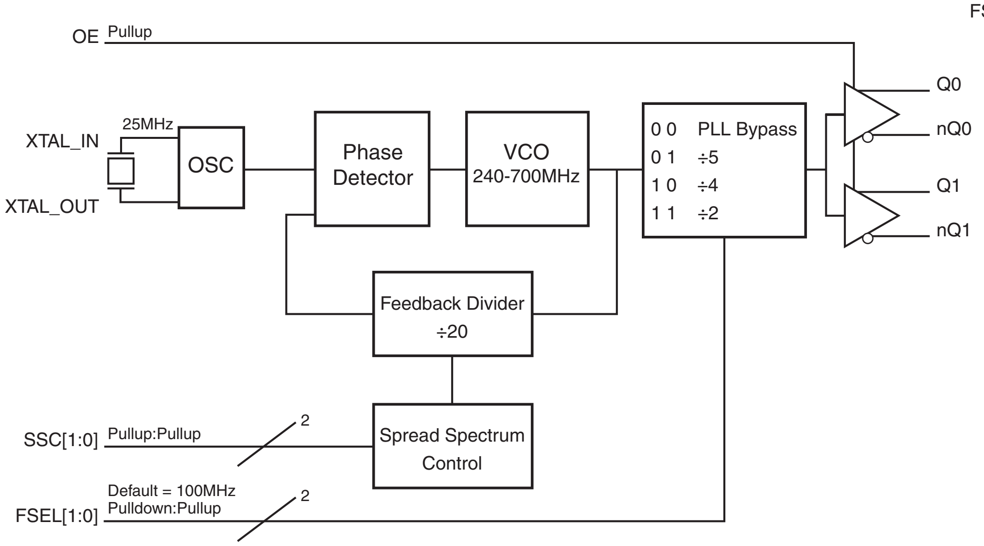
Features

- Two LVDS outputs at 25MHz, 100MHz, 125MHz or 250MHz
- Crystal oscillator interface, 25MHz, 18pF parallel resonant crystal
- Supports the following output frequencies: 25MHz, 100MHz, 125MHz or 250MHz
- VCO range: 240MHz - 700MHz
- Supports SSC downspread at 0.50% and -0.75%, centerspread at ±0.25% and no spread options
- Cycle-to-cycle jitter: 70ps (typical)
- Period jitter: 40ps (typical)
- Full 3.3V power supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 11	V_{DD}	Power		Core supply pins.
3, 4, 6, 8, 12, 18, 20, 21, 23, 24	nc	Unused		No connect.
5, 27	V_{DDO}	Power		Output supply pins.
7	FSEL0	Input	Pullup	Output frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.
9	FSEL1	Input	Pulldown	Output frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.
10, 19	SSC0 SSC1	Input	Pullup	Spread spectrum control pins. See Table 3B. LVCMOS/LVTTL interface levels.
13, 14	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. (PLL reference.)
15	OE	Input		Output enable pin. Logic HIgh, outputs are enabled. Logic LOW, outputs are in Hi-Z. LVCMOS/LVTTL interface levels.
16, 17, 22. 29. 30	GND	Power		Power supply ground.
25, 26	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
28	V_{DDA}	Power		Analog supply pin.
31, 32	nQ0, Q0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pulllup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. FSEL[1:0] FUNCTION TABLE

Input		Outputs
FSEL1	FSEL0	Q[0:1], nQ[0:1]
0	0	PLL Bypass (25MHz)
0	1	100MHz (default)
1	0	125MHz
1	1	250MHz

TABLE 3B. SSC[1:0] FUNCTION TABLE

Input		Spread %
SSC1	SSC0	
0	0	Center ± -0.25
0	1	Down -0.5
1	0	Down -0.75
1	1	No Spread (default)

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	43.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			83		mA
I_{DDA}	Analog Supply Current			12		mA
I_{DDO}	Output Supply Current			26		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FSEL1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		SSC0, SSC1, FSEL0, OE	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	FSEL1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		SSC0, SSC1, FSEL0, OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.33		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)					Ω
Shunt Capacitance				7	pF
Drive Level				100	µW

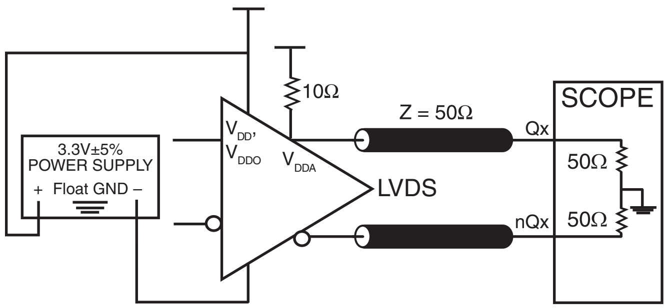
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

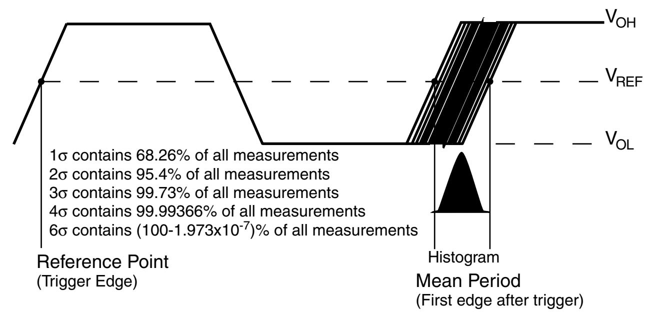
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			25		MHz
				125		MHz
				100		MHz
				250		MHz
*t*jit(per)	Period Jitter, RMS	25MHz		35		ps
		100MHz		45		ps
		125MHz		40		ps
		250MHz		40		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2	25MHz		60		ps
		100MHz		70		ps
		125MHz		60		ps
		250MHz		70		ps
*t*sk(o)	Output Skew; NOTE 2, 3			40		ps
F_{xtal}	Crystal Input Range; NOTE 1		12	25	35	MHz
F_M	SSC Modulation Frequency; NOTE 4					kHz
F_{MF}	SSC Modulation Factor; NOTE 4					%
SSC_{red}	Spectral Reduction; NOTE 5			11		dB
t_{STABLE}	Power-up to Stable Clock Output				10	ms
t_R / t_F	Output Rise/Fall Time	20% - 80%		525		ps
odc	Output Duty Cycle			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Only valid within the VCO operating range.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 4: Spread Spectrum clocking enabled.

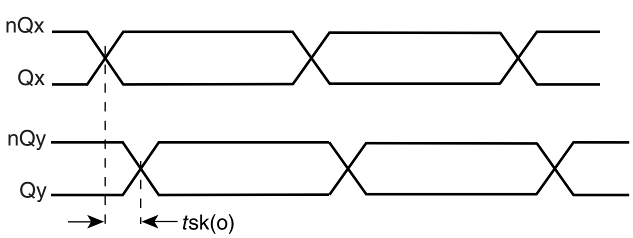
PARAMETER MEASUREMENT INFORMATION



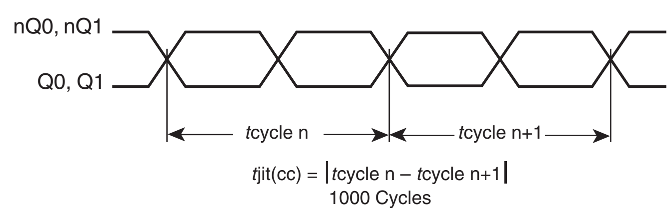
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



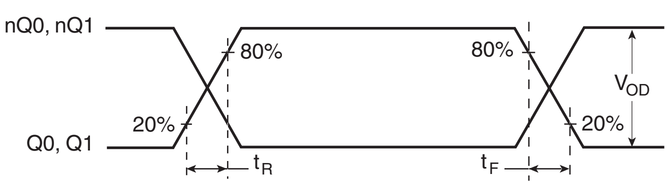
PERIOD JITTER



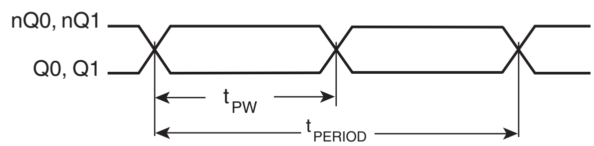
OUTPUT SKEW



CYCLE-TO-CYCLE JITTER



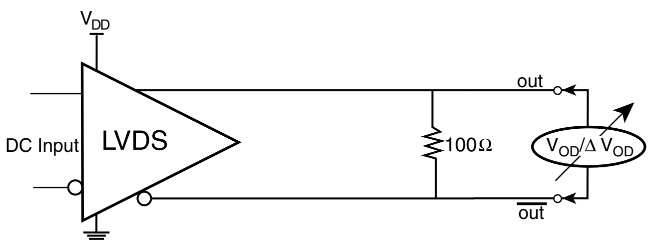
OUTPUT RISE/FALL TIME



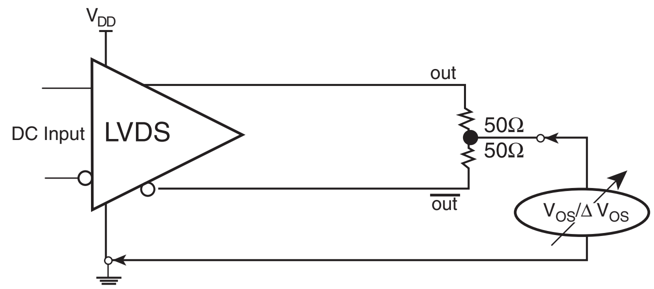
$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844202-245 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

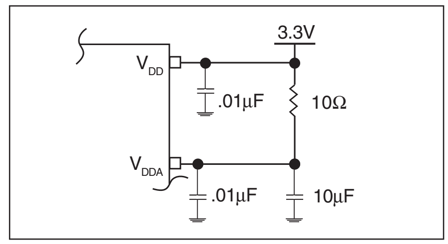


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Crystal Input Interface

The ICS844204-245 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

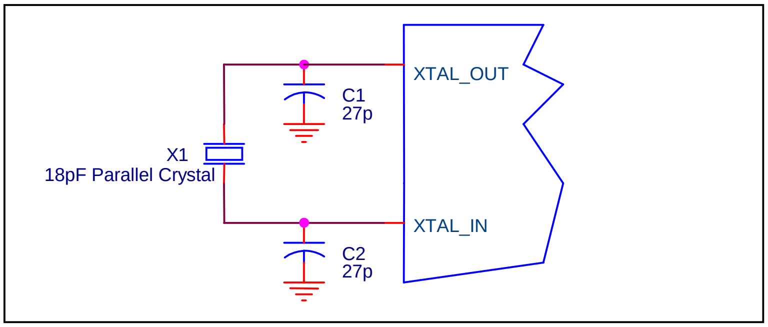


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note the device performance is guaranteed by using a quartz crystal.

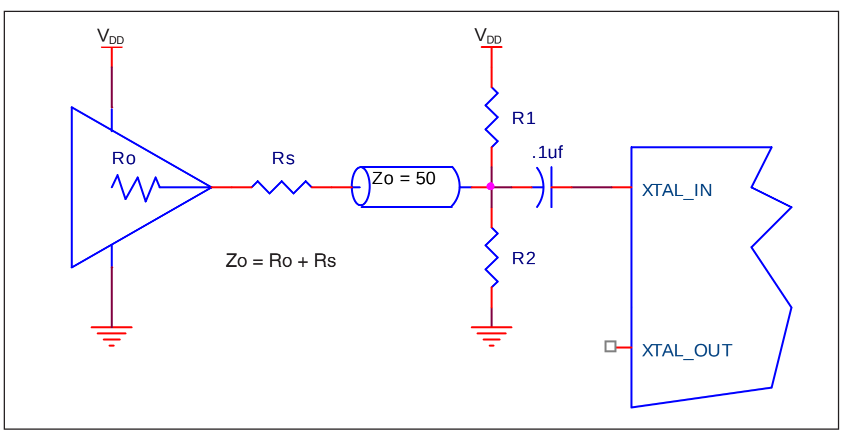


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/ slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

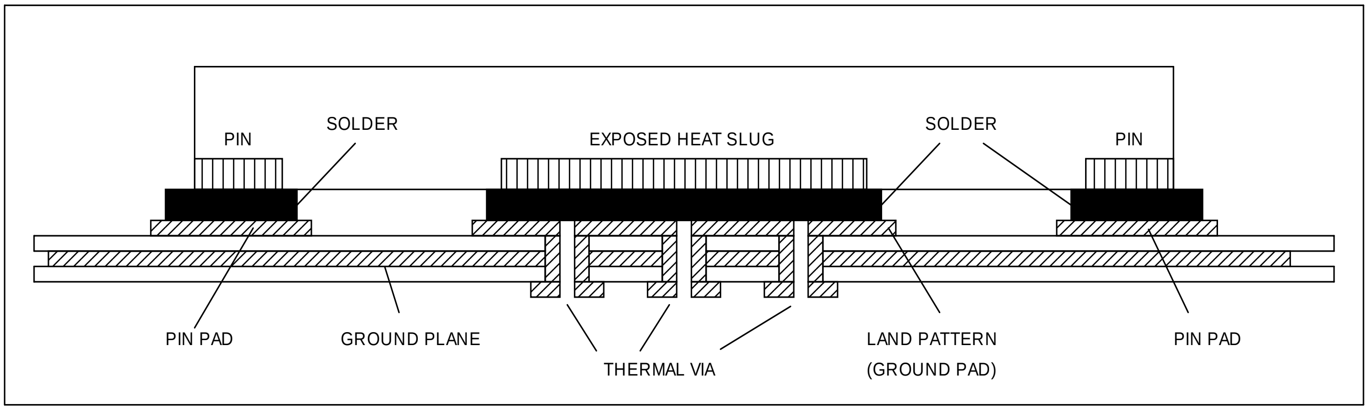


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 5.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

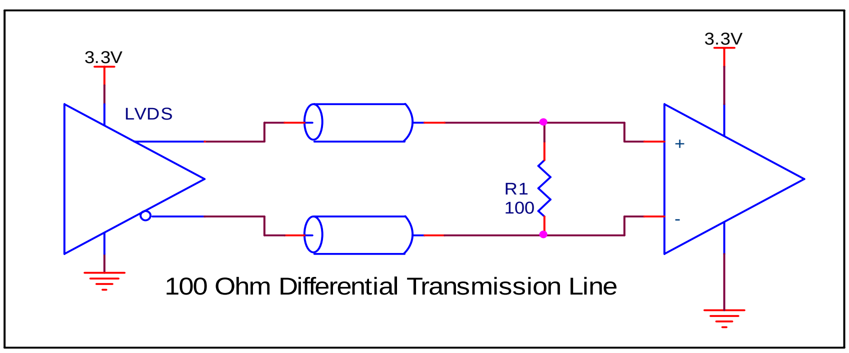


Figure 5. Typical LVDS Driver Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844202-245. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844202-245 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.645V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX} + I_{DDO\_MAX})$ = 3.465V * (83mA + 12mA + 26mA) = **419.27mW**

2. Junction Temperature.

Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 43.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.419W * 43.4°C/W = 88.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

Reliability Information

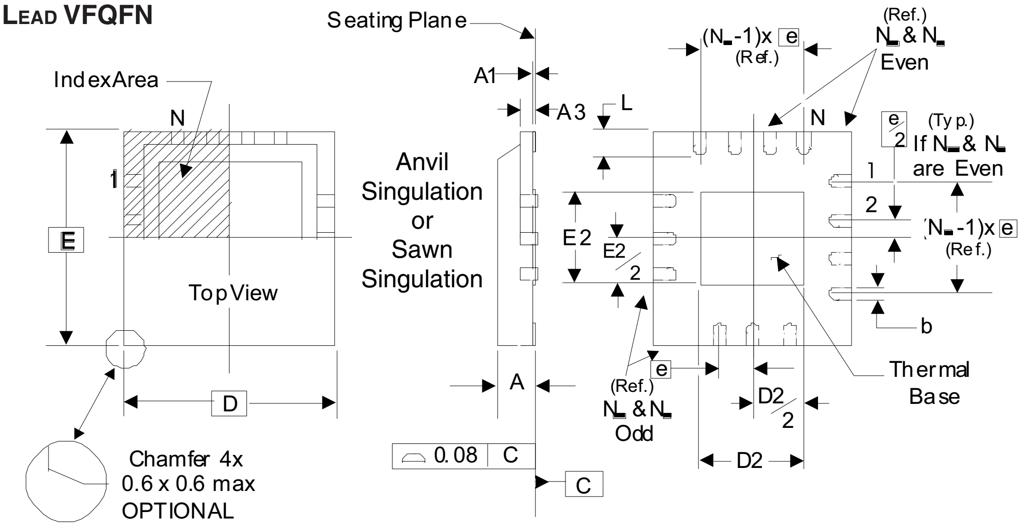
Table 7. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

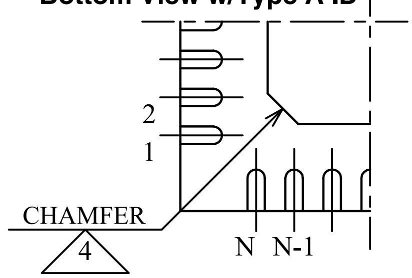
Transistor Count

The transistor count for ICS844202-245 is: 4715

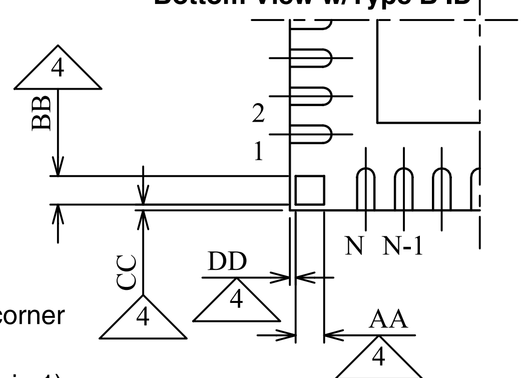
Package Outline - K Suffix for 32 Lead VFQFN



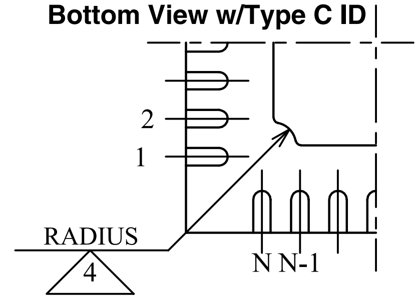
Bottom View w/Type A ID



Bottom View w/Type B ID



Bottom View w/Type C ID



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18		0.30
N_D, N_E			8
D, E	5.00 BASIC		
D2, E2	3.00		3.30
e	0.50 BASIC		
L	0.30		0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844202BK-245LF	ICS402B245L	32 Lead "Lead-Free" VFQFN	tray	0°C to 70°C
844202BK-245LFT	ICS402B245L	32 Lead "Lead-Free" VFQFN	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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