



CY7C164
CY7C166

16K x 4 Static RAM

Features

- High speed
— 15 ns
- Output enable ($\overline{OE}$) feature (7C166)
- CMOS for optimum speed/power
- Low active power
— 633 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and

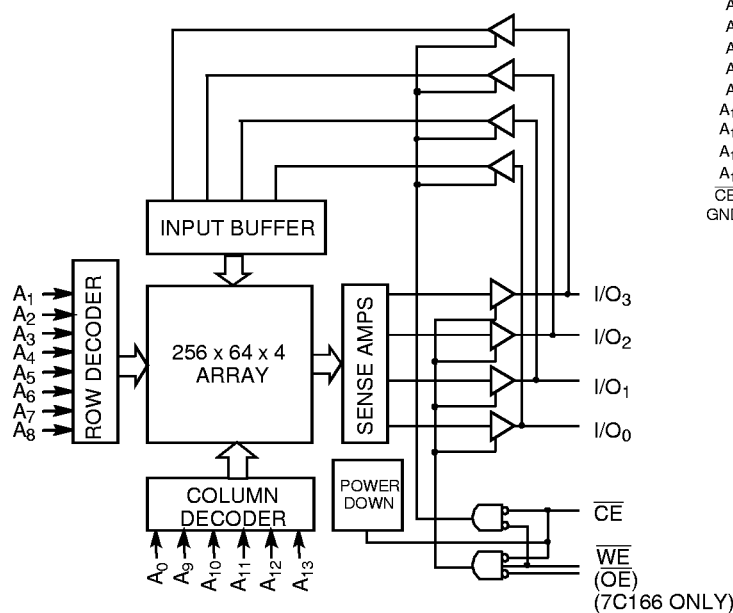
three-state drivers. The CY7C166 has an active LOW Output Enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW (and the Output Enable ($\overline{OE}$) is LOW for the 7C166). Data on the four input/output pins (I/O₀ through I/O₃) is written into the memory location specified on the address pins (A₀ through A₁₃).

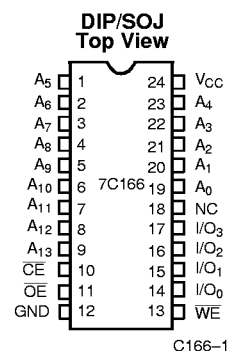
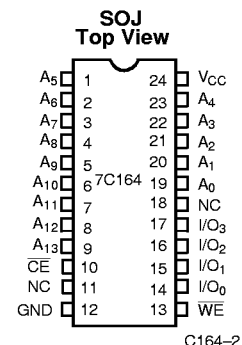
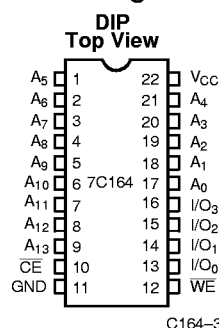
Reading the device is accomplished by taking Chip Enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166), while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in a high-impedance state when Chip Enable ($\overline{CE}$) is HIGH (or Output Enable ($\overline{OE}$) is HIGH for 7C166). A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide^[1]

	7C164-15 7C166-15	7C164-20 7C166-20	7C164-25 7C166-25	7C164-35 7C166-35
Maximum Access Time (ns)	15	20	25	35
Maximum Operating Current (mA)	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	20/20	20/20

Note:

1. For military specifications, see the CY7C164A/CY7C166A data sheet

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[2] -0.5V to +7.0V

DC Input Voltage^[2] -0.5V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C164-15 7C166-15		7C164-20 7C166-20		7C164-25, 35 7C166-25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		115		80		70	mA
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		40		20	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

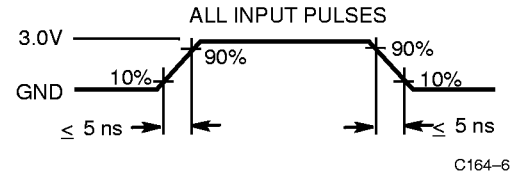
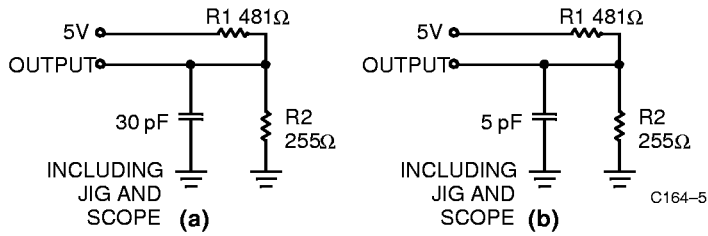
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT — 167Ω — 1.73V

Switching Characteristics Over the Operating Range^[6]

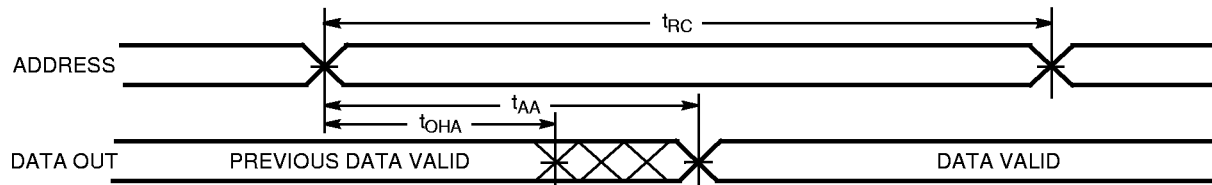
Parameter	Description		7C164-15 7C166-15		7C164-20 7C166-20		7C164-25 7C166-25		7C164-35 7C166-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
t _{RC}	Read Cycle Time		15		20		25		35		ns
t _{AA}	Address to Data Valid			15		20		25		35	ns
t _{OHA}	Output Hold from Address Change		3		5		5		5		ns
t _{ACE}	CE LOW to Data Valid			15		20		25		35	ns
t _{DOE}	OE LOW to Data Valid	7C166		10		10		12		15	ns
t _{LZOE}	OE LOW to Low Z	7C166	3		3		3		3		ns
t _{HZOE}	OE HIGH to High Z	7C166		8		8		10		12	ns
t _{LZCE}	CE LOW to Low Z ^[7]		3		5		5		5		ns
t _{HZCE}	CE HIGH to High Z ^[7, 8]			8		8		10		15	ns
t _{PU}	CE LOW to Power-Up		0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down			15		20		20		20	ns
WRITE CYCLE ^[9]											
t _{WC}	Write Cycle Time		15		20		20		25		ns
t _{SCE}	CE LOW to Write End		12		15		20		25		ns
t _{AW}	Address Set-Up to Write End		12		15		20		25		ns
t _{HA}	Address Hold from Write End		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start		0		0		0		0		ns
t _{PWE}	WE Pulse Width		12		15		15		20		ns
t _{SD}	Data Set-Up to Write End		10		10		10		15		ns
t _{HD}	Data Hold from Write End		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[7]		5		5		5		5		ns
t _{HZWE}	WE LOW to High Z ^[7, 8]			7		7		7		10	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) in AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

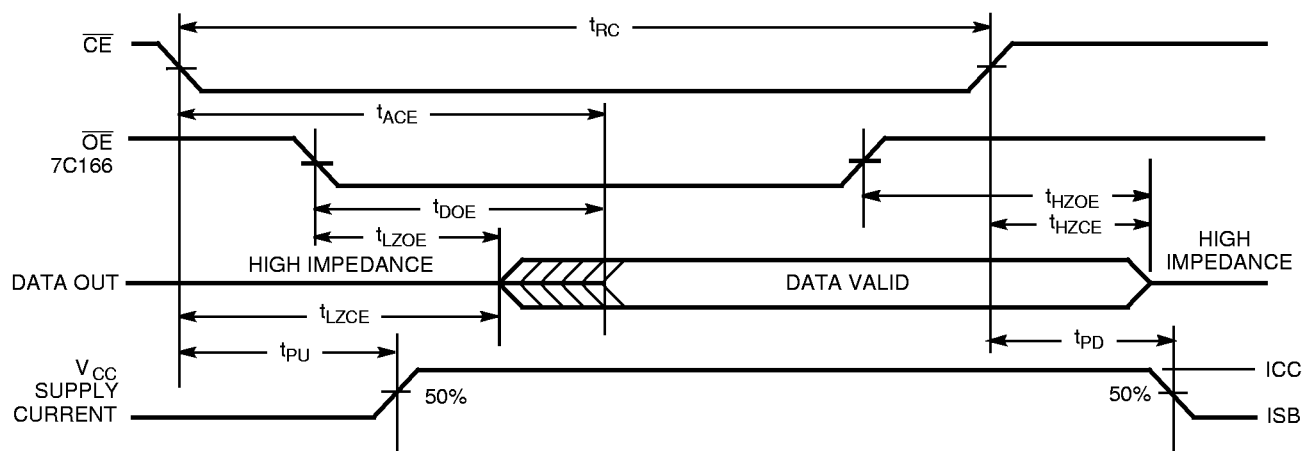
Switching Waveforms

Read Cycle No.1 [10, 11]



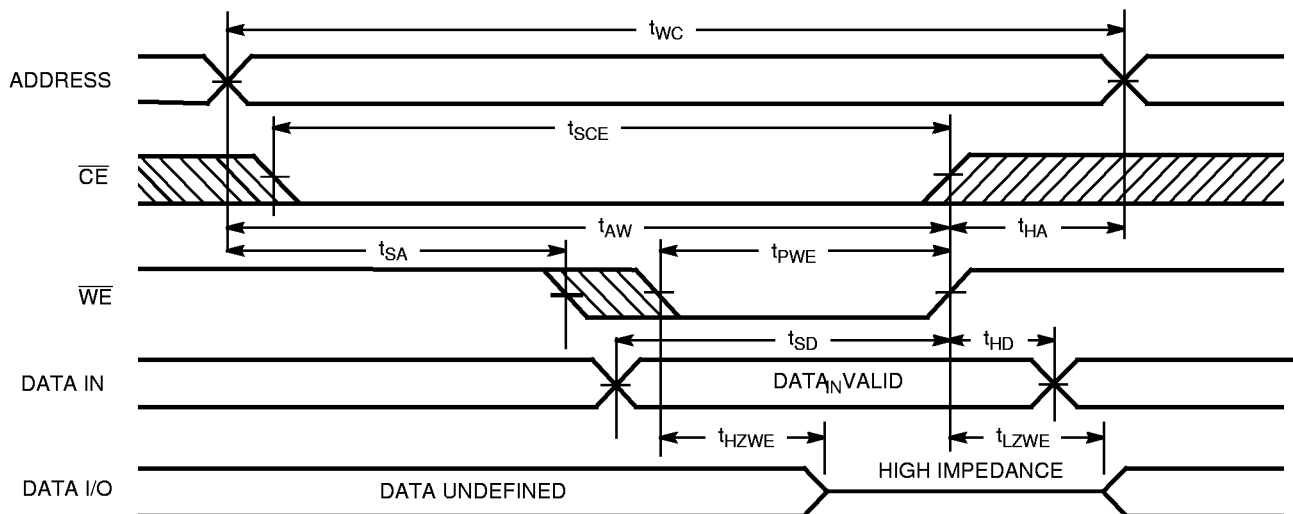
C164-7

Read Cycle No. 2 [10, 12]



C164-8

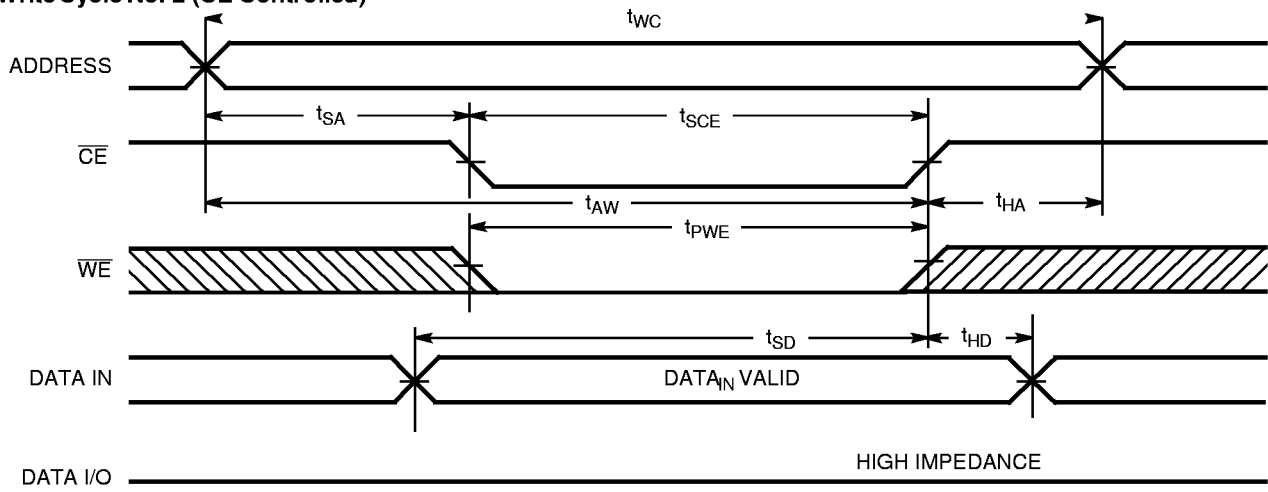
Write Cycle No. 1 ($\overline{WE}$ Controlled) [9, 13]



C164-9

Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$. (7C166: $\overline{OE} = V_{IL}$ also).
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. 7C166 only: Data I/O will be high-impedance if $\overline{OE} = V_{IH}$.

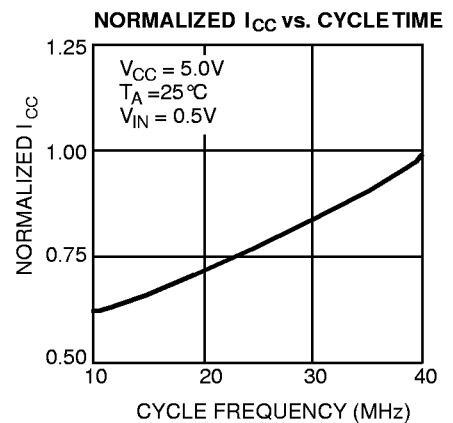
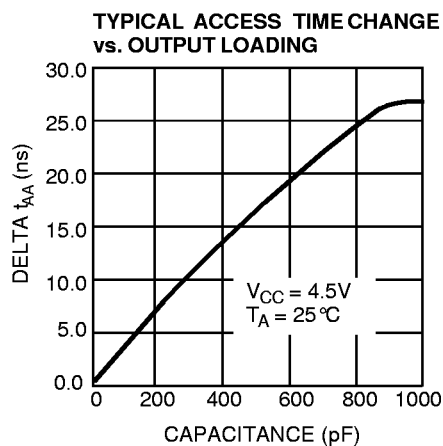
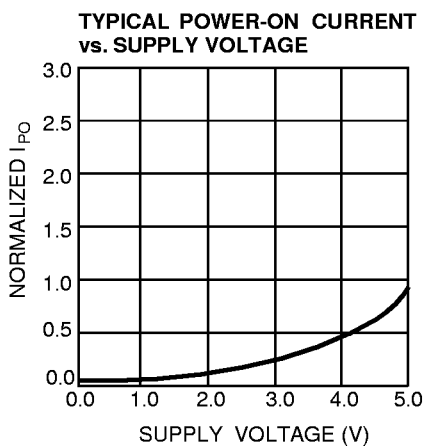
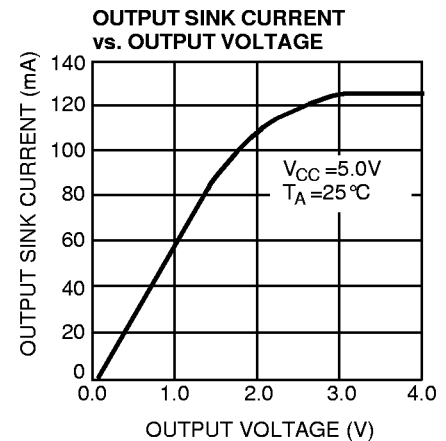
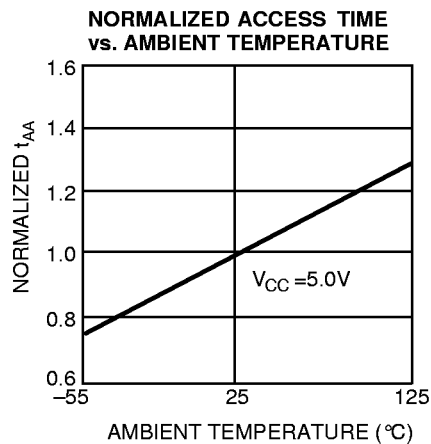
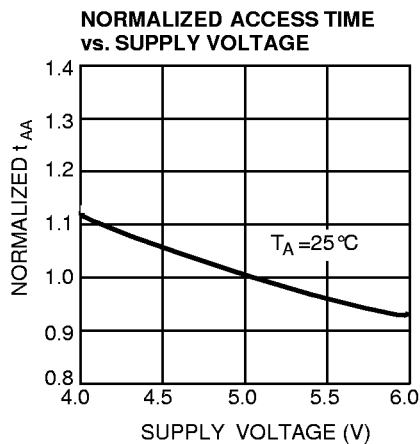
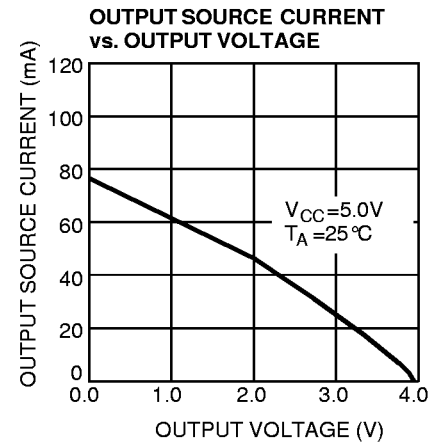
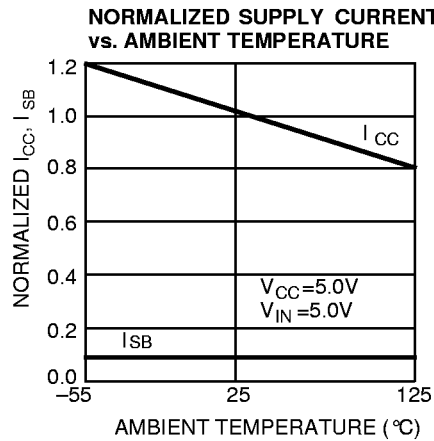
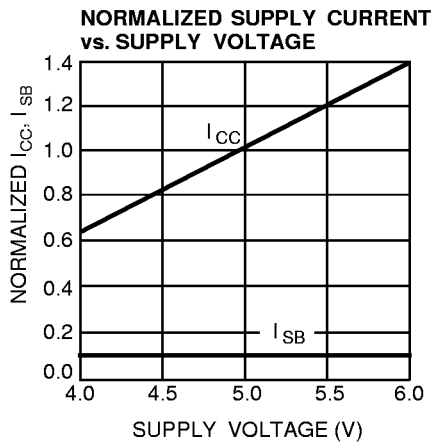
Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13, 14]


C164-10

Note:

14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



CY7C164 Truth Table

CE	WE	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

CY7C166 Truth Table

CE	WE	OE	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	H	Data In	Write
L	H	H	High Z	Write

Address Designators

Address Name	Address Function	CY 7C164 Pin Number	CY7C166 Pin Number
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23

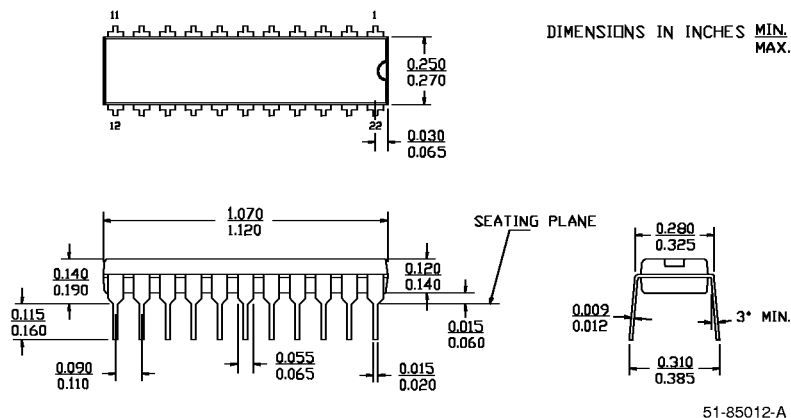
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C164-15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-15VC	V13	24-Lead Molded SOJ	
20	CY7C164-20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-20VC	V13	24-Lead Molded SOJ	
25	CY7C164-25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-25VC	V13	24-Lead Molded SOJ	
35	CY7C164-35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-35VC	V13	24-Lead Molded SOJ	

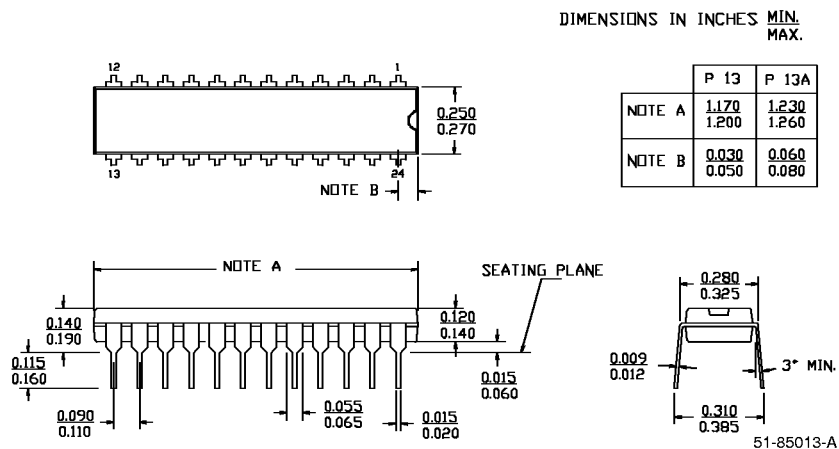
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C166-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-15VC	V13	24-Lead Molded SOJ	
20	CY7C166-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-20VC	V13	24-Lead Molded SOJ	
25	CY7C166-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-25VC	V13	24-Lead Molded SOJ	
35	CY7C166-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-35VC	V13	24-Lead Molded SOJ	

Package Diagrams

22-Lead (300-Mil) Molded DIP P9



24-Lead (300-Mil) Molded DIP P13/P13A



24-Lead (300-Mil) Molded SOJ V13

