



**Z86E61/Z86E63**

**CMOS Z8 16K/32K EPROM  
Microcontroller**

**Product Specification**

PS014401-1001



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## FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC, 44-Pin LQFP Style Packages
- 4.5V to 5.5V Operating Range
- Clock Speeds: 16 and 20 MHz
- Low Power Consumption: 275 mW (max)
- Fast Instruction Pointer: 1.0 ms @ 12 MHz
- Two Standby Modes: STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- High Voltage Protection on High Voltage Inputs
- RAM and EPROM Protect
- EPROM:
  - 16 Kbytes Z86E61
  - 32 Kbytes Z86E63
- 256 Bytes Register File
  - 236 Bytes of General-Purpose RAM
  - 16 Bytes of Control and Status Registers
  - 4 Bytes for Ports
- Two Programmable 8-Bit Counter/Timers. Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive



## GENERAL DESCRIPTION

The Z86E61/E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32 Kbytes of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-Pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 4 Kbytes of ROM and 236 bytes of general-purpose RAM, the Z86E61/E63 offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/E63 offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/E63 can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration: Program Memory, Data Memory, and 236 general-purpose registers.

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/E63 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Power connections follow conventional descriptions below:

| Connection | Circuit         | Device          |
|------------|-----------------|-----------------|
| Power      | V <sub>CC</sub> | V <sub>DD</sub> |
| Ground     | GND             | V <sub>SS</sub> |

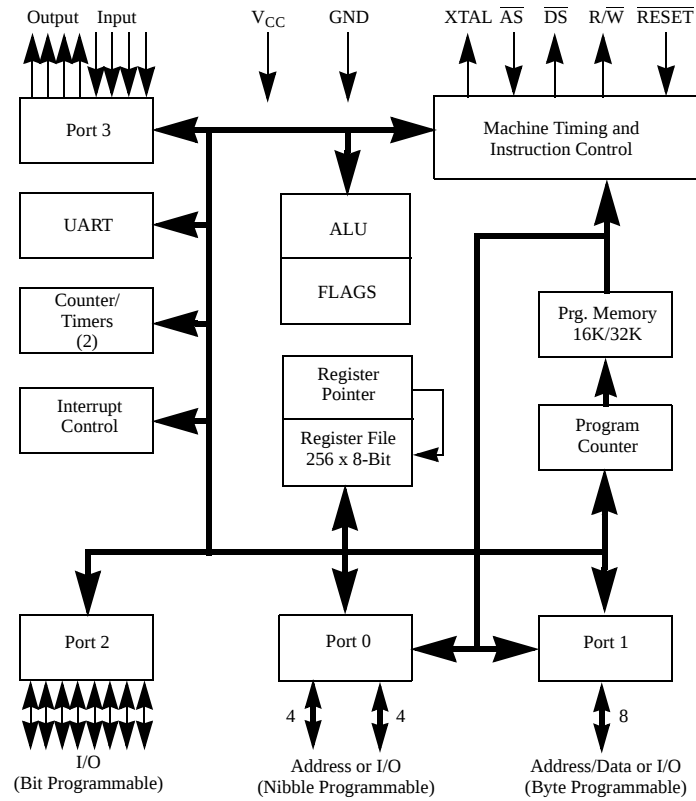
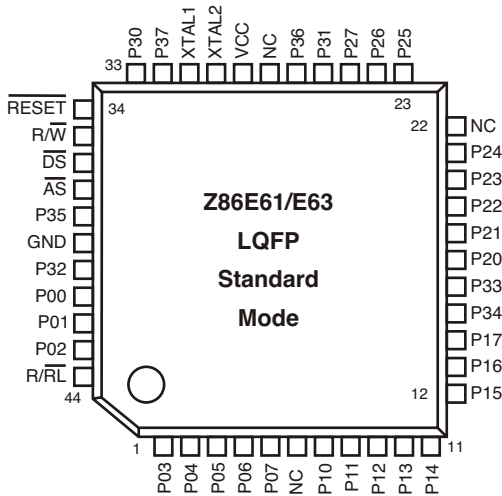
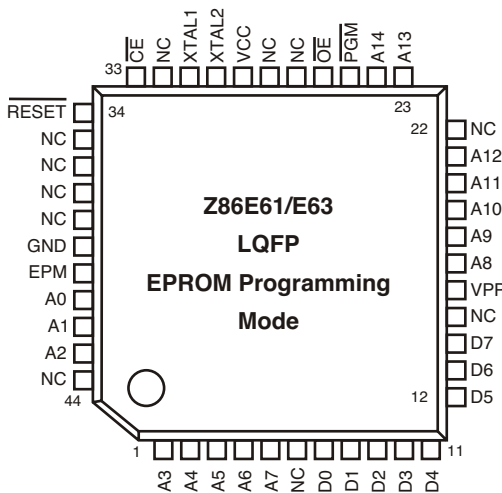


Figure 1. Z86E61/E63 Functional Block Diagram



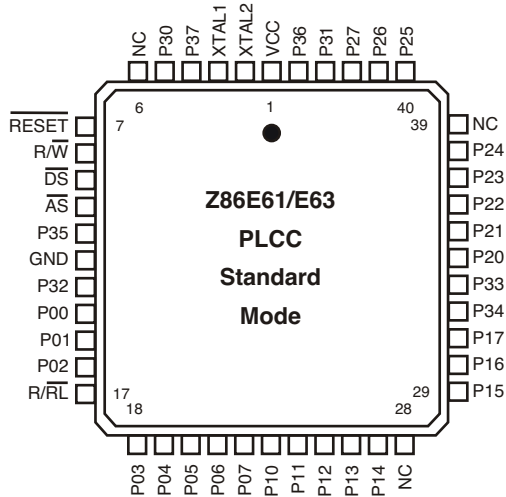
### Pin Description - Standard Mode

|                |                          |              |
|----------------|--------------------------|--------------|
| XTAL2          | Crystal Oscillator Clock | Output       |
| XTAL1          | Crystal Oscillator Clock | Input        |
| RESET          | Reset                    | Input        |
| R/W            | Read/Write               | Output       |
| DS             | Data Strobe              | Output       |
| AS             | Address Strobe           | Output       |
| P00-P07 Port 0 | 8 bit Genaral IO         | Input/Output |
| P10-P17 Port 1 | 8 bit Genaral IO         | Input/Output |
| P20-P27 Port 2 | 8 bit Genaral IO         | Input/Output |
| P30-P33 Port 3 | 4 bit Input              | Input        |
| P34-P37 Port 3 | 4 bit Output             | Output       |
| R/RL           | ROM/ROMless Ctrl         | Input        |
| GND            | Ground                   | Input        |
| VCC            | Power Supply             | Input        |



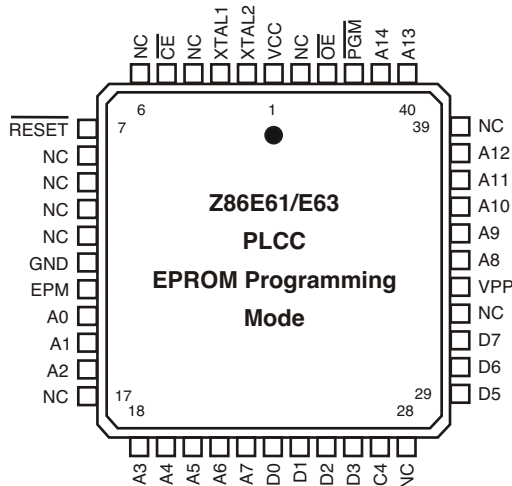
### Pin Description - EPROM Programming Mode

|        |                          |              |
|--------|--------------------------|--------------|
| XTAL2  | Crystal Oscillator Clock | Output       |
| XTAL1  | Crystal Oscillator Clock | Input        |
| CE     | Chip Enable              | Input        |
| RESET  | Reset                    | Input        |
| EPM    | EPROM Prog Mode          | Input        |
| A0-A14 | 15-bit Address bus       | Input        |
| D7-D0  | 8-bit Data bus           | Input/Output |
| VPP    | Prog Voltage             | Input        |
| PGM    | Prog Mode                | Input        |
| OE     | Output Enable            | Input        |
| NC     | Not Connected            | Input        |
| GND    | Ground                   | Input        |
| VCC    | Power Supply             | Input        |



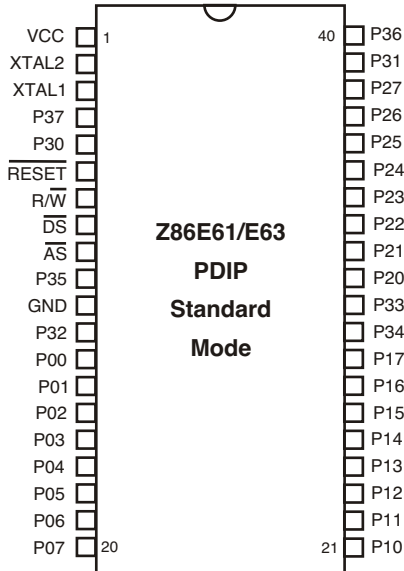
### Pin Description - Standard Mode

|                |                          |              |
|----------------|--------------------------|--------------|
| XTAL2          | Crystal Oscillator Clock | Output       |
| XTAL1          | Crystal Oscillator Clock | Input        |
| RESET          | Reset                    | Input        |
| R/W            | Read/Write               | Output       |
| DS             | Data Strobe              | Output       |
| AS             | Address Strobe           | Output       |
| P00-P07 Port 0 | 8 bit Genaral IO         | Input/Output |
| P10-P17 Port 1 | 8 bit Genaral IO         | Input/Output |
| P20-P27 Port 2 | 8 bit Genaral IO         | Input/Output |
| P30-P33 Port 3 | 4 bit Input              | Input        |
| P34-P37 Port 3 | 4 bit Output             | Output       |
| R/RL           | ROM/ROMless Ctrl         | Input        |
| GND            | Ground                   | Input        |
| VCC            | Power Supply             | Input        |



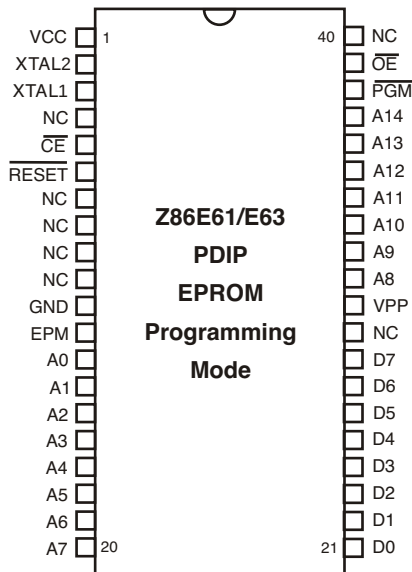
### Pin Description - EPROM Programming Mode

|        |                          |              |
|--------|--------------------------|--------------|
| XTAL2  | Crystal Oscillator Clock | Output       |
| XTAL1  | Crystal Oscillator Clock | Input        |
| CE     | Chip Enable              | Input        |
| RESET  | Reset                    | Input        |
| EPM    | EPROM Prog Mode          | Input        |
| A0-A14 | 15-bit Address bus       | Input        |
| D7-D0  | 8-bit Data bus           | Input/Output |
| VPP    | Prog Voltage             | Input        |
| PGM    | Prog Mode                | Input        |
| OE     | Output Enable            | Input        |
| NC     | Not Connected            | Input        |
| GND    | Ground                   | Input        |
| VCC    | Power Supply             | Input        |



### Pin Description - Standard Mode

|                |                          |              |
|----------------|--------------------------|--------------|
| XTAL2          | Crystal Oscillator Clock | Output       |
| XTAL1          | Crystal Oscillator Clock | Input        |
| RESET          | Reset                    | Input        |
| R/W            | Read/Write               | Output       |
| DS             | Data Strobe              | Output       |
| AS             | Address Strobe           | Output       |
| P00-P07 Port 0 | 8 bit Genaral IO         | Input/Output |
| P10-P17 Port 1 | 8 bit Genaral IO         | Input/Output |
| P20-P27 Port 2 | 8 bit Genaral IO         | Input/Output |
| P30-P33 Port 3 | 4 bit Input              | Input        |
| P34-P37 Port 3 | 4 bit Output             | Output       |
| GND            | Ground                   | Input        |
| VCC            | Power Supply             | Input        |



### Pin Description - EPROM Programming Mode

|        |                          |              |
|--------|--------------------------|--------------|
| XTAL2  | Crystal Oscillator Clock | Output       |
| XTAL1  | Crystal Oscillator Clock | Input        |
| CE     | Chip Enable              | Input        |
| RESET  | Reset                    | Input        |
| EPM    | EPROM Prog Mode          | Input        |
| A0-A14 | 15-bit Address bus       | Input        |
| D7-D0  | 8-bit Data bus           | Input/Output |
| VPP    | Prog Voltage             | Input        |
| PGM    | Prog Mode                | Input        |
| OE     | Output Enable            | Input        |
| NC     | Not Connected            | Input        |
| GND    | Ground                   | Input        |
| VCC    | Power Supply             | Input        |



## PIN FUNCTIONS

### ROMless (Input, Active Low).

Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When pulled High to  $V_{CC}$ , the device functions as a normal Z86E61/E63 EPROM version.

► **Note:** This pin is only available on the 44-pin versions of the Z86E61/E63.

### $\overline{DS}$ (Output, Active Low).

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available  $\overline{DS}$  prior to the trailing edge of  $\overline{DS}$ . For WRITE operations, the falling edge of  $\overline{DS}$  indicates that output data is valid.

### $\overline{AS}$ (Output, Active Low).

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of  $\overline{AS}$ . Under program control,  $\overline{AS}$  can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

### XTAL2, XTAL1

*Crystal 2, Crystal 1 (time-based input and output, respectively).* These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

### $\overline{R/W}$ (Output, Write Low).

The Read/Write signal is Low when the MCU is writing to the external program or data memory.

### $\overline{RESET}$ (Input, Active Low).

To avoid asynchronous and noisy reset problems, the Z86E61/E63 is equipped with a reset filter of four external clocks (4TpC). If the external  $\overline{RESET}$  signal is less than 4TpC in duration, no reset occurs.



On the fifth clock after the  $\overline{\text{RESET}}$  is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external  $\overline{\text{RESET}}$ , whichever is longer. During the reset cycle,  $\overline{\text{DS}}$  is held active Low while  $\overline{\text{AS}}$  cycles at a rate of  $T_{\text{pC}}/2$ . When  $\overline{\text{RESET}}$  is deactivated, program execution begins at location 000C (HEX). Power-up reset time must be held low for 50 ms, or until  $V_{\text{CC}}$  is stable, whichever is longer.

### Port 0 (P07-P00)

Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control  $\overline{\text{DAV0}}$  and  $\text{RDY0}$  (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

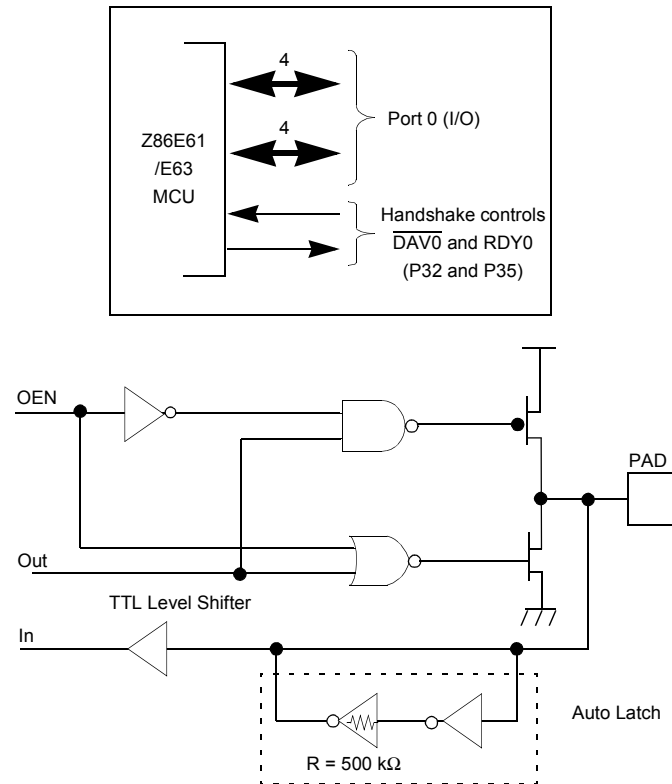
In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 8).

### Port 1 (P17-P10)

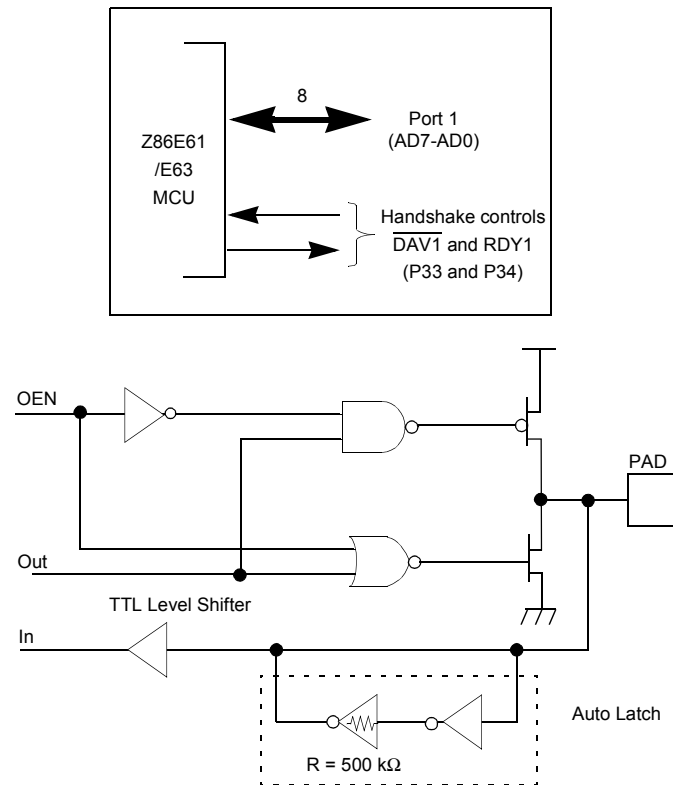
Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86E61/E63, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls  $\text{RDY1}$  and  $\overline{\text{DAV1}}$ .

Memory locations greater than 16384 (E61) or 32768 (E63) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/ Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0,  $\overline{AS}$ ,  $\overline{DS}$ , and  $\overline{R/W}$ , allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output (Figure 7).

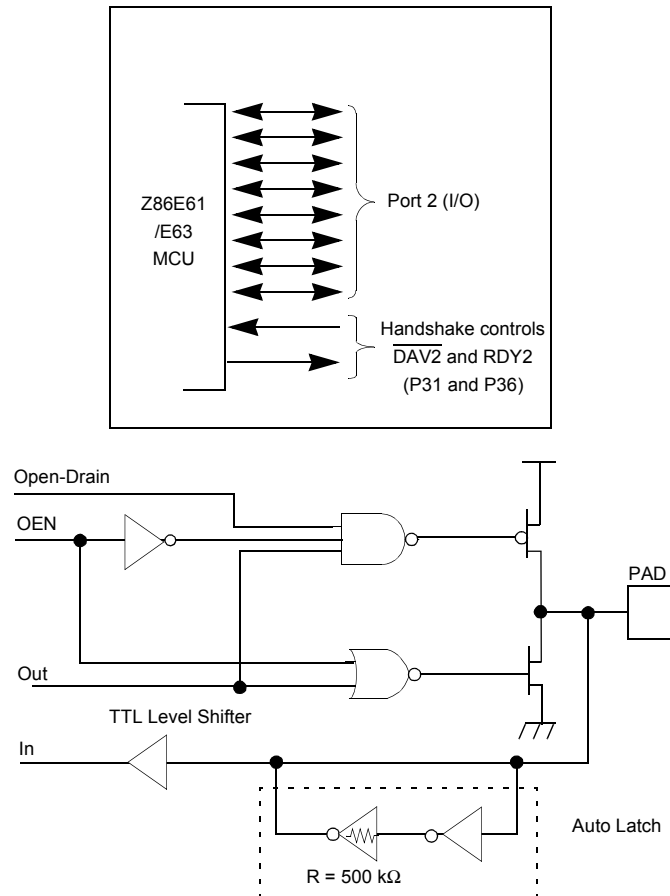


**Figure 6. Port 0 Configuration**



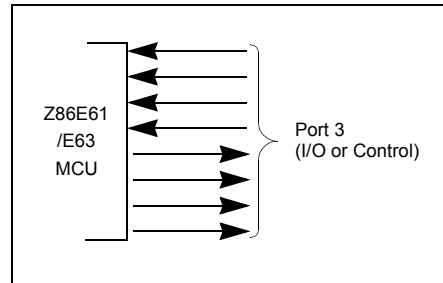
**Figure 7. Port 1 Configuration**

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines  $\overline{\text{DAV2}}$  and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 8 and Table 21 on page 16).



**Figure 8. Port 2 Configuration**

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 9).



**Figure 9. Port 3 Configuration**

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 ( $\overline{DAV}$  and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals ( $T_{IN}$  and  $T_{OUT}$ ) Data Memory Select (/DM) and EPROM control signals (P30 =  $\overline{CE}$ , P31 =  $\overline{OE}$ , P32 = EPM and P33 =  $V_{PP}$ ).

**Table 21. Port 3 Pin Assignments**

| Pin | I/O | CTCI      | Int. | P0 HS | P1 HS | P2 HS | UART       | Ext | EPROM           |
|-----|-----|-----------|------|-------|-------|-------|------------|-----|-----------------|
| P30 | IN  | $T_{IN}$  | IRQ3 |       |       |       | Serial In  |     | $\overline{CE}$ |
| P31 | IN  | $T_{IN}$  | IRQ2 |       |       | D/R   |            |     | $\overline{OE}$ |
| P32 | IN  | $T_{IN}$  | IRQ0 | D/R   |       |       |            |     | EPM             |
| P33 | IN  | $T_{IN}$  | IRQ1 |       | D/R   |       |            |     | $V_{PP}$        |
| P34 | OUT | $T_{OUT}$ |      |       | R/D   |       |            | DM  |                 |
| P35 | OUT | $T_{OUT}$ |      | R/D   |       |       |            |     |                 |
| P36 | OUT | $T_{OUT}$ |      |       |       | R/D   |            |     |                 |
| P37 | OUT | $T_{OUT}$ |      |       |       |       | Serial Out |     |                 |
| T0  |     |           | IRQ4 |       |       |       |            |     |                 |
| T1  |     |           | IRQ5 |       |       |       |            |     |                 |

1. HS = Handshake Signals D = Data Available R = Ready

## UART OPERATION

Port 3 lines, P37 and P30, are programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z86E61/E63 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

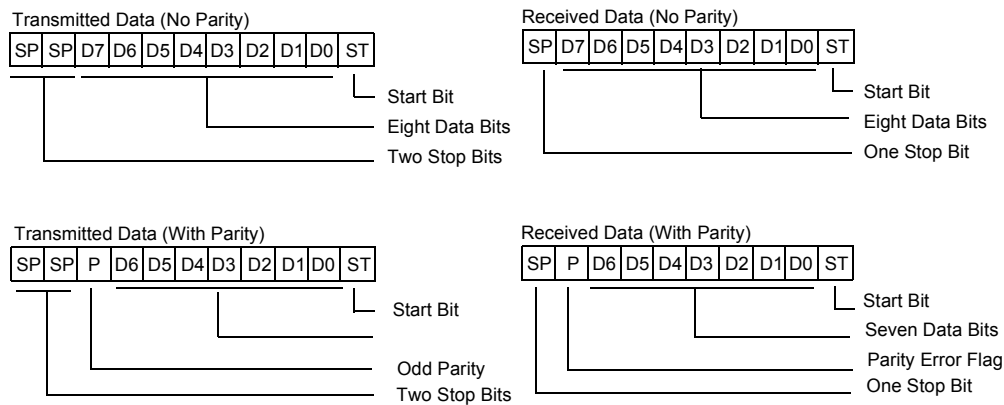


Figure 10. Serial Data Formats

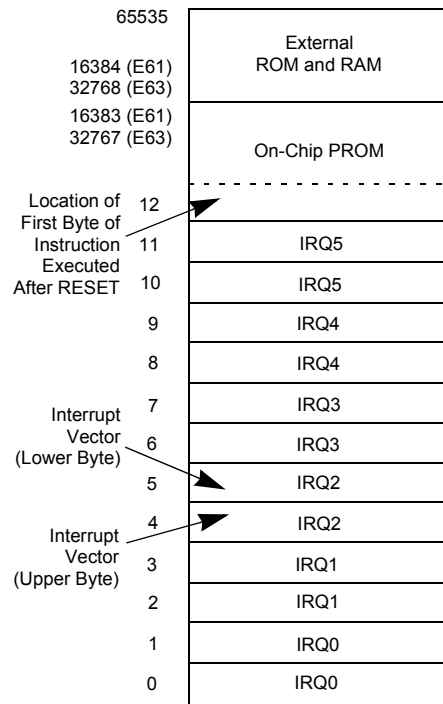
### Auto Latch

The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

- **Note:** P33-P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to  $V_{CC}$  because of the EPROM high voltage detection circuits. Exceeding the  $V_{IH}$  maximum specification during standard operating mode may cause the device to enter EPROM mode.

## ADDRESS SPACE

**Program Memory.** The Z86E61/E63 can address 48 Kbytes (E61) or 32 Kbytes (E63) of external program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 16383 (E61) or 32767 (E63) consists of on-chip EPROM. At addresses 16384 (E61) or 32768 (E63) and above, the Z86E61/E63 executes external program memory fetches. In ROMless mode, the Z86E61/E63 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.



**Figure 11. Program Memory Configuration**

## Data Memory ( $\overline{DM}$ )

The EPROM version can address up to 48 Kbytes (E61) or 32 Kbytes (E63) of external data memory space beginning at location 16384 (E61) or 32768 (E63). The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space.  $\overline{DM}$ , an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory



space (Figure 12). The state of the  $\overline{DM}$  signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM ( $\overline{DM}$  inactive) memory, and an LDE instruction references DATA ( $\overline{DM}$  active Low) memory.

## Register File

The register file consists of four I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 13). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E61/E63 also allows short 4-bit register addressing using the Register Pointer (Figure 14). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

## Stack

The Z86E61/E63 has a 16-bit Stack Pointer (R255-R254) used for external stacks that reside anywhere in the data memory for the ROMless mode, but only from 16384 (E61) or 32768 (E63) to 65535 in the EPROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH Bits 15-8) can be used as a general purpose register when using internal stack only.

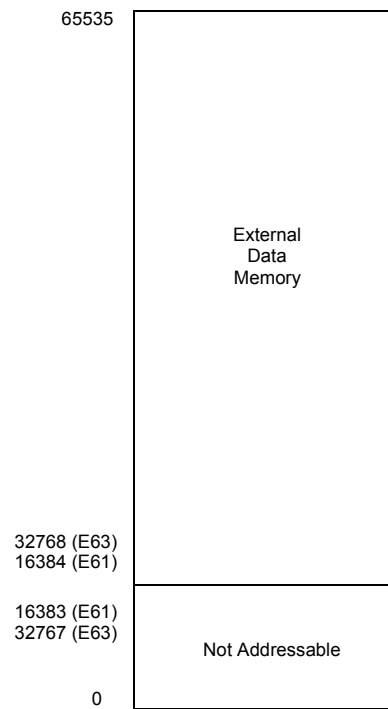


Figure 12. Data Memory Configuration

| LOCATION |                             | IDENTIFIERS |
|----------|-----------------------------|-------------|
| R255     | Stack Pointer (Bits 7-0)    | SPL         |
| R254     | Stack Pointer (Bits 15-8)   | SPH         |
| R253     | Register Pointer            | RP          |
| R252     | Program Control Flags       | FLAGS       |
| R251     | Interrupt Mask Register     | IMR         |
| R250     | Interrupt Request Register  | IRQ         |
| R249     | Interrupt Priority Register | IPR         |
| R248     | Port 0-1 Mode               | P01M        |
| R247     | Port 3 Mode                 | P3M         |
| R246     | Port 2 Mode                 | P2M         |
| R245     | T0 Prescaler                | PRE0        |
| R244     | Timer/Counter0              | T0          |
| R243     | T1 Prescaler                | PRE1        |
| R242     | Timer/Counter1              | T1          |
| R241     | Timer Mode                  | TMR         |
| R240     | Serial I/O                  | SIO         |
| R239     | General Purpose Registers   |             |
| R4       |                             |             |
| R3       |                             | P3          |
| R2       |                             | P2          |
| R1       |                             | P1          |
| R0       | Port 0                      | P0          |

**Figure 13. Register File**

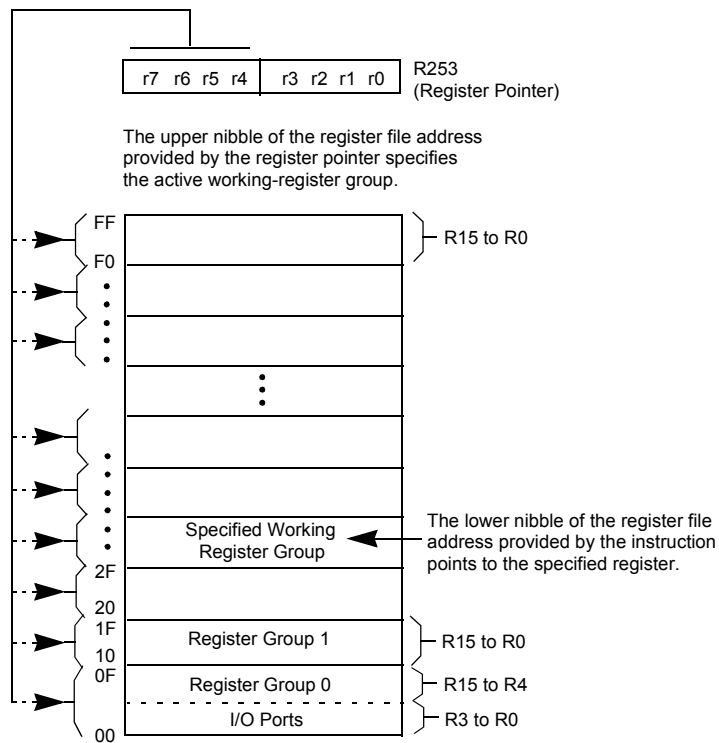


Figure 14. Register Pointer

## FUNCTIONAL DESCRIPTION

### Counter/Timers

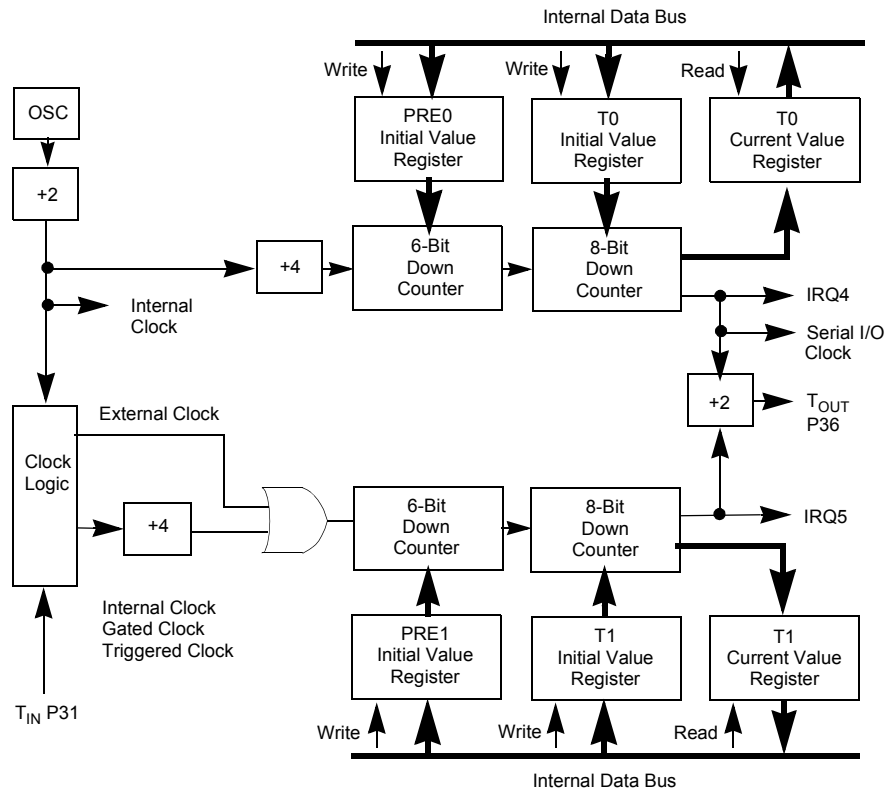
There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero

(single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (TOUT) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.



**Figure 15. Counter/Timers Block Diagram**

## Interrupts

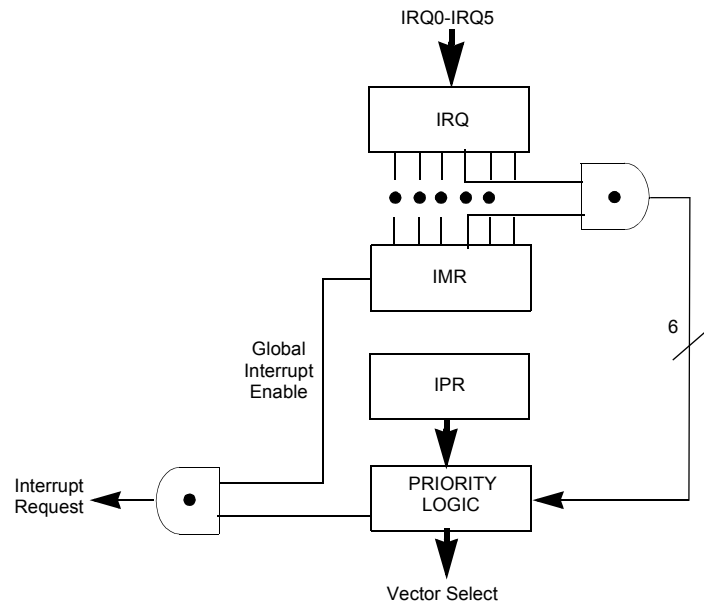
The Z86E61/E63 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally

or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register (refer to Table 21 on page 16).

All Z86E61/E63 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.



**Figure 16. Interrupt Block Diagram**

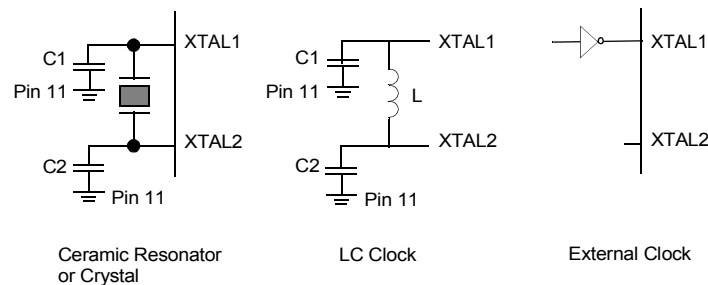
For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the inter-

nal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

## Clock

The Z86E61/E63 on-chip oscillator has a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 16 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors ( $10 \text{ pF} < C_L < 100 \text{ pF}$ ) from each pin to ground (Figure 17).

► **Note:** Actual capacitor value specified by crystal manufacturer.



**Figure 17. Oscillator Configuration**

## HALT

Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

## STOP

This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to  $5 \mu\text{A}$  (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000Ch.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user



must execute a NOP (opcode = 0FFH) immediately before the appropriate SLEEP instruction. i.e.,

|    |      |                      |
|----|------|----------------------|
| FF | NOP  | ; clear the pipeline |
| 6F | STOP | ; enter STOP mode    |
|    | or   |                      |
| FF | NOP  | ; clear the pipeline |
| 7F | HALT | ; enter HALT mode    |

## PROGRAMMING

### Z86E61/E63 User Modes

The Z86E61/E63 uses separate AC timing cycles for the different User Modes available. Table 22 on page 27 shows the Z86E61/E63 User Modes. Table 23 on page 28 shows the timing of the programming waveforms.

#### User MODE 1 EPROM Read

The Z86E61 /E63 EPROM read cycle is provided so that the user may read the Z86E61 /E63 as a standard 27128 (E61) or 27256 (E63) EPROM. This is accomplished by driving the  $\overline{\text{EPM}}$  pin (P32) to VH and activating  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$ .  $\overline{\text{PGM}}$  remains inactive. This mode is not valid after execution of an EPROM protect cycle. Timing for the EPROM read cycle is shown in Figure 18.

#### User MODE 2 EPROM Program

The Z86E61/E63 Program function conforms to the Intelligent programming algorithm. The device is programmed with  $V_{\text{CC}}$ , at 6.0V and  $V_{\text{PP}} = 12.5\text{V}$ . Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E61/E63 programming cycle is shown in Figure 18.

#### User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that  $V_{\text{pp}}$  is active and  $V_{\text{CC}}$  must be driven to 6.0V. Timing is shown in Figure 18.



## User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/E63. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding mode and configuration registers), but first the user's program must set bit 6 of the IMR (R251). Timing is shown in Figure 20 and Figure 21.

User Modes. Table 6 shows the programming voltage of each mode of the Z86E61/E63.

Table 22. OTP Programming<sup>a</sup>

| User/Test Mode<br>Device Pin No. | Device Pins                  |                             |                              |                              |                 |                 |                 | Port 1<br>CNFG<br>Data |
|----------------------------------|------------------------------|-----------------------------|------------------------------|------------------------------|-----------------|-----------------|-----------------|------------------------|
|                                  | P33                          | P32                         | P30                          | P31                          | P20             | ADDR            | V <sub>CC</sub> |                        |
| User Modes                       | V <sub>PP</sub>              | EPM                         | CE                           | OE                           | PGM             | ADDR            | V <sub>CC</sub> |                        |
| EPROM Read                       | V <sub>IH</sub>              | V <sub>H</sub> <sup>c</sup> | V <sub>IL</sub> <sup>d</sup> | V <sub>IL</sub>              | V <sub>IH</sub> | Addr            | 5.0V            | Out                    |
| Program                          | V <sub>PP</sub> <sup>b</sup> | X                           | V <sub>IL</sub>              | V <sub>IH</sub> <sup>e</sup> | V <sub>IL</sub> | Addr            | 6.0V            | In                     |
| Program Verify                   | V <sub>PP</sub> <sup>b</sup> | X                           | V <sub>IL</sub>              | V <sub>IL</sub>              | V <sub>IH</sub> | Addr            | 6.0V            | Out                    |
| EPROM Protect                    | V <sub>PP</sub> <sup>b</sup> | V <sub>H</sub>              | V <sub>H</sub>               | V <sub>IH</sub>              | V <sub>IL</sub> | XX <sup>f</sup> | 6.0V            | XX                     |
| RAM Protect                      | V <sub>PP</sub>              | X                           | V <sub>H</sub>               | V <sub>IH</sub>              | V <sub>IL</sub> | XX <sup>f</sup> | 6.0V            | XX                     |

- a. I<sub>PP</sub> during programming = 40 mA maximum.  
I<sub>CC</sub> during programming, verify, or read = 40 mA maximum.
- b. V<sub>PP</sub> = 12.0 ± 0.5 V.
- c. V<sub>H</sub> = 12.0 ± 0.5 V
- d. V<sub>IL</sub> = 0 V
- e. V<sub>IH</sub> = 5 V.
- f. XX = Irrelevant.

## Z86E63 Signal Description for EPROM Program/Read

The following signals are required to correctly program or read the Z86E63 device.

### ADDR

The address must remain stable throughout the program read cycle.

### DATA

The I/O data bus must be stable during programming ( $\overline{\text{OE}}$  High,  $\overline{\text{PGM}}$  Low, V<sub>PP</sub> High). During read the data bus outputs data.



## XCLK

A clock is required to clock the  $\overline{\text{RESET}}$  signal into the registers before programming.

A constant clock can be applied, or the XCLK input can be toggled a minimum of 12 cycles before any programming or verify function begins. The maximum clock frequency to be applied when in the EPROM mode is 12 MHz.

## $\overline{\text{RESET}}$

The reset input can be held to a constant Low or High value throughout normal programming. It must be held High to program the EPROM protect option bit. Also, any time the  $\overline{\text{RESET}}$  input changes state the XCLK must be clocked a minimum of 12 times to clock the  $\overline{\text{RESET}}$  through the reset filter.

## $\overline{\text{OE}}$

When the device is placed in EPROM mode, the  $\overline{\text{OE}}$  input also serves as the precharge for the sense amp. The precharge signal should be Low for the first half of the stable address and High for the second half. The PRECHG signal is inverted from the  $\overline{\text{OE}}$  signal so the  $\overline{\text{OE}}$  should be High on the first half and Low on the second half, or stable address. The EPROM output data should be sampled during the second half of stable address.

The access time of the EPROM is defined in later sections. This two part calculation of access time is required because this is a precharged sense amp with a precharge clock.

**Table 23. Timing of Programming Waveforms**

| Parameters | Name                              | Min  | Max | Units         |
|------------|-----------------------------------|------|-----|---------------|
| 1          | Address Setup Time                | 2    |     | $\mu\text{s}$ |
| 2          | Data Setup Time                   | 2    |     | $\mu\text{s}$ |
| 3          | $V_{PP}$ Setup                    | 2    |     | $\mu\text{s}$ |
| 4          | $V_{CC}$ Setup Time               | 2    |     | $\mu\text{s}$ |
| 5          | Chip Enable Setup Time            | 2    |     | $\mu\text{s}$ |
| 6          | Program Pulse Width               | 0.95 |     | ms            |
| 7          | Data Hold Time                    | 2    |     | $\mu\text{s}$ |
| 8          | $\overline{\text{OE}}$ Setup Time | 2    |     | $\mu\text{s}$ |
| 9          | Data Access Time                  |      | 200 | ns            |
| 10         | Data Output Float Time            |      | 100 | ns            |

Table 23. Timing of Programming Waveforms (Continued)

| Parameters | Name                                         | Min  | Max | Units   |
|------------|----------------------------------------------|------|-----|---------|
| 11         | Over program Pulse Width                     | 2.85 |     | ms      |
| 12         | EPM Setup Time                               | 2    |     | $\mu$ s |
| 13         | $\overline{\text{PGM}}$ Setup Time           | 2    |     | $\mu$ s |
| 14         | Address to $\overline{\text{OE}}$ Setup Time | 2    |     | $\mu$ s |
| 15         | Option Program Pulse Width                   | 78   |     | ms      |

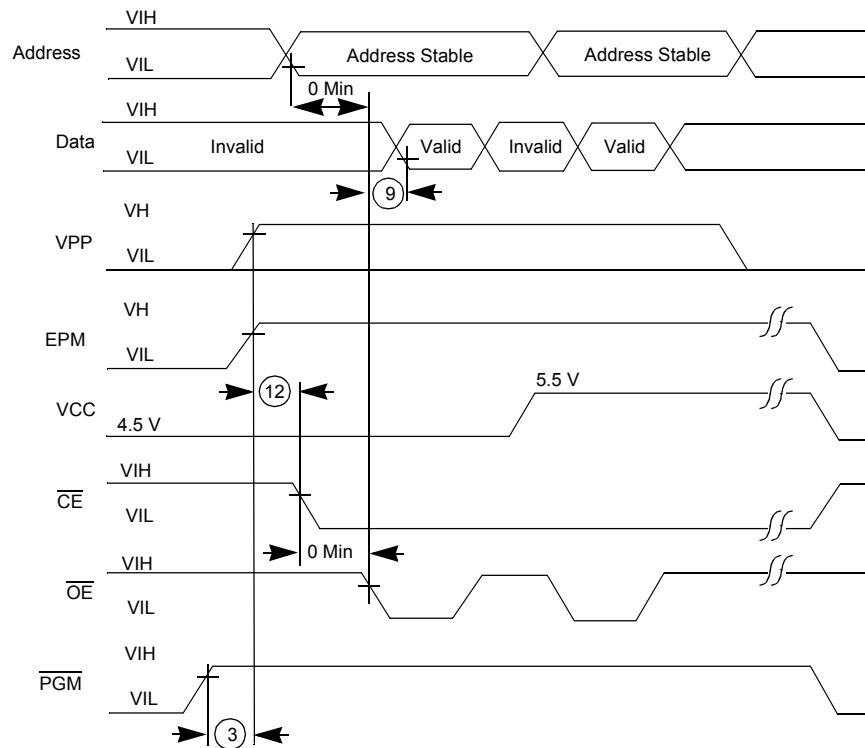


Figure 18. EPROM Read

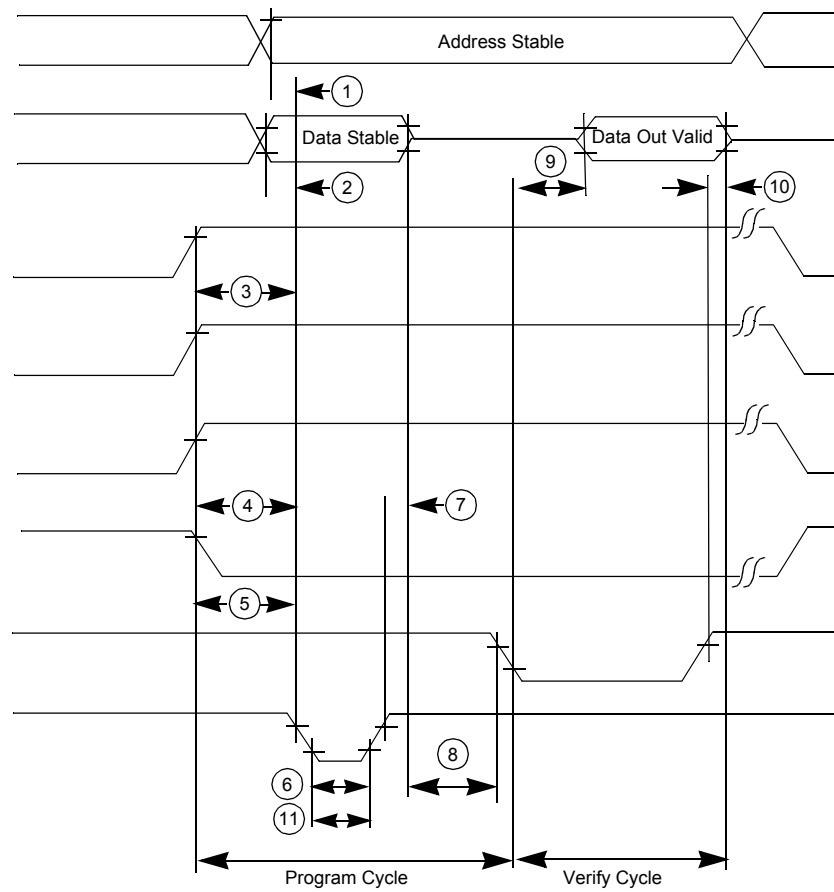
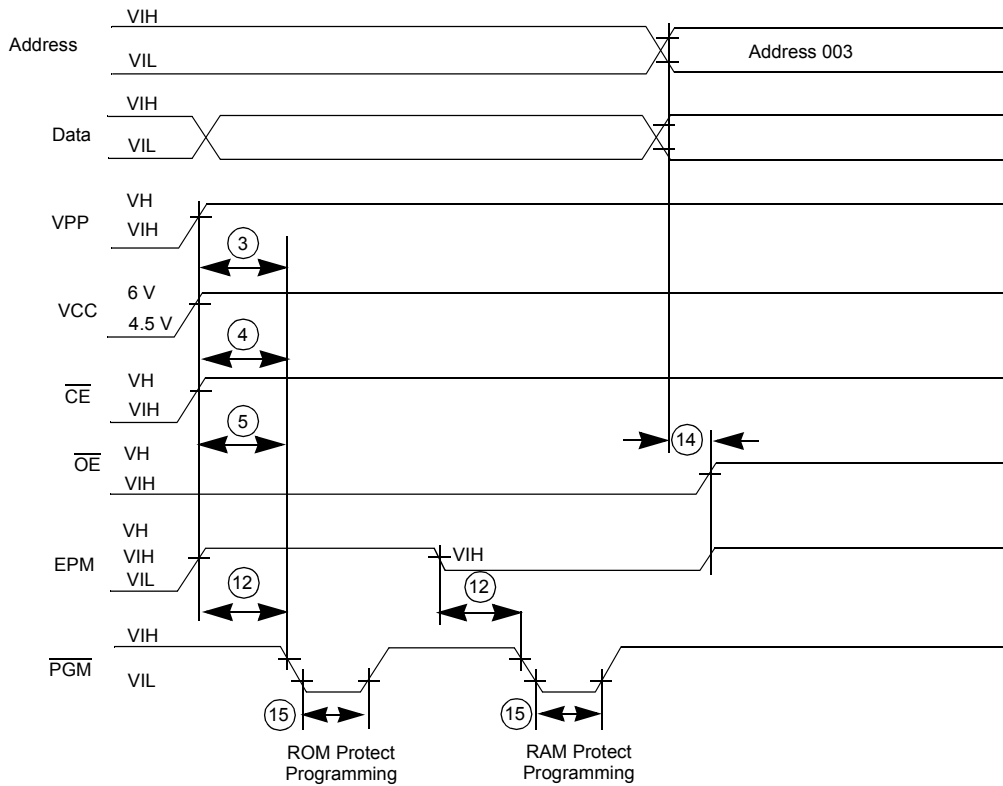
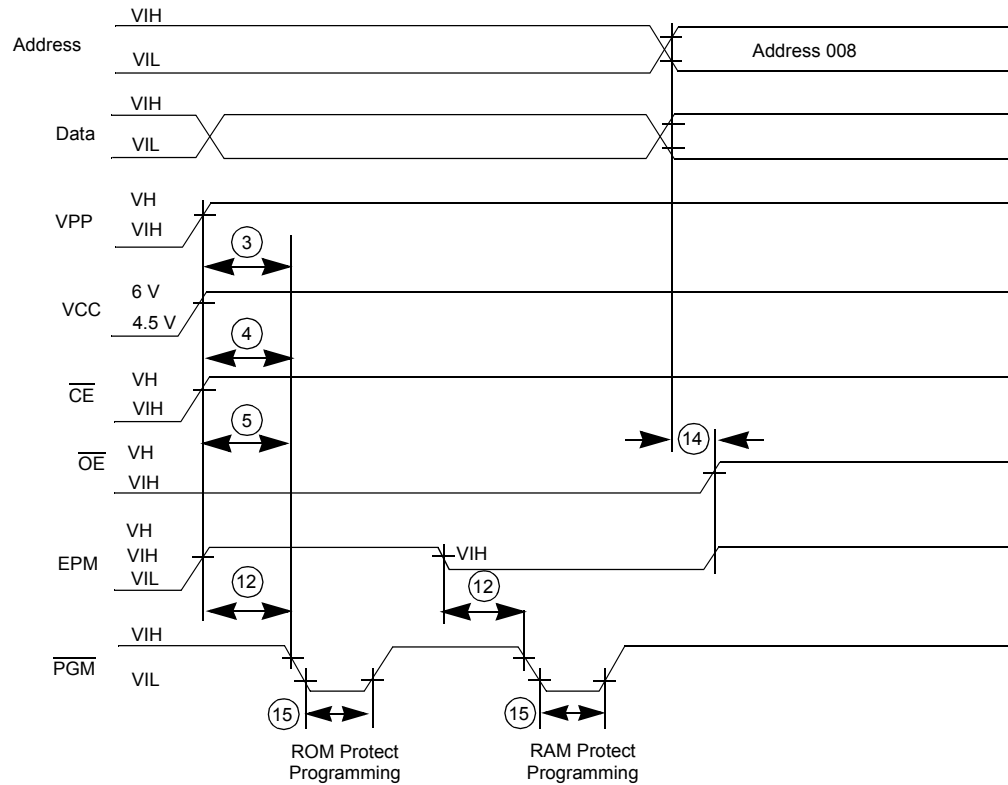


Figure 19. EPROM Program and Verity



**Figure 20. Programming EPROM, RAM Protect, and 4K Size Selection**



**Figure 21. Programming EPROM, RAM Protect, and 16K Size Selection**

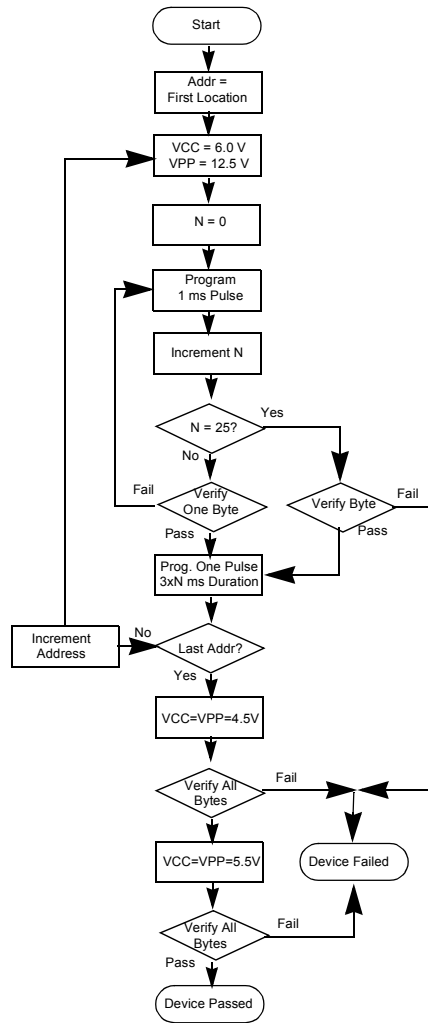


Figure 22. Intelligent Programming Flowchart

## ABSOLUTE MAXIMUM RATINGS

Table 24. Absolute Maximum Ratings

| Symbol    | Description                 | Min  | Max   | Units |
|-----------|-----------------------------|------|-------|-------|
| $V_{CC}$  | Supply Voltage <sup>a</sup> | -0.3 | + 7.0 | V     |
| $T_{STG}$ | Storage Temp                | -65  | +150  | °C    |

**Table 24. Absolute Maximum Ratings (Continued)**

| Symbol | Description                   | Min | Max               | Units |
|--------|-------------------------------|-----|-------------------|-------|
| $T_A$  | Operating Ambient Temperature |     | Note <sup>b</sup> | °C    |

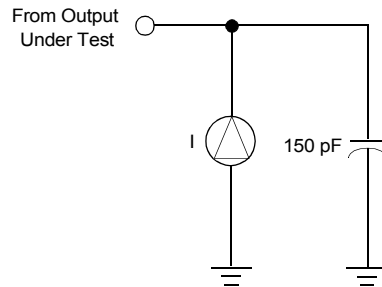
a. Voltages on all pins with respect to GND.

b. See See "ORDERING INFORMATION" on page 62.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 23).



**Figure 23. Test Load Diagram**



## DC CHARACTERISTICS

Table 25. DC Characteristics

| Sym         | Parameter                | $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$ |                | Typical<br>@ 25 °C | Units         | Conditions                                          |
|-------------|--------------------------|------------------------------------------------------------------|----------------|--------------------|---------------|-----------------------------------------------------|
|             |                          | Min                                                              | Max            |                    |               |                                                     |
|             | Max Input Voltage        |                                                                  | 7              |                    | V             | $I_{IN} = 250\text{ }\mu\text{A}$                   |
|             | Max Input Voltage        |                                                                  | 13             |                    | V             | P33-P30 Only                                        |
| $V_{CH}$    | Clock Input High Voltage | 3.8                                                              | $V_{CC} + 0.3$ |                    | V             | Driven by External Clock Generator                  |
| $V_{CL}$    | Clock Input Low Voltage  | -0.3                                                             | 0.8            |                    | V             | Driven by External Clock Generator                  |
| $V_{IH}$    | Input High Voltage       | 2.0                                                              | $V_{CC} + 0.3$ |                    | V             |                                                     |
| $V_{IL}$    | Input Low Voltage        | -0.3                                                             | 0.8            |                    | V             |                                                     |
| $V_{OH}$    | Output High Voltage      | 2.4                                                              |                |                    | V             | $I_{OH} = -2.0\text{ mA}$                           |
| $V_{OL}$    | Output Low Voltage       |                                                                  | 0.4            |                    | V             | $I_{OL} = +2.0\text{ mA}$                           |
| $V_{RH}$    | Reset Input High Voltage | 3.8                                                              | $V_{CC} + 0.3$ |                    | V             |                                                     |
| $V_{RI}$    | Reset Input Low Voltage  | -0.3                                                             | 0.8            |                    | V             |                                                     |
| $I_{IL}$    | Input Leakage            | -10                                                              | 10             |                    | $\mu\text{A}$ | 0 V $V_{IN} + 5.25\text{ V}$                        |
| $I_{OL}$    | Output Leakage           | -10                                                              | 10             |                    | $\mu\text{A}$ | 0 V $V_{IN} + 5.25\text{ V}$                        |
| $I_{IR}$    | Reset Input Current      |                                                                  | -50            |                    | $\mu\text{A}$ | $V_{CC} = +5.25\text{ V}$ , $V_{RL} = 0\text{ V}$   |
| $I_{CC}$    | Supply Current           |                                                                  | 50             | 25                 | mA            | @ 16 MHz                                            |
|             |                          |                                                                  | 60             | 35                 | mA            | @ 20 MHz                                            |
| $I_{CC1}$   | Standby Current          |                                                                  | 15             | 5                  | mA            | HALT Mode $V_{IN} = 0\text{ V}$ , $V_{CC}$ @ 16 MHz |
|             |                          |                                                                  | 20             | 10                 | mA            | HALT Mode $V_{IN} = 0\text{ V}$ , $V_{CC}$ @ 20 MHz |
| $I_{CC2}^a$ | Standby Current          |                                                                  | 20             | 5                  | $\mu\text{A}$ | STOP Mode $V_{IN} = 0\text{ V}$ , $V_{CC}$ @ 16 MHz |
|             |                          |                                                                  | 20             | 5                  | $\mu\text{A}$ | STOP Mode $V_{IN} = 0\text{ V}$ , $V_{CC}$ @ 20 MHz |

- a. ICC2 requires loading TMR (F1Hh) with any value prior to STOP execution.  
Use this sequence:  
LD TMR,#00  
NOP  
STOP

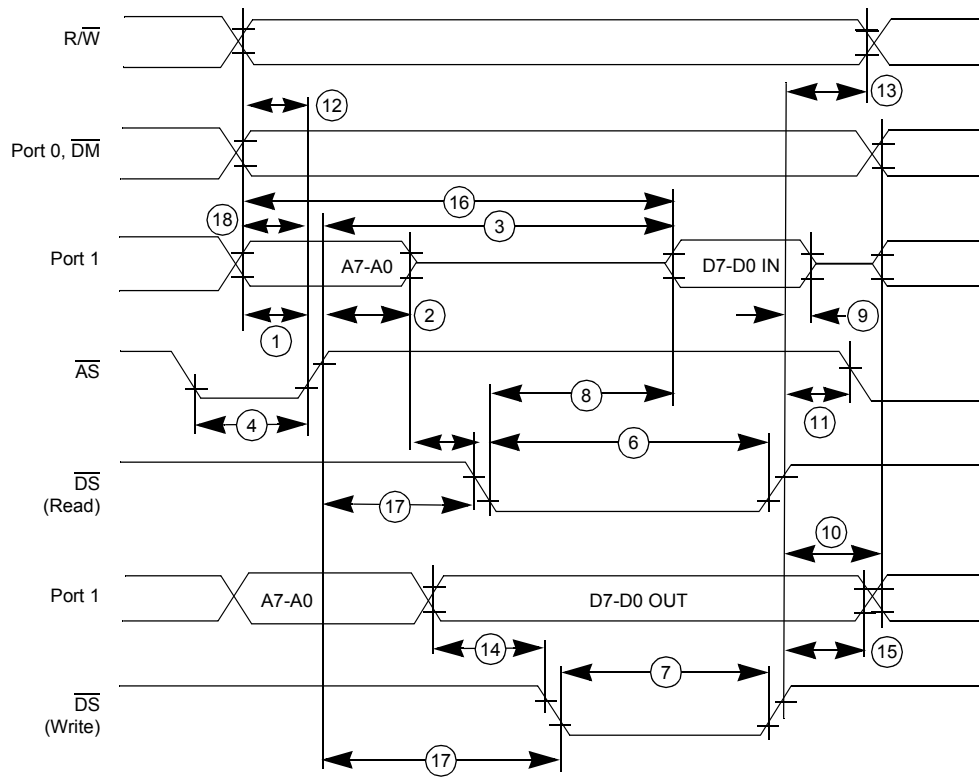


Figure 24. External I/O or Memory Read/Write Timing



## AC CHARACTERISTICS

Table 26. External I/O or Memory Read and Write Timing

|    |            |                                                                   | TA = 0°C to +70°C   |     |        |     |       |                       |
|----|------------|-------------------------------------------------------------------|---------------------|-----|--------|-----|-------|-----------------------|
|    |            |                                                                   | 16 MHz <sup>a</sup> |     | 20 MHz |     |       |                       |
| No | Symbol     | Parameter                                                         | Min                 | Max | Min    | Max | Units | Notes                 |
| 1  | TdA(AS)    | Address Valid to $\overline{\text{AS}}$ Rise Delay                | 20                  |     | 26     |     | ns    | Note <sup>b,c</sup>   |
| 2  | TdAS(A)    | $\overline{\text{AS}}$ Rise to Address Float Delay                | 30                  |     | 28     |     | ns    | Note <sup>b,c</sup>   |
| 3  | TdAS(DR)   | $\overline{\text{AS}}$ Rise to Read Data Req'd Valid              |                     | 180 |        | 160 | ns    | Note <sup>b,c,d</sup> |
| 4  | TwAS       | $\overline{\text{AS}}$ Low Width                                  | 35                  |     | 36     |     | ns    | Note <sup>b,c</sup>   |
| 5  | TdAZ(DS)   | Address Float to $\overline{\text{DS}}$ Fall                      | 0                   |     | 0      |     | ns    |                       |
| 6  | TwDSR      | $\overline{\text{DS}}$ (Read) Low Width                           | 135                 |     | 130    |     | ns    | Note <sup>b,c,d</sup> |
| 7  | TwDSW      | $\overline{\text{DS}}$ (Write) Low Width                          | 80                  |     | 75     |     | ns    | Note <sup>b,c,d</sup> |
| 8  | TdDSR(DR)  | $\overline{\text{DS}}$ Fall to Read Data Req'd Valid              |                     | 75  |        | 100 | ns    | Note <sup>b,c,d</sup> |
| 9  | ThDR(DS)   | Read Data to $\overline{\text{DS}}$ Rise Hold Time                | 0                   |     | 0      |     | ns    | Note <sup>b,c</sup>   |
| 10 | TdDS(A)    | $\overline{\text{DS}}$ Rise to Address Active Delay               | 35                  |     | 48     |     | ns    | Note <sup>b,c</sup>   |
| 11 | TdDS(AS)   | $\overline{\text{DS}}$ Rise to $\overline{\text{AS}}$ Fall Delay  | 30                  |     | 36     |     | ns    | Note <sup>b,c</sup>   |
| 12 | TdR/W(AS)  | R/W Valid to $\overline{\text{AS}}$ Rise Delay                    | 20                  |     | 32     |     | ns    | Note <sup>b,c</sup>   |
| 13 | TdDS(R/W)  | $\overline{\text{DS}}$ Rise to R/W Not Valid                      | 30                  |     | 36     |     | ns    | Note <sup>b,c</sup>   |
| 14 | TdDW(DSW)  | Write Data Valid to $\overline{\text{DS}}$ Fall (Write) Delay     | 25                  |     | 40     |     | ns    | Note <sup>b,c</sup>   |
| 15 | TdDS(DW)   | $\overline{\text{DS}}$ Rise to Write Data Not Valid Delay         | 30                  |     | 40     |     | ns    | Note <sup>b,c</sup>   |
| 16 | TdA(DR)    | Address Valid to Read Data Req'd Valid                            |                     | 200 |        | 200 | ns    | Note <sup>b,c,d</sup> |
| 17 | TdAS(DS)AS | AS Rise to $\overline{\text{DS}}$ Fall Delay                      | 40                  |     | 48     |     | ns    | Note <sup>b,c</sup>   |
| 18 | TdDM(AS)   | $\overline{\text{DM}}$ Valid to $\overline{\text{AS}}$ Fall Delay | 30                  |     | 36     |     | ns    | Note <sup>b,c</sup>   |

- a. All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.  
b. Timing numbers given are for minimum TpC.  
c. See Table 11  
d. When using extended memory timing add 2 TpC.



**Table 27. Clock Dependent Formulas**

| Number | Symbol    | Equation                   |
|--------|-----------|----------------------------|
| 1      | TdA(AS)   | $0.40 \text{ TpC} + 0.32$  |
| 2      | TdAS(A)   | $0.59 \text{ TpC} - 3.25$  |
| 3      | TdAS(DR)  | $2.83 \text{ TpC} + 6.14$  |
| 4      | TwAS      | $0.66 \text{ TpC} - 1.65$  |
| 6      | TwDSR     | $2.33 \text{ TpC} - 10.56$ |
| 7      | TwDSW     | $1.27 \text{ TpC} + 1.67$  |
| 8      | TdDSR(DR) | $1.97 \text{ TpC} - 42.5$  |
| 10     | TdDS(A)   | $0.8 \text{ TpC}$          |
| 11     | TdDS(AS)  | $0.59 \text{ TpC} - 3.14$  |
| 12     | TdR/W(AS) | $0.4 \text{ TpC}$          |
| 13     | TdDS(R/W) | $0.8 \text{ TpC} - 15$     |
| 14     | TdDW(DSW) | $0.4 \text{ sTpC}$         |
| 15     | TdDS(DW)  | $0.88 \text{ TpC} - 19$    |
| 16     | TdA(DR)   | $4 \text{ TpC} - 20$       |
| 17     | TdAS(DS)  | $0.91 \text{ TpC} - 10.7$  |
| 18     | TdDM(AS)  | $0.9 \text{ TpC} - 26.3$   |

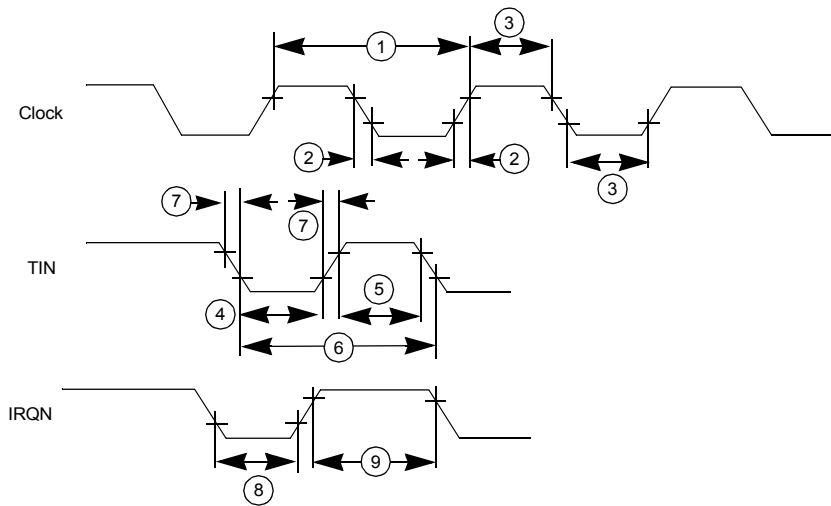


Figure 25. Additional Timing



## AC CHARACTERISTICS

Table 28. Additional Timing

|    |             |                                    | TA = 0°C to +70°C |      |        |      |       |                     |
|----|-------------|------------------------------------|-------------------|------|--------|------|-------|---------------------|
|    |             |                                    | 16 MHz            |      | 20 MHz |      |       |                     |
|    |             |                                    | Min               | Max  | Min    | Max  |       |                     |
| No | Symbol      | Parameter                          | Min               | Max  | Min    | Max  | Units | Notes               |
| 1  | TpC         | Input Clock Period                 | 62.5              | 1000 | 50     | 1000 | ns    | Note <sup>a</sup>   |
| 2  | TrC,TfC     | Clock Input Rise & Fall Times      |                   | 10   |        | 15   | ns    | Note <sup>a</sup>   |
| 3  | TwC         | Input Clock Width                  | 21                |      | 37     |      | ns    | Note <sup>a</sup>   |
| 4  | TwTinL      | Timer Input Low Width              | 50                |      | 75     |      | ns    | Note <sup>b</sup>   |
| 5  | TwTinH      | Timer Input High Width             | 5TpC              |      | 5TpC   |      |       | Note <sup>b</sup>   |
| 6  | TpTin       | Timer Input Period                 | 8TpC              |      | 8TpC   |      |       | Note <sup>b</sup>   |
| 7  | TrTin,TfTin | Timer Input Rise & Fall Times      | 100               |      | 100    |      | ns    | Note <sup>b</sup>   |
| 8A | TwIL        | Interrupt Request Input Low Times  | 70                |      | 50     |      | ns    | Note <sup>b,c</sup> |
| 8B | TwIL        | Interrupt Request Input Low Times  | 5TpC              |      | 5TpC   |      |       | Note <sup>b,d</sup> |
| 9  | TwIH        | Interrupt Request Input High Times | 5TpC              |      | 5TpC   |      |       | Note <sup>b,e</sup> |

- a. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- b. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- c. Interrupt request through Port 3 (P33-P31).
- d. Interrupt request through Port 30.
- e. Interrupt references request through Port 3.

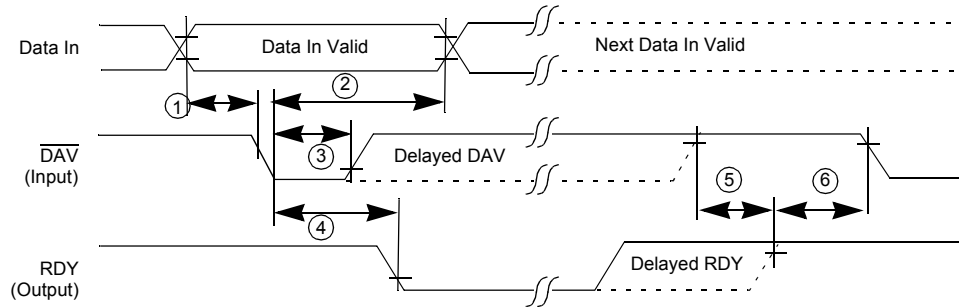


Figure 26. Input Handshake Timing

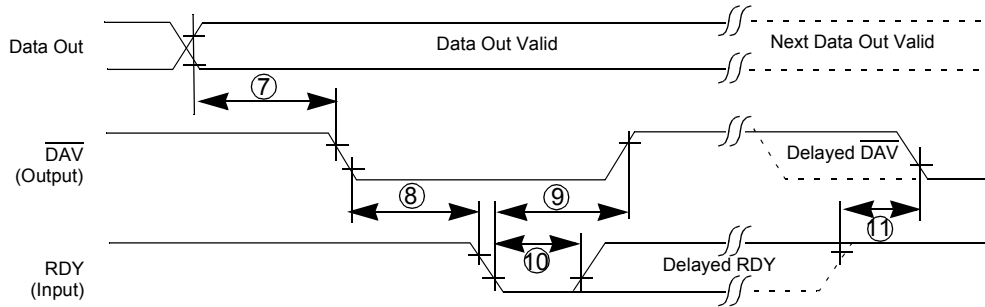


Figure 27. Output Handshake Timing

Table 29. Handshake Timing

| No | Symbol       | Parameter                  | T <sub>A</sub> = 0°C to +70°C |     |        |     | Data Direction |
|----|--------------|----------------------------|-------------------------------|-----|--------|-----|----------------|
|    |              |                            | 16 MHz                        |     | 20 MHz |     |                |
|    |              |                            | Min                           | Max | Min    | Max |                |
| 1  | TsDI(DAV)    | Data In Setup Time         | 0                             |     | 0      |     | IN             |
| 2  | ThDI(DAV)    | Data In Hold Time          | 145                           |     | 145    |     | IN             |
| 3  | TwDAV        | Data Available Width       | 110                           |     | 110    |     | IN             |
| 4  | TdDAVI(RDY)  | DAV Fall to RDY Fall Delay |                               | 115 |        | 115 | IN             |
| 5  | TdDAVId(RDY) | DAV Rise to RDY Rise Delay |                               | 115 |        | 115 | IN             |
| 6  | TdRDY0(DAV)  | RDY Rise to DAV Fall Delay | 0                             |     | 0      |     | IN             |
| 7  | TdD0(DAV)    | Data Out to DAV Fall Delay |                               | TpC |        | TpC | OUT            |



Table 29. Handshake Timing (Continued)

| No | Symbol       | Parameter                  | T <sub>A</sub> = 0°C to +70°C |     |        |     | Data Direction |
|----|--------------|----------------------------|-------------------------------|-----|--------|-----|----------------|
|    |              |                            | 16 MHz                        |     | 20 MHz |     |                |
|    |              |                            | Min                           | Max | Min    | Max |                |
| 8  | TdDAV0(RDY)  | DAV Fall to RDY Fall Delay | 0                             |     | 0      |     | OUT            |
| 9  | TdRDY0(DAV)  | RDY Fall to DAV Rise Delay |                               | 115 |        | 115 | OUT            |
| 10 | TwRDY        | RDY Width                  | 110                           |     | 110    |     | OUT            |
| 11 | TdRDY0d(DAV) | RDY Rise to DAV Fall Delay |                               | 115 |        | 115 | OUT            |

## Z8 CONTROL REGISTER DIAGRAMS

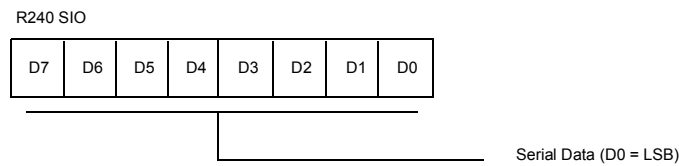


Figure 28. Serial I/O Register (F0H: Read/Write)

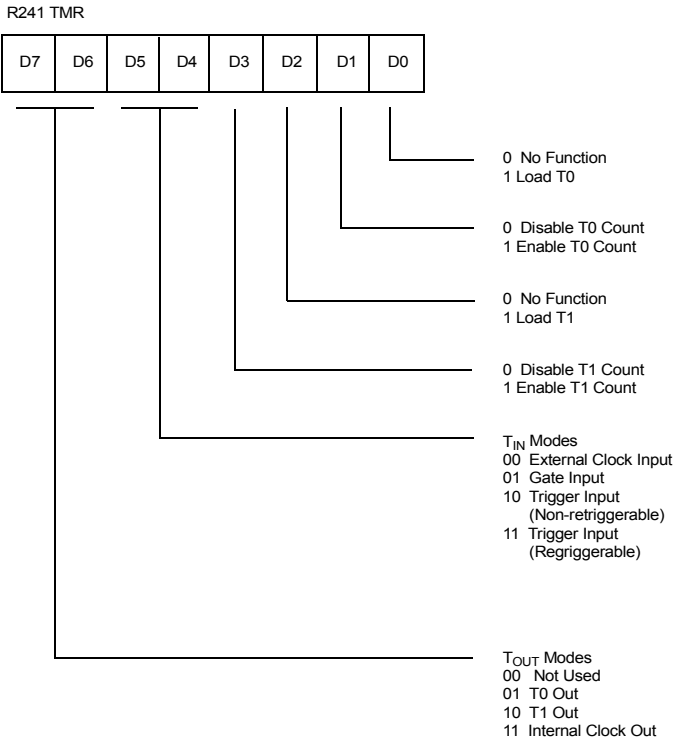


Figure 29. Timer Mode Register (F1<sub>H</sub>: Read/Write)

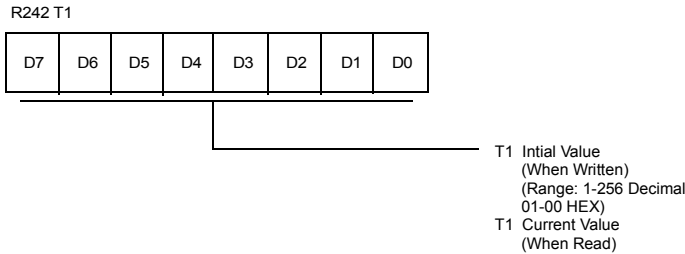
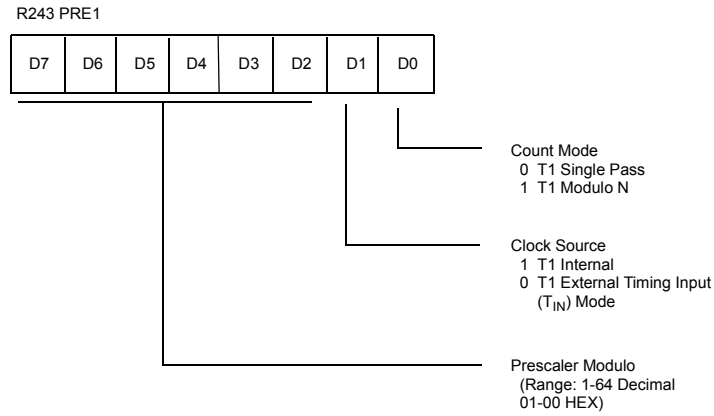
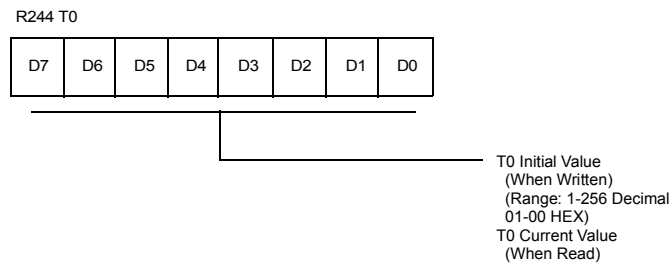


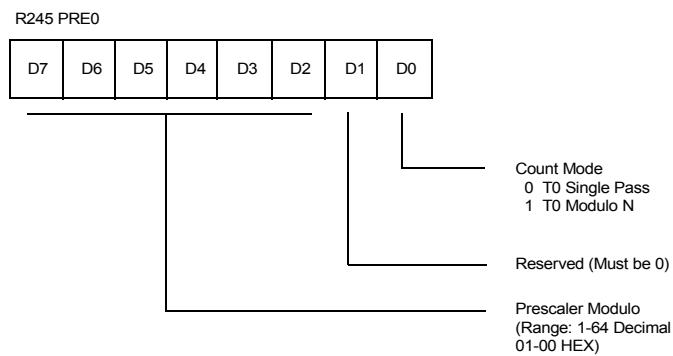
Figure 30. Counter/Timer 1 Register (F2<sub>H</sub>: Read/Write)



**Figure 31. Prescaler 1 Register (F3<sub>H</sub>: Write Only)**



**Figure 32. Counter/Timer 0 Register (F4<sub>H</sub>: Read/Write)**



**Figure 33. Prescaler 0 Register (F5<sub>H</sub>: Write Only)**

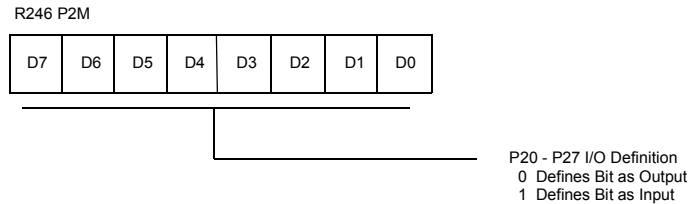


Figure 34. Port 2 Mode Register (F6<sub>H</sub>: Write Only)

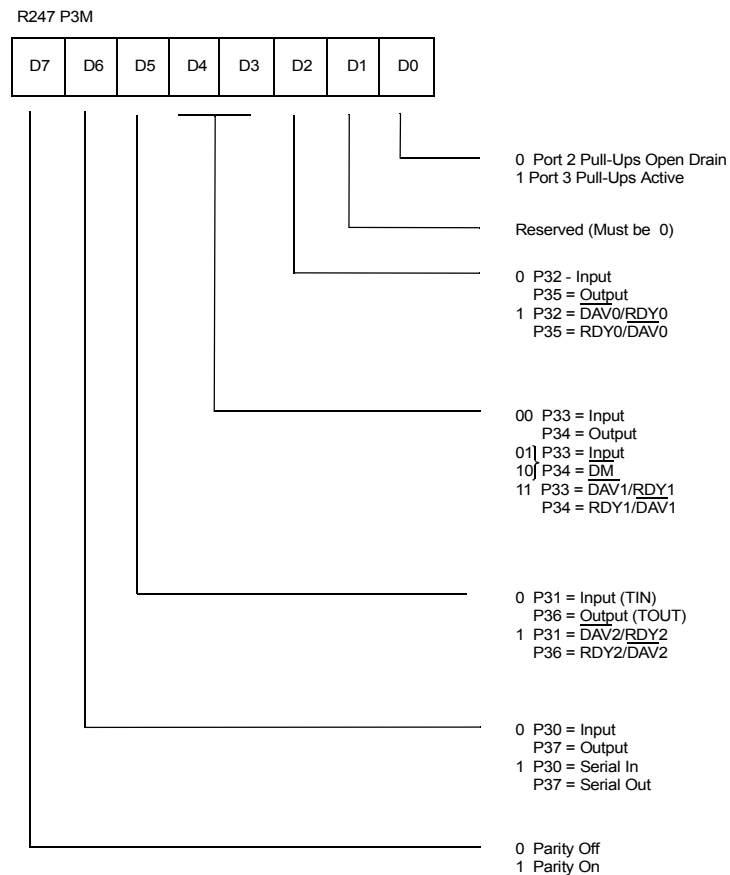


Figure 35. Port 3 Mode Register (F7<sub>H</sub>: Write Only)

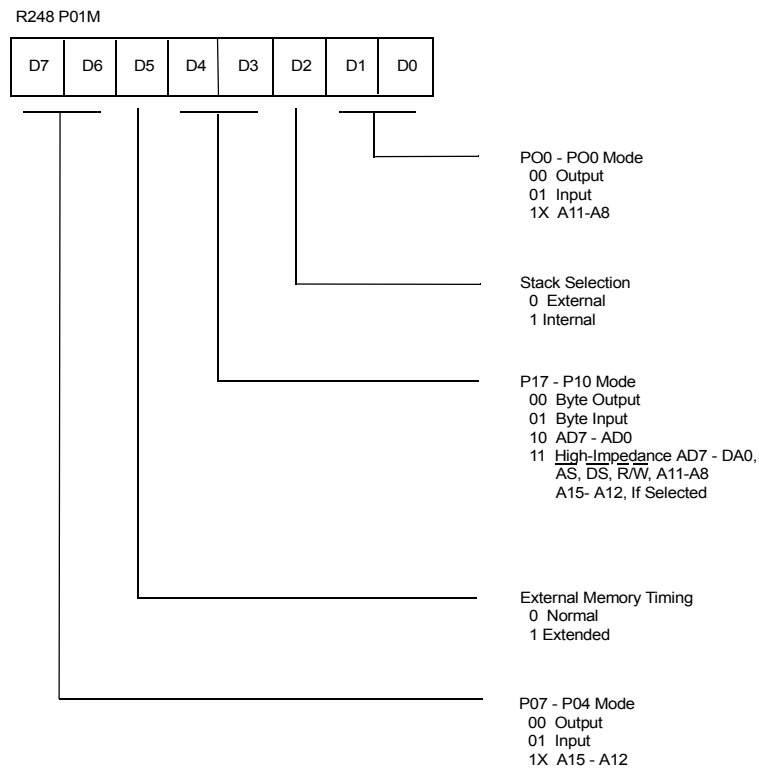
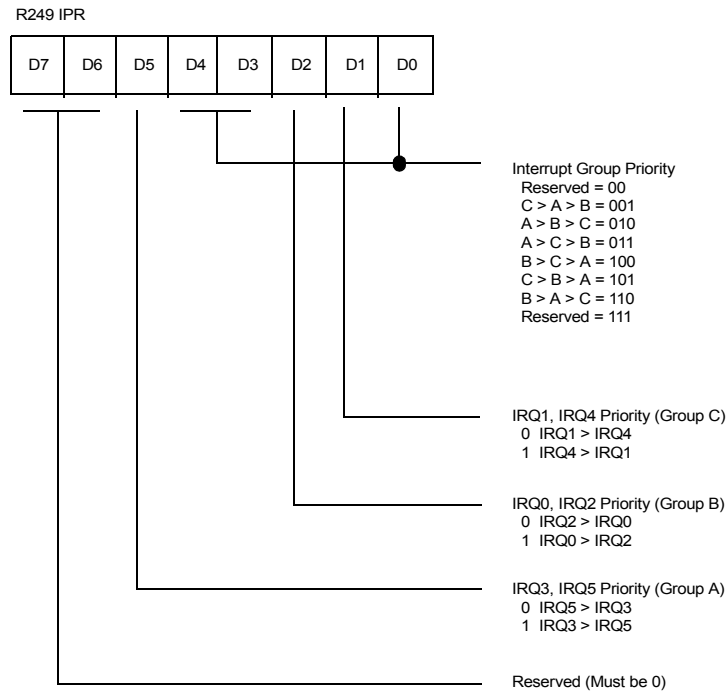
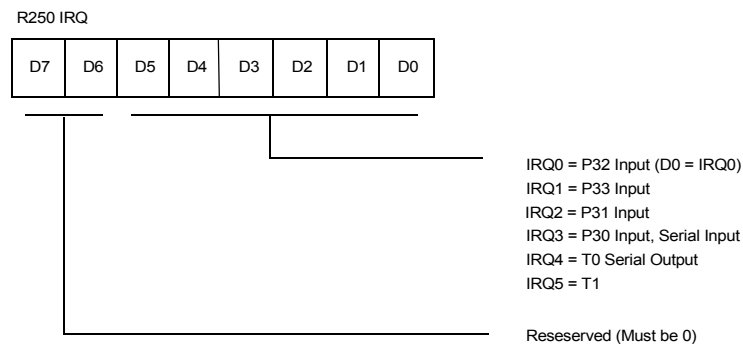


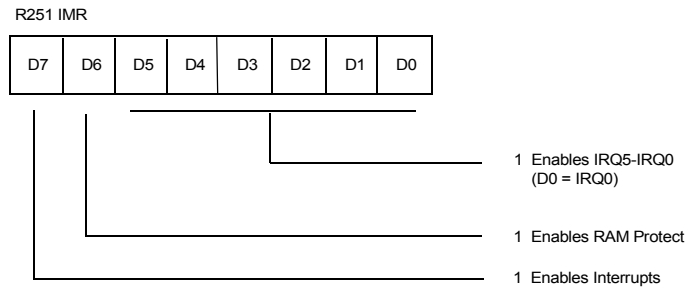
Figure 36. Port 0 and 1 Mode Register (F8<sub>H</sub>: Write Only)



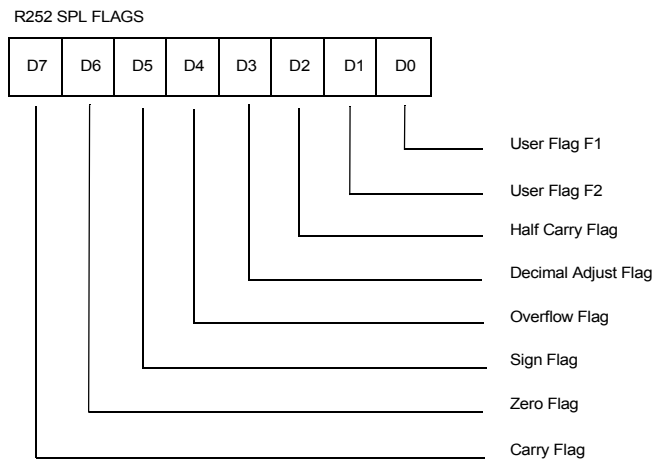
**Figure 37. Interrupt Priority Register (F9<sub>H</sub>: Write Only)**



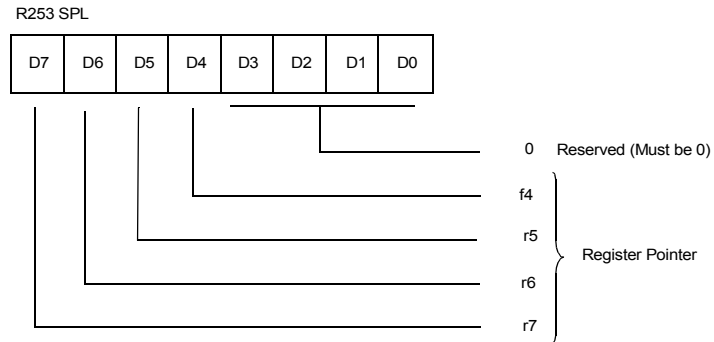
**Figure 38. Interrupt Request Register (FA<sub>H</sub>: Read/Write)**



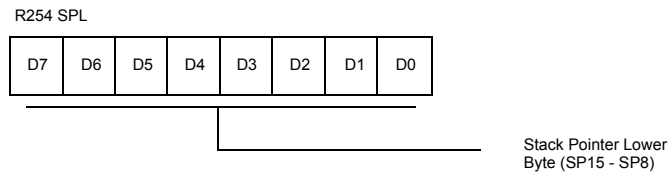
**Figure 39. Interrupt Mask Register (FB<sub>H</sub>: Read/Write)**



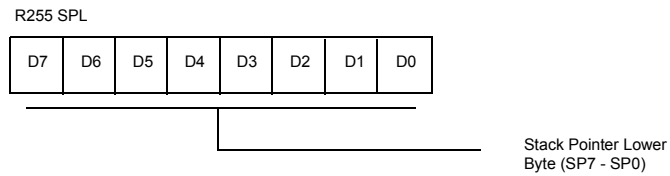
**Figure 40. Flag Register (FC<sub>H</sub>: Read/Write)**



**Figure 41. Register Pointer Register (FD<sub>H</sub>: Read/Write)**



**Figure 42. Stack Pointer Register (FE<sub>H</sub>: Read/Write)**



**Figure 43. Stack Pointer Register (FF<sub>H</sub>: Read/Write)**

## DC CHARACTERISTICS

### Supply Current

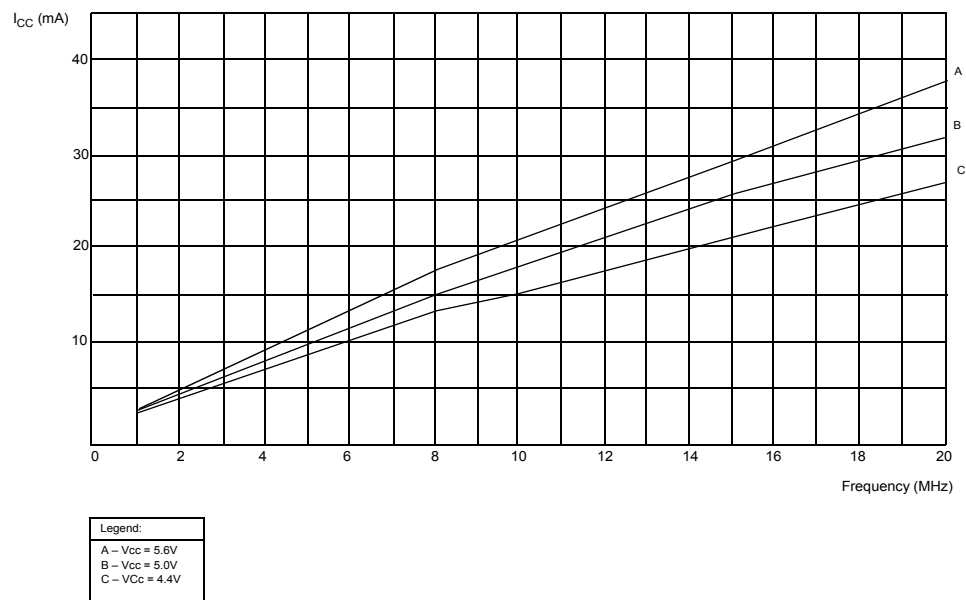


Figure 44. Typical  $I_{CC}$  vs. Frequency

## Standby Current

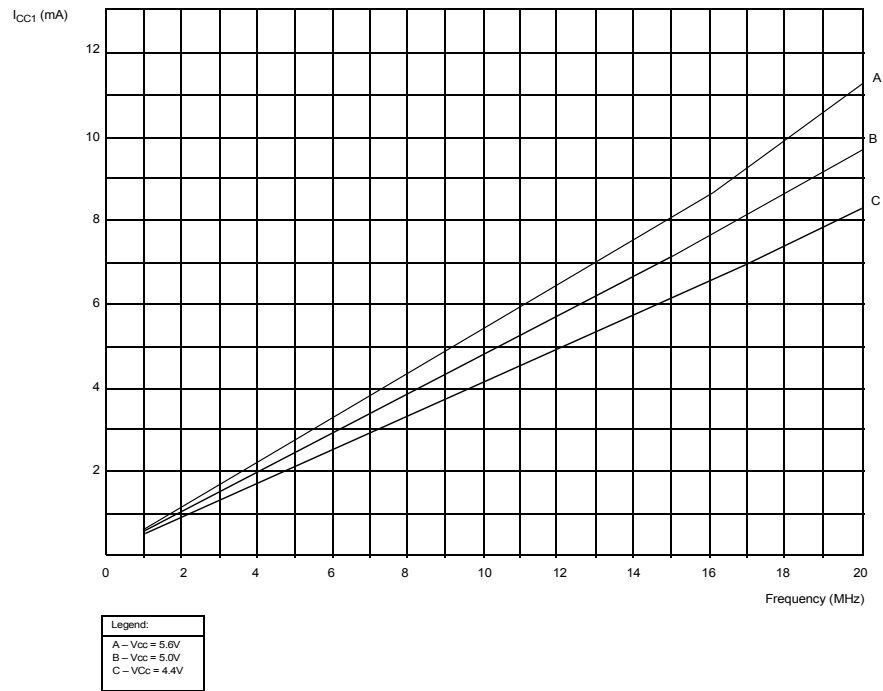


Figure 45. Typical  $I_{CC1}$  vs. Frequency



## INSTRUCTION SET NOTATION

**Addressing Modes.** The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary (Table 14).

**Table 30. Instruction Set Notation**

| Symbol | Meaning                                                          |
|--------|------------------------------------------------------------------|
| IRR    | Indirect register pair or indirect working register pair address |
| Irr    | Indirect working register pair only                              |
| X      | Indexed address                                                  |
| DA     | Direct address                                                   |
| RA     | Relative address                                                 |
| IM     | Immediate                                                        |
| R      | Register or working register address                             |
| r      | Working register address only                                    |
| IR     | Indirect register or indirect working register address           |
| Ir     | Indirect working register address only                           |
| RR     | Register pair or working register pair address                   |

**Symbols.** The following symbols are used in describing the instruction set.

| Symbol | Meaning                              |
|--------|--------------------------------------|
| dst    | Destination location or contents     |
| src    | Source location or contents          |
| cc     | Condition Code                       |
| @      | Indirect address prefix              |
| SP     | Stack Pointer                        |
| PC     | Program Counter                      |
| FLAGS  | Flag Register (Control Register 252) |
| RP     | Register Pointer (R253)              |
| IMR    | Interrupt Mask Register (R251)       |

**Flags.** Control register (R252) contains the following six flags:

| Symbol | Meaning             |
|--------|---------------------|
| C      | Carry flag          |
| Z      | Zero flag           |
| S      | Sign flag           |
| V      | Overflow flag       |
| D      | Decimal-adjust flag |
| H      | Half-carry flag     |

Affected flags are indicated by:

| Symbol | Meaning                             |
|--------|-------------------------------------|
| 0      | Clear to zero                       |
| 1      | Set to one                          |
| *      | Set to clear according to operation |
| -      | Unaffected                          |
| x      | Undefined                           |

## CONDITION CODES

**Table 31. Condition Codes**

| Value | Mnemonic | Meaning               | Flags Set     |
|-------|----------|-----------------------|---------------|
| 1000  |          | Always True           |               |
| 0111  | C        | Carry                 | C = 1         |
| 1111  | NC       | No Carry              | C = 0         |
| 0110  | Z        | Zero                  | Z = 1         |
| 1110  | NZ       | Not Zero              | Z = 0         |
| 1101  | PL       | Plus                  | S = 0         |
| 0101  | MI       | Minus                 | S = 1         |
| 0100  | OV       | Overflow              | V = 1         |
| 1100  | NOV      | No Overflow           | V = 0         |
| 0110  | EQ       | Equal                 | Z = 1         |
| 1110  | NE       | Not Equal             | Z = 0         |
| 1001  | GE       | Greater Than or Equal | (S XOR V) = 0 |



**Table 31. Condition Codes (Continued)**

| Value | Mnemonic | Meaning                        | Flags Set                                |
|-------|----------|--------------------------------|------------------------------------------|
| 0001  | LT       | Less than                      | $(S \text{ XOR } V) = 1$                 |
| 1010  | GT       | Greater Than                   | $[Z \text{ OR } (S \text{ XOR } V)] = 0$ |
| 0010  | LE       | Less Than or Equal             | $[Z \text{ OR } (S \text{ XOR } V)] = 1$ |
| 1111  | UGE      | Unsigned Greater Than or Equal | $C = 0$                                  |
| 0111  | ULT      | Unsigned Less Than             | $C = 1$                                  |
| 1011  | UGT      | Unsigned Greater Than          | $(C = 0 \text{ AND } Z = 0) = 1$         |
| 0011  | ULE      | Unsigned Less Than or Equal    | $(C \text{ OR } Z) = 1$                  |
| 0000  | F        | Never True (Always False)      |                                          |

## INSTRUCTION FORMATS

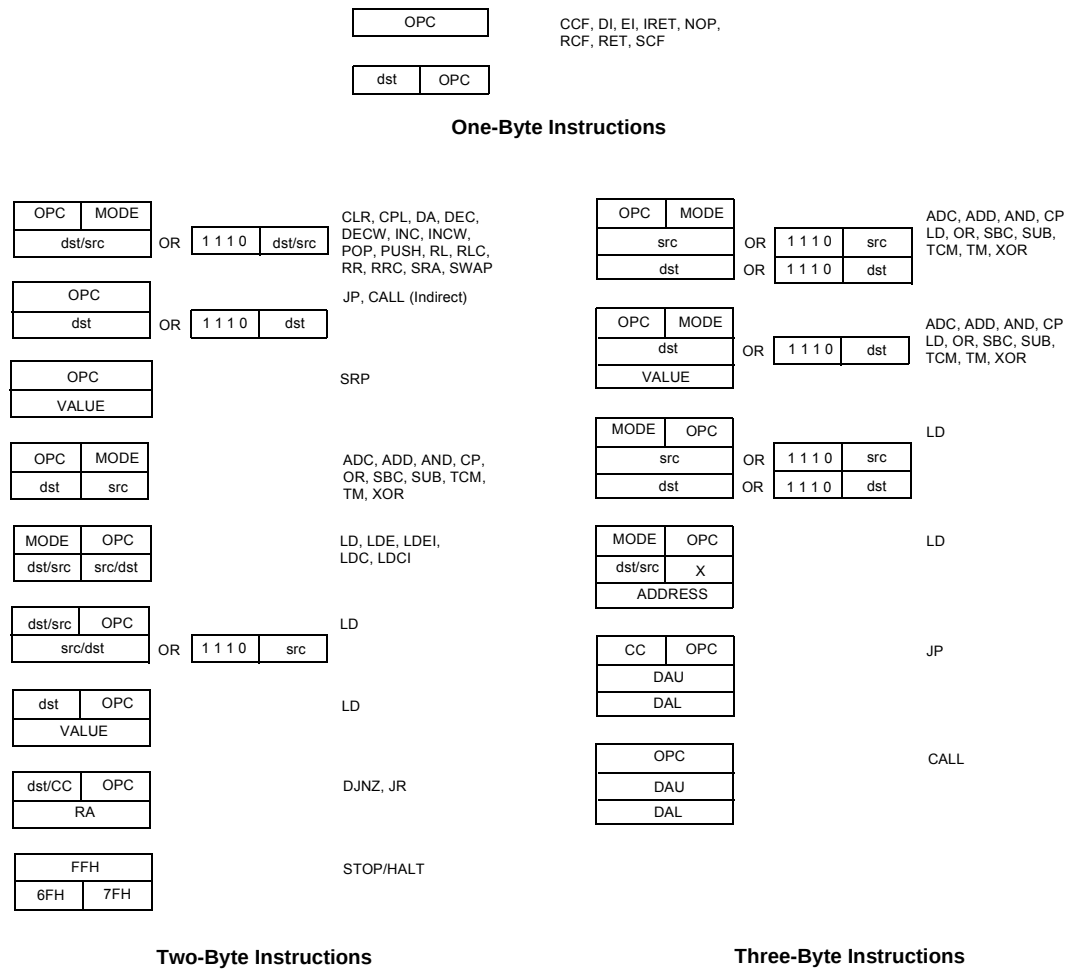


Figure 46. Instruction Formats



## INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " $\leftarrow$ ". For example:

$\text{dst} \leftarrow \text{dst} + \text{src}$

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

$\text{dst} (7)$

refers to bit 7 of the destination operand

**Table 32. Instruction Summary**

| Instruction and Operation                                                                                                          | Address Mode      |     | Opcode Byte (Hex) | Flags Affected |   |   |   |   |   |
|------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----|-------------------|----------------|---|---|---|---|---|
|                                                                                                                                    | dst               | src |                   | C              | Z | S | V | D | H |
| <b>ADC</b> dst, src<br>$\text{dst} \leftarrow \text{dst} + \text{src} + \text{C}$                                                  | Note <sup>a</sup> |     | 1[ ]              | *              | * | * | * | 0 | * |
| <b>ADD</b> dst, src<br>$\text{dst} \leftarrow \text{dst} + \text{src}$                                                             | Note <sup>a</sup> |     | 0[ ]              | *              | * | * | * | 0 | * |
| <b>AND</b> dst, src<br>$\text{dst} \leftarrow \text{dst} \text{ AND } \text{src}$                                                  | Note <sup>a</sup> |     | 5[ ]              | -              | * | * | 0 | - | - |
| <b>CALL</b> dst<br>$\text{SP} \leftarrow \text{SP} - 2$<br>$@\text{SP} \leftarrow \text{PC},$<br>$\text{PC} \leftarrow \text{dst}$ | DA<br>IRR         |     | 06<br>D4          | -              | - | - | - | - | - |
| <b>CCF</b><br>$\text{C} \leftarrow \text{NOT C}$                                                                                   |                   |     | EF                | *              | - | - | - | - | - |
| <b>CLR</b> dst<br>$\text{dst} \leftarrow 0$                                                                                        | R<br>IR           |     | B0<br>B11         | -              | - | - | - | - | - |
| <b>COM</b> dst<br>$\text{dst} \leftarrow \text{NOT dst}$                                                                           | R<br>IR           |     | 60<br>61          | -              | * | * | 0 | - | - |
| <b>CP</b> dst, src<br>$\text{dst} - \text{src}$                                                                                    | Note <sup>a</sup> |     | A[ ]              | *              | * | * | * | - | - |
| DA dst<br>$\text{dst} \leftarrow \text{DA dst}$                                                                                    | R<br>IR           |     | 40<br>41          | *              | * | * | X | - | - |



Table 32. Instruction Summary (Continued)

| Instruction<br>and Operation | Address Mode |     | Opcode<br>Byte (Hex) | Flags Affected |   |   |   |   |   |
|------------------------------|--------------|-----|----------------------|----------------|---|---|---|---|---|
|                              | dst          | src |                      | C              | Z | S | V | D | H |
| <b>DEC</b> dst               | R            |     | 00                   | -              | * | * | * | - | - |
| dst ← dst - 1                | IR           |     | 01                   |                |   |   |   |   |   |
| <b>DECW</b> dst              | RR           |     | 80                   | -              | * | * | * | - | - |
| dst ← dst - 1                | IR           |     | 81                   |                |   |   |   |   |   |
| DI                           |              |     | 8F                   | -              | - | - | - | - | - |
| IMR(7) ← 0                   |              |     |                      |                |   |   |   |   |   |
| <b>DJNZ</b> r, dst           | RA           |     | rA                   | -              | - | - | - | - | - |
| r ← r - 1                    |              |     | r = 0-F              |                |   |   |   |   |   |
| if r ≠ 0                     |              |     |                      |                |   |   |   |   |   |
| PC ← PC + dst                |              |     |                      |                |   |   |   |   |   |
| Range: +127,<br>-128         |              |     |                      |                |   |   |   |   |   |
| EI                           |              |     | 9F                   | -              | - | - | - | - | - |
| IMR(7) ← 1                   |              |     |                      |                |   |   |   |   |   |
| HALT                         |              |     | 7F                   | -              | - | - | - | - | - |
| <b>INC</b> dst               | r            |     | rE                   | -              | * | * | * | - | - |
| dst ← dst + 1                |              |     | r = 0 - F            |                |   |   |   |   |   |
|                              | R            |     | 20                   |                |   |   |   |   |   |
|                              | IR           |     | 21                   |                |   |   |   |   |   |
| <b>INCW</b> dst              | RR           |     | A0                   | -              | * | * | * | - | - |
| dst ← dst + 1                | IR           |     | A1                   |                |   |   |   |   |   |
| IRET                         |              |     | BF                   | *              | * | * | * | * | * |
| FLAGS ← @SP;                 |              |     |                      |                |   |   |   |   |   |
| SP ← SP + 1                  |              |     |                      |                |   |   |   |   |   |
| PC ← @SP;                    |              |     |                      |                |   |   |   |   |   |
| SP ← SP + 2;                 |              |     |                      |                |   |   |   |   |   |
| IMR(7) ← 1                   |              |     |                      |                |   |   |   |   |   |
| <b>JP</b> cc, dst            | DA           |     | cD                   | -              | - | - | - | - | - |



Table 32. Instruction Summary (Continued)

| Instruction<br>and Operation                          | Address Mode      |     | Opcode<br>Byte (Hex) | Flags Affected |   |   |   |   |   |
|-------------------------------------------------------|-------------------|-----|----------------------|----------------|---|---|---|---|---|
|                                                       | dst               | src |                      | C              | Z | S | V | D | H |
| if cc is true,<br>PC←dst                              | IRR               |     | c = 0 - F<br>30      |                |   |   |   |   |   |
| <b>JR</b> cc, dst                                     | RA                |     | cB                   | -              | - | - | - | - | - |
| if cc is true,<br>PC←PC + dst<br>Range: +127,<br>-128 |                   |     | c = 0 - F            |                |   |   |   |   |   |
| <b>LD</b> dst, src                                    | r                 | Im  | rC                   | -              | - | - | - | - | - |
| dst←src                                               | r                 | R   | r8                   |                |   |   |   |   |   |
|                                                       | R                 | r   | r9                   |                |   |   |   |   |   |
|                                                       |                   |     | r = 0-F              |                |   |   |   |   |   |
|                                                       | r                 | X   | C7                   |                |   |   |   |   |   |
|                                                       | X                 | r   | D7                   |                |   |   |   |   |   |
|                                                       | r                 | lr  | E3                   |                |   |   |   |   |   |
|                                                       | lr                | r   | F3                   |                |   |   |   |   |   |
|                                                       | R                 | R   | E4                   |                |   |   |   |   |   |
|                                                       | R                 | IR  | E5                   |                |   |   |   |   |   |
|                                                       | R                 | IM  | E6                   |                |   |   |   |   |   |
|                                                       | IR                | IM  | E7                   |                |   |   |   |   |   |
|                                                       | IR                | R   | F5                   |                |   |   |   |   |   |
| <b>LDC</b> dst, src                                   | r                 | lrr | C2                   | -              | - | - | - | - | - |
| dst←src                                               |                   |     |                      |                |   |   |   |   |   |
| <b>LDCI</b> dst, src                                  | lr                | lrr | C3                   | -              | - | - | - | - | - |
| dst←src                                               |                   |     |                      |                |   |   |   |   |   |
| r←r + 1;<br>rr←rr + 1                                 |                   |     |                      |                |   |   |   |   |   |
| <b>NOP</b>                                            |                   |     | FF                   | -              | - | - | - | - | - |
| <b>OR</b> dst, src                                    | Note <sup>a</sup> |     | 4[ 1                 | -              | * | * | 0 | - | - |



Table 32. Instruction Summary (Continued)

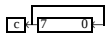
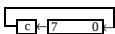
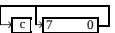
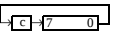
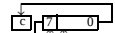
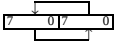
| Instruction and Operation                                                           | Address Mode      |     | Opcode Byte (Hex) | Flags Affected |   |   |   |   |   |
|-------------------------------------------------------------------------------------|-------------------|-----|-------------------|----------------|---|---|---|---|---|
|                                                                                     | dst               | src |                   | C              | Z | S | V | D | H |
| dst←dst OR src                                                                      |                   |     |                   |                |   |   |   |   |   |
| POP                                                                                 | R                 |     | 50                | -              | - | - | - | - | - |
| dst←@SP;<br>SP←SP + 1                                                               | IR                |     | 51                |                |   |   |   |   |   |
| <b>PUSH</b> src                                                                     | R                 |     | 70                | -              | - | - | - | - | - |
| SP←SP-1;<br>@SP←src                                                                 | IR                |     | 71                |                |   |   |   |   |   |
| RCF<br>C←0                                                                          |                   |     | CF                | 0              | - | - | - | - | - |
| RET<br>PC←@SP;<br>SP←SP +2                                                          |                   |     | AF                | -              | - | - | - | - | - |
| <b>RL</b> dst                                                                       | R                 |     | 90                | *              | * | * | * | - | - |
|  | IR                |     | 91                |                |   |   |   |   |   |
| <b>RLC</b> dst                                                                      | R                 |     | 10                | *              | * | * | * | - | - |
|  | IR                |     | 11                |                |   |   |   |   |   |
| <b>RR</b> dst                                                                       | R                 |     | E0                | *              | * | * | * | - | - |
|  | IR                |     | E1                |                |   |   |   |   |   |
| <b>RRC</b> dst                                                                      | R                 |     | C0                | *              | * | * | * | - | - |
|  | IR                |     | C1                |                |   |   |   |   |   |
| <b>SBC</b> dst, src<br>dst←dst←src←C                                                | Note <sup>a</sup> |     | 3[ ]              | *              | * | * | * | 1 | * |
| SCF<br>C←1                                                                          |                   |     | DF                | 1              | - | - | - | - | - |
| <b>SRA</b> dst                                                                      | R                 |     | D0                | *              | * | * | 0 | - | - |
|  | IR                |     | D1                |                |   |   |   |   |   |
| <b>SRP</b> dst                                                                      | Im                |     | 31                | -              | - | - | - | - | - |



Table 32. Instruction Summary (Continued)

| Instruction and Operation                                                         | Address Mode      |     | Opcode Byte (Hex) | Flags Affected |   |   |   |   |   |
|-----------------------------------------------------------------------------------|-------------------|-----|-------------------|----------------|---|---|---|---|---|
|                                                                                   | dst               | src |                   | C              | Z | S | V | D | H |
| RP←src                                                                            |                   |     |                   |                |   |   |   |   |   |
| STOP                                                                              |                   |     | 6F                | 1              | - | - | - | - | - |
| <b>SUB</b> dst, src                                                               | Note <sup>a</sup> |     | 2[ ]              | [              | [ | [ | [ | 1 | [ |
| dst←dst←src                                                                       |                   |     |                   |                |   |   |   |   |   |
| <b>SWAP</b> dst                                                                   | R                 |     | F0                | X              | * | * | X | - | - |
|  | IR                |     | F1                |                |   |   |   |   |   |
| <b>TCM</b> dst, src                                                               | Note <sup>a</sup> |     | 6[ ]              | -              | * | * | 0 | - | - |
| (NOT dst)                                                                         |                   |     |                   |                |   |   |   |   |   |
| AND src                                                                           |                   |     |                   |                |   |   |   |   |   |
| <b>TM</b> dst, src                                                                | Note <sup>a</sup> |     | 7[ ]              | -              | * | * | 0 | - | - |
| dst AND src                                                                       |                   |     |                   |                |   |   |   |   |   |
| <b>XOR</b> dst, src                                                               | Note <sup>a</sup> |     | B[ ]              | -              | * | * | 0 | - | - |
| dst←dst                                                                           |                   |     |                   |                |   |   |   |   |   |
| XOR src                                                                           |                   |     |                   |                |   |   |   |   |   |

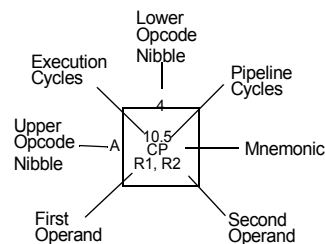
- a. These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

| Address Mode |     | Lower Opcode Nibble |
|--------------|-----|---------------------|
| dst          | src |                     |
| r            | r   | [2]                 |
| r            | Ir  | [3]                 |
| R            | R   | [4]                 |
| R            | IR  | [5]                 |
| R            | IM  | [6]                 |
| IR           | IM  | [7]                 |

## OPCODE MAP

|                    |   | Lower Nibble (Hex)    |                        |                        |                          |                       |                        |                       |                         |                     |                     |                           |                        |                     |                         |                  |              | F |
|--------------------|---|-----------------------|------------------------|------------------------|--------------------------|-----------------------|------------------------|-----------------------|-------------------------|---------------------|---------------------|---------------------------|------------------------|---------------------|-------------------------|------------------|--------------|---|
|                    |   | 0                     | 1                      | 2                      | 3                        | 4                     | 5                      | 6                     | 7                       | 8                   | 9                   | A                         | B                      | C                   | D                       | E                | F            |   |
| Upper Nibble (Hex) | 0 | 6.6<br>DEC<br>R1      | 6.5<br>DEC<br>IR1      | 6.5<br>ADD<br>r1, r2   | 8.5<br>ADD<br>r1, Ir2    | 10.5<br>ADD<br>R2, R1 | 10.5<br>ADD<br>IR2, R1 | 10.5<br>ADD<br>R1, 1M | 10.5<br>ADD<br>R1, 1M   | 6.5<br>LD<br>r1, R2 | 6.5<br>LD<br>r2, R1 | 12/10.5<br>DJNZ<br>r1, RA | 12/0.0<br>JA<br>cc, RA | 6.5<br>LD<br>r1, 1M | 12/10.0<br>JP<br>cc, DA | 6.5<br>INC<br>r1 |              |   |
|                    | 1 | 6.5<br>RLC<br>R1      | 6.5<br>RLC<br>IR1      | 6.5<br>ADC<br>r1, r2   | 6.5<br>ADC<br>r1, Ir2    | 10.5<br>ADC<br>R2, R1 | 10.5<br>ADC<br>IR2, R1 | 10.5<br>ADC<br>R1, 1M | 10.5<br>ADC<br>R1, 1M   |                     |                     |                           |                        |                     |                         |                  |              |   |
|                    | 2 | 6.5<br>INC<br>R1      | 6.6<br>WC<br>IR1       | 6.5<br>SUB<br>r1, r2   | 0.5<br>SUB<br>r1, Ir2    | 10.5<br>SUB<br>R2, R1 | 10.5<br>SUB<br>R2, R1  | 10.5<br>SUB<br>R2, 1M | 10.5<br>BUB<br>IR1, 1M  |                     |                     |                           |                        |                     |                         |                  |              |   |
|                    | 3 | 6.5<br>JP<br>IRR1     | 6.1<br>SRP<br>1M       | 6.5<br>SBC<br>r1, r2   | 6.5<br>SBC<br>r1, Ir2    | 10.5<br>SBC<br>R2, R1 | 10.5<br>SBC<br>IR2, R1 | 10.5<br>SBC<br>R1, 1M | 10.5<br>SBC<br>IR1, 1M  |                     |                     |                           |                        |                     |                         |                  |              |   |
|                    | 4 | 8.5<br>DA<br>R1       | 8.5<br>DA<br>IR1       | 6.5<br>OR<br>r1, r2    | 6.5<br>OR<br>r1, Ir2     | 10.5<br>OR<br>R2, R1  | 10.5<br>OR<br>IR2, R1  | 10.5<br>OR<br>R1, 1M  |                         |                     |                     |                           |                        |                     |                         |                  |              |   |
|                    | 5 | 10.5<br>POP<br>R1     | 10.5<br>POP<br>IR1     | 6.5<br>AND<br>r1, r2   | 6.5<br>AND<br>r1, Ir2    | 10.5<br>AND<br>R2, R1 | 10.5<br>AND<br>IR2, R1 | 10.5<br>AND<br>R1, 1M | 10.5<br>AND<br>IR1, 1M  |                     |                     |                           |                        |                     |                         |                  |              |   |
|                    | 6 | 6.5<br>COM<br>R1      | 6.5<br>COM<br>IR1      | 6.5<br>TCM<br>r1, r2   | 6.5<br>TCM<br>r1, Ir2    | 10.5<br>TCM<br>R2, R1 | 10.5<br>TCM<br>IR2, R1 | 10.5<br>TCM<br>R1, 1M | 10.5<br>TCM<br>IR1, 1M  |                     |                     |                           |                        |                     |                         |                  | 6.0<br>STOP  |   |
|                    | 7 | 10/12.1<br>PUSH<br>R2 | 10/12.1<br>PUSH<br>IR2 | 6.5<br>TM<br>r1, r2    | 6.5<br>TM<br>r1, Ir2     | 10.5<br>TM<br>R2, R1  | 10.5<br>TM<br>IR2, R1  | 10.5<br>TM<br>R1, 1M  | 10.5<br>TM<br>IR1, 1M   |                     |                     |                           |                        |                     |                         |                  | 7.0<br>HALT  |   |
|                    | 8 | 10.5<br>DECW<br>RR1   | 10.5<br>DECW<br>IR1    | 12.0<br>LDE<br>r1, Ir2 | 18.0<br>LDEI<br>r1, Ir2  |                       |                        |                       |                         |                     |                     |                           |                        |                     |                         |                  | 6.1<br>DI    |   |
|                    | 9 | 6.5<br>RL<br>R1       | 6.5<br>RL<br>IR1       | 12.0<br>LDE<br>r1, Ir2 | 18.0<br>LDEI<br>r1, Ir2  |                       |                        |                       |                         |                     |                     |                           |                        |                     |                         |                  | 6.1<br>EI    |   |
|                    | A | 10.5<br>INCW<br>RR1   | 10.5<br>INCW<br>IR1    | 6.5<br>CP<br>r1, r2    | 6.5<br>CP<br>r1, Ir2     | 10.5<br>CP<br>R2, R1  | 10.5<br>CP<br>IR2, R1  | 10.5<br>CP<br>R1, 1M  | 10.5<br>CP<br>IR1, 1M   |                     |                     |                           |                        |                     |                         |                  | 14.0<br>RET  |   |
|                    | B | 6.5<br>CLR<br>R1      | 6.5<br>CLR<br>IR1      | 6.5<br>XOR<br>r1, r2   | 6.5<br>XOR<br>r1, Ir2    | 10.5<br>XOR<br>R2, R1 | 10.5<br>XOR<br>IR2, R1 | 10.5<br>XOR<br>R1, 1M | 10.5<br>XOR<br>IR1, 1M  |                     |                     |                           |                        |                     |                         |                  | 16.0<br>IRET |   |
|                    | C | 6.5<br>RRC<br>R1      | 6.5<br>RRC<br>IR1      | 12.0<br>LDC<br>r1, Ir2 | 18.0<br>LDC<br>Ir1, Ir2  |                       |                        |                       | 10.5<br>LD<br>r1, x, R2 |                     |                     |                           |                        |                     |                         |                  | 6.5<br>RCF   |   |
|                    | D | 6.5<br>SRA<br>R1      | 6.5<br>SRA<br>IR1      | 12.0<br>LDC<br>r1, Ir2 | 18.0<br>LDCI<br>Ir1, Ir2 | 20.0<br>CALL*<br>IRR1 |                        | 20.0<br>CALL<br>DA    | 10.5<br>LD<br>r2, x, R1 |                     |                     |                           |                        |                     |                         |                  | 6.5<br>SCF   |   |
|                    | E | 6.5<br>RR<br>R1       | 6.5<br>RR<br>IR1       |                        | 6.5<br>LD<br>r1, IR2     | 10.5<br>LD<br>R2, R1  | 10.5<br>LD<br>IR2, R1  | 10.5<br>LD<br>R1, 1M  | 10.5<br>LD<br>IR1, 1M   |                     |                     |                           |                        |                     |                         |                  | 6.5<br>CCF   |   |
|                    | F | 8.5<br>SWAP<br>R1     | 8.5<br>SWAP<br>IR1     |                        | 6.5<br>LD<br>Ir1, r2     |                       | 10.5<br>LD<br>R2, IR1  |                       |                         |                     |                     |                           |                        |                     |                         |                  | 6.0<br>NOP   |   |
|                    |   | 2                     |                        |                        |                          | 3                     |                        |                       |                         | 2                   |                     |                           |                        | 3                   |                         |                  |              | 1 |
|                    |   | Bytes per Instruction |                        |                        |                          |                       |                        |                       |                         |                     |                     |                           |                        |                     |                         |                  |              |   |



### Legend:

R = 8-bit Address  
r = 4-bit Address  
R1 or r1 = Dst Address  
R2 or r2 = Src Address

### Sequence:

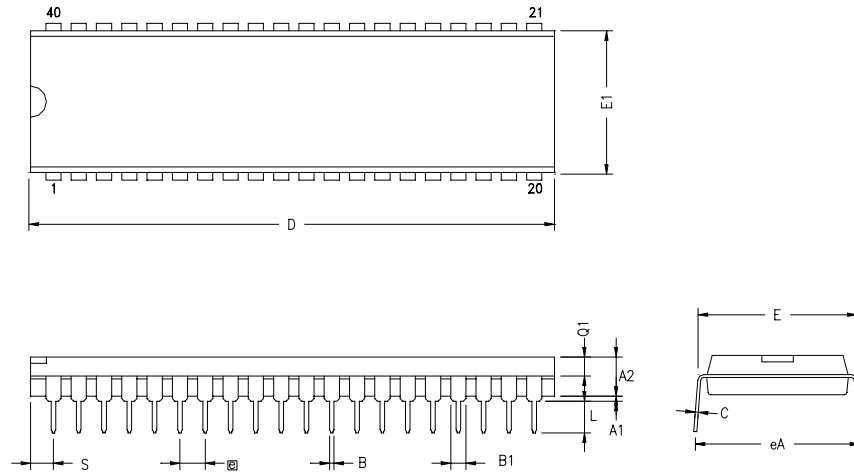
Opcode, First Operand,  
Second Operand

**Note:** Blank areas not defined

\*2-byte instruction appears as  
a 3-byte instruction

Figure 47. Opcode Map

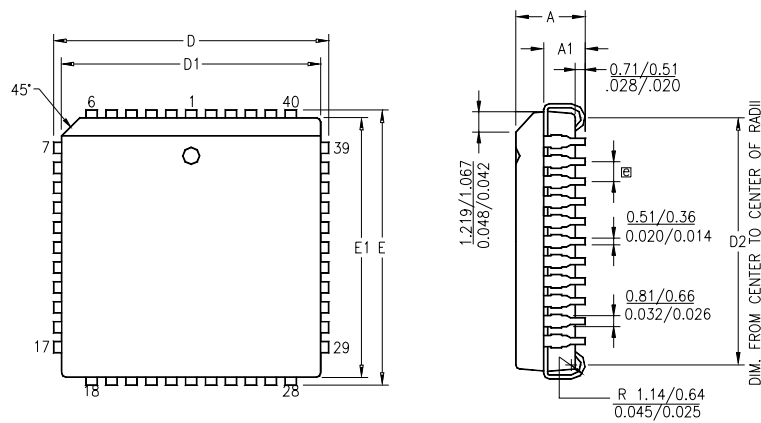
## PACKAGE INFORMATION



| SYMBOL | MILLIMETER |       | INCH     |       |
|--------|------------|-------|----------|-------|
|        | MIN        | MAX   | MIN      | MAX   |
| A1     | 0.51       | 1.02  | .020     | .040  |
| A2     | 3.18       | 3.94  | .125     | .155  |
| B      | 0.38       | 0.53  | .015     | .021  |
| B1     | 1.02       | 1.52  | .040     | .060  |
| C      | 0.23       | 0.38  | .009     | .015  |
| D      | 52.07      | 52.58 | 2.050    | 2.070 |
| E      | 15.24      | 15.75 | .600     | .620  |
| E1     | 13.59      | 14.22 | .535     | .560  |
| □      | 2.54 TYP   |       | .100 TYP |       |
| eA     | 15.49      | 16.76 | .610     | .660  |
| L      | 3.05       | 3.81  | .120     | .150  |
| Q1     | 1.40       | 1.91  | .055     | .075  |
| S      | 1.52       | 2.29  | .060     | .090  |

CONTROLLING DIMENSIONS : INCH

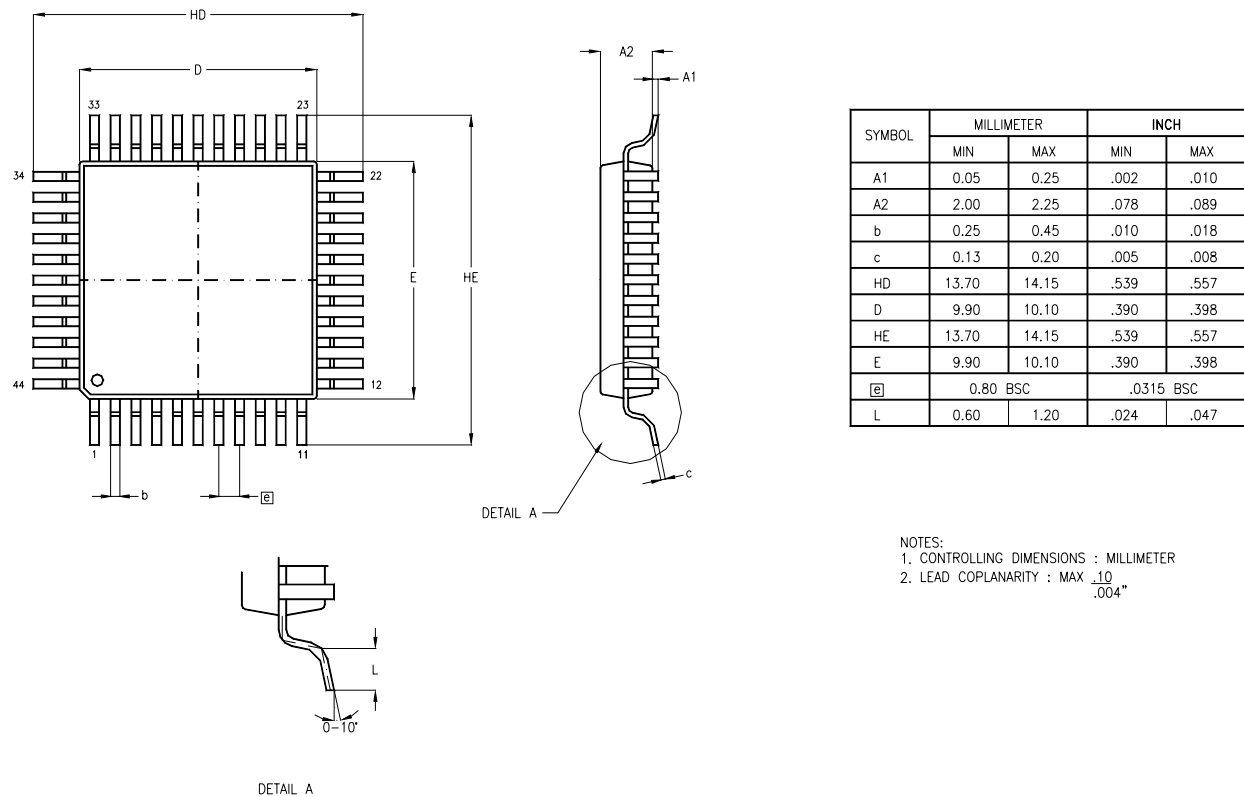
Figure 48. 40-Pin DIP Package Diagram



| SYMBOL | MILLIMETER |       | INCH      |       |
|--------|------------|-------|-----------|-------|
|        | MIN        | MAX   | MIN       | MAX   |
| A      | 4.27       | 4.57  | 0.168     | 0.180 |
| A1     | 2.41       | 2.92  | 0.095     | 0.115 |
| D/E    | 17.40      | 17.65 | 0.685     | 0.695 |
| D1/E1  | 16.51      | 16.66 | 0.650     | 0.656 |
| D2     | 15.24      | 16.00 | 0.600     | 0.630 |
| □      | 1.27 BSC   |       | 0.050 BSC |       |

- NOTES:  
1. CONTROLLING DIMENSION : INCH  
2. LEADS ARE COPLANAR WITHIN 0.004".  
3. DIMENSION :  $\frac{MM}{INCH}$

Figure 49. 44-Pin PLCC Package Diagram



**Figure 50. 44-Pin LQFP Package Diagram**

## ORDERING INFORMATION

| <b>Z86E61</b>     |                    |                   |                    |
|-------------------|--------------------|-------------------|--------------------|
| <b>16 MHz</b>     |                    | <b>20 MHz</b>     |                    |
| <b>40-Pin DIP</b> | <b>44-Pin PLCC</b> | <b>40-Pin DIP</b> | <b>44-Pin PLCC</b> |
| Z86E6116PSC       | Z86E6116VSC        | Z86E6120PSC       | Z86E6120VSC        |
| <b>Z86E63</b>     |                    |                   |                    |
| <b>16 MHz</b>     |                    | <b>20 MHz</b>     |                    |
| <b>40-Pin DIP</b> | <b>44-Pin PLCC</b> | <b>40-Pin DIP</b> | <b>44-Pin PLCC</b> |
| Z86E6316PSC       | Z86E6316VSC        | Z86E6320PSC       | Z86E6320VSC        |

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.



## CODES

- Preferred Package  
P = Plastic DIP  
V = Plastic Chip Carrier
- Temperature  
S = 0°C to +70°C
- Speeds  
12 = 16 MHz  
16 = 20 MHz
- Environmental  
C = Plastic Standard

### Example:

