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Jameco Part Number 1736773

Dual/Quad Micropower, 1MHz C-Load Picoampere Bias Current JFET Input Op Amps

FEATURES

- **Input Bias Current:**
2pA Max (LT1464A)
20pA Max (LT1464, LT1465)
- **Supply Current per Amplifier: 200µA Max**
- **Gain Bandwidth Product: 1MHz Typ**
- **Slew Rate: 0.9V/µs Typ**
- **Input Common Mode Range Includes Positive Rail**
- **Unity-Gain Stable for C-Load™ Up to 10nF**
- **Open-Loop Gain: 1 Million Typ**
- **Guaranteed Specs with ±5V, ±15V Supplies**
- **Guaranteed Matching Specifications**
- **Standard Pinout: SO-8, SO-14 Package**

APPLICATIONS

- Battery-Powered Systems
- Photocurrent Amplifiers
- Low Frequency, Micropower Active Filters
- Low Droop Track-and-Hold Circuits

DESCRIPTION

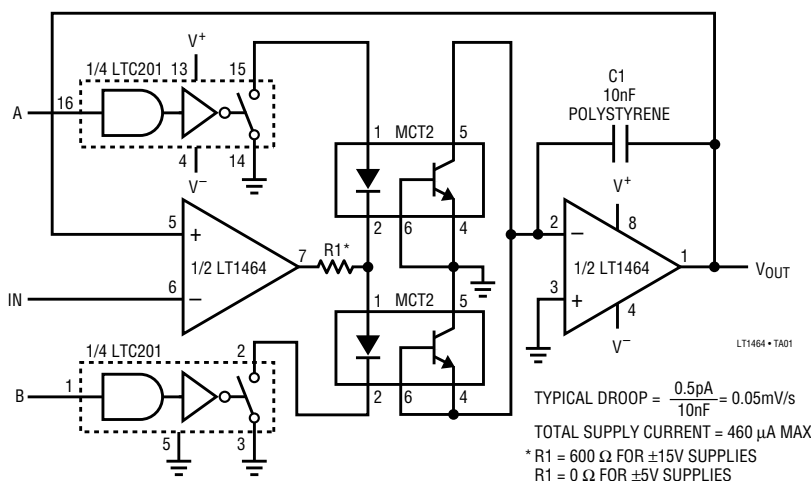
The LT®1464 (dual) and LT1465 (quad) are the first micropower op amps (200µA max per amp) to offer picoampere input bias currents (500fA typ) and unity-gain stability for capacitive loads up to 10nF. The output can swing a 10k load to within 1.5V of either supply, just like op amps that require an order of magnitude more supply current. This unique combination of performance makes the LT1464/LT1465 ideal over a wide range of input and output impedances.

In the design and testing of the LT1464/LT1465, particular emphasis has been placed on optimizing performance in the low cost SO-8 (dual) and 14-lead SO (quad) package for ±15V and ±5V supplies. The input common mode range includes the positive rail. Slew rate (0.5V/µs min) and gain bandwidth product (650kHz min) are 100% tested. A full set of matching specifications is also provided.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
 C-Load is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

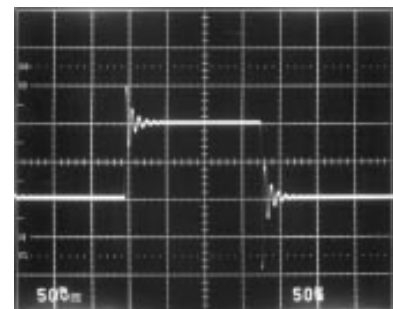
Micropower Low Droop Track-and-Hold/Peak Detector



FUNCTION	MODE	IN A	IN B	MODE	IN A	IN B
Track-and-Hold	Track	0	0	Hold	1	1
Positive Peak Detector	Reset	0	0	Store	0	1
Negative Peak Detector	Reset	0	0	Store	1	0

LTC201 switch is open for logic "1".

Small-Signal Response, C_{LOAD} = 10nF



A_V = 1
 V_S = ±5V, ±15V
 C_L = 10nF

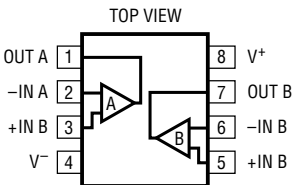
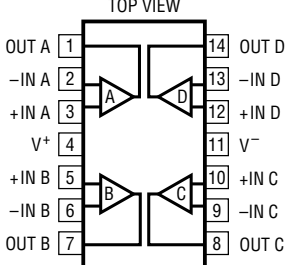
1464 • TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 20\text{V}$
 Differential Input Voltage $\pm 40\text{V}$
 Input Current 20mA
 Output Short-Circuit Duration Indefinite
 Operating Temperature Range -40°C to 85°C

Specified Temperature Range -40°C to 85°C
 Maximum Junction Temperature 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

 N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$ (N) $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$ (S)	ORDER PART NUMBER	 N PACKAGE 14-LEAD PDIP S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 110^{\circ}\text{C/W}$ (N) $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$ (S)	ORDER PART NUMBER
	LT1464ACN8 LT1464ACS8 LT1464CN8 LT1464CS8		LT1465CN LT1465CS
	S8 PART MARKING		
	1464A 1464		

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1464AC			LT1464C/LT1465C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5\text{V}$ $V_S = \pm 15\text{V}$		0.4 0.6	0.8 2.0		0.4 0.6	0.8 2.0	mV mV
I_{OS}	Input Offset Current	$V_S = \pm 5\text{V}$ $V_S = \pm 15\text{V}$		0.2 0.5	1.2 2.0		0.5	15	pA pA
I_B	Input Bias Current	$V_S = \pm 5\text{V}$ $V_S = \pm 15\text{V}$		± 0.4 ± 0.5	± 2.0 ± 3.0		± 0.5	± 20	pA pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2			2		μV_{P-P}
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ $f_0 = 1000\text{Hz}$		33 24			33 24		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
	Input Noise Current Density	$f_0 = 10\text{Hz}$, 1kHz (Note 3)		0.4			0.4		$\text{fA}/\sqrt{\text{Hz}}$
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12.5\text{V}$ to 15V	76	85		74	85		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 20\text{V}$	81	90		78	90		dB
R_{IN}	Input Resistance—Differential Common Mode Common Mode	$V_{CM} = -12.5\text{V}$ to 8V $V_{CM} = 8\text{V}$ to 15V		10^{12} 10^{12} 0^{11}			10^{12} 10^{12} 10^{11}		Ω Ω Ω
C_{IN}	Input Capacitance			3			3		pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10\text{V}$, $R_L = 10\text{k}$	350	1000		300	900		V/mV
		$V_O = \pm 10\text{V}$, $R_L = 2\text{k}$	150	450		150	450		V/mV
		$V_S = \pm 5\text{V}$, $V_O = \pm 2\text{V}$, $R_L = 10\text{k}$	100	250		100	250		V/mV
		$V_S = \pm 5\text{V}$, $V_O = \pm 1\text{V}$, $R_L = 2\text{k}$	50	170		50	170		V/mV

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1464AC			LT1464C/LT1465C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output Voltage Swing	$R_L = 10k$	± 13.5	± 13.7		± 13.5	± 13.7		V
		$R_L = 2k$	± 13.3	± 13.5		± 13.3	± 13.5		V
		$V_S = \pm 5V$, $R_L = 2k$	± 3.5	± 3.7		± 3.5	± 3.7		V
SR	Slew Rate	$R_L = 10k$ (Note 4)	0.5	0.9		0.5	0.9		V/ μs
GBW	Gain Bandwidth Product	$f = 10kHz$	650	1000		650	1000		kHz
I_S	Supply Current per Amplifier	$V_S = \pm 5V$		145	200		145	200	μA
				135	200		135	200	μA
	Channel Separation	$f = 10Hz$, $V_O = \pm 10V$, $R_L = 10k$		132			132		dB
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$		0.5	1.3		0.5	1.3	mV
		$V_S = \pm 15V$		0.8	3.3		0.8	3.3	mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)	$V_S = \pm 5V$		0.4	3.0				pA
		$V_S = \pm 15V$		0.5	4.0		0.5	30	pA
$\Delta CMRR$	Common Mode Rejection Match	(Notes 5, 7)	74	85		71	85		dB
$\Delta PSRR$	Power Supply Rejection Match	(Notes 5, 7)	78	88		74	88		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1464AC			LT1464C/LT1465C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$	●		0.5	1.4		0.5	1.4	mV
		$V_S = \pm 15V$	●		0.9	2.8		0.9	2.8	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		7	20		7	20	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●		10	50		25	450	pA
I_B	Input Bias Current		●		60	150		150	750	pA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12V$ to $15V$	●	75	85		73	85		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 20V$	●	80	89		77	89		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10k$	●	200	600		200	600		V/mV
		$V_O = \pm 10V$, $R_L = 2k$	●	100	350		100	350		V/mV
		$V_S = \pm 5V$, $V_O = \pm 2V$, $R_L = 10k$	●	80	200		80	200		V/mV
		$V_S = \pm 5V$, $V_O = \pm 1V$, $R_L = 2k$	●	45	150		45	150		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	± 13.4	± 13.6		± 13.4	± 13.6		V
		$R_L = 2k$	●	± 13.2	± 13.4		± 13.2	± 13.4		V
		$V_S = \pm 5V$, $R_L = 2k$	●	± 3.4	± 3.6		± 3.4	± 3.6		V
SR	Slew Rate	$R_L = 10k$ (Note 4)	●	0.4	0.8		0.4	0.8		V/ μs
GBW	Gain Bandwidth Product	$f = 10kHz$	●	540	870		540	870		kHz
I_S	Supply Current per Amplifier	$V_S = \pm 5V$	●		160	220		160	220	μA
			●		150	220		150	220	μA
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$	●		0.7	2.0		0.7	2.0	mV
		$V_S = \pm 15V$	●		0.9	3.5		0.9	3.5	mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)		●		5	40		35	500	pA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1464AC			LT1464C/LT1465C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$\Delta CMRR$	Common Mode Rejection Match	(Notes 5, 7)	●	73	84		70	84		dB
$\Delta PSRR$	Power Supply Rejection Match	(Notes 5, 7)	●	77	85		73	85		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40^\circ C \leq T_A \leq 85^\circ C$ (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1464AC			LT1464C/LT1465C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$	●		0.6	1.5		0.6	1.5	mV
		$V_S = \pm 15V$	●		1.0	3.0		1.0	3.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		7	20		7	20	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●		40	150		60	700	pA
I_B	Input Bias Current		●		200	500		300	2500	pA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12V$ to $15V$	●	74	84		72	84		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 20V$	●	79	88		76	88		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10k$	●	175	400		175	400		V/mV
		$V_O = \pm 10V$, $R_L = 2k$	●	80	250		80	250		V/mV
		$V_S = \pm 5V$, $V_O = \pm 2V$, $R_L = 10k$	●	70	180		70	180		V/mV
		$V_S = \pm 5V$, $V_O = \pm 1V$, $R_L = 2k$	●	45	140		45	140		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	± 13.2	± 13.4		± 13.2	± 13.4		V
		$R_L = 2k$	●	± 13.0	± 13.2		± 13.0	± 13.2		V
		$V_S = \pm 5V$, $R_L = 2k$	●	± 3.2	± 3.4		± 3.2	± 3.4		V
SR	Slew Rate	$R_L = 10k$ (Note 4)	●	0.35	0.7		0.35	0.7		V/ μs
GBW	Gain Bandwidth Product	$f = 10kHz$	●	510	850		510	850		kHz
I_S	Supply Current per Amplifier		●		165	230		165	230	μA
		$V_S = \pm 5V$	●		160	230		160	230	μA
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$	●		0.8	2.5		0.8	2.5	mV
		$V_S = \pm 15V$	●		1.0	4.0		1.0	4.0	mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)		●		20	100		70	800	pA
$\Delta CMRR$	Common Mode Rejection Match	(Notes 5, 7)	●	72	83		69	83		dB
$\Delta PSRR$	Power Supply Rejection Match	(Notes 5, 7)	●	76	81		73	81		dB

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1465s (or 100 LT1464s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: The LT1464 and LT1465 are designed, characterized and expected to meet these extended temperature limits, but are not tested at $-40^\circ C$ and $85^\circ C$. Guaranteed I grade parts are available, consult factory.

Note 3: Current noise is calculated from the formula: $i_n = (2qI_b)^{1/2}$ where $q = (1.6)(10)^{-19}$ coulomb. The noise of source resistors up to $1G\Omega$ swamps the contribution of current noise.

Note 4: Slew rate is measured in $A_V = -1$; input signal is $\pm 7.5V$, output is measured at $\pm 2.5V$.

Note 5: $\Delta CMRR$ and $\Delta PSRR$ are defined as follows:

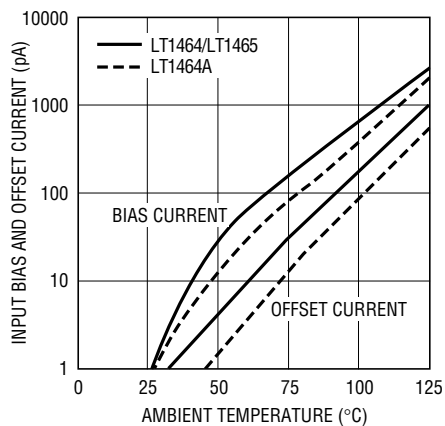
1. CMRR and PSRR are measured in $\mu V/V$ on the individual amplifiers.
2. The difference is calculated between the matching sides in $\mu V/V$.
3. The result is converted to dB.

Note 6: This parameter is not 100% tested.

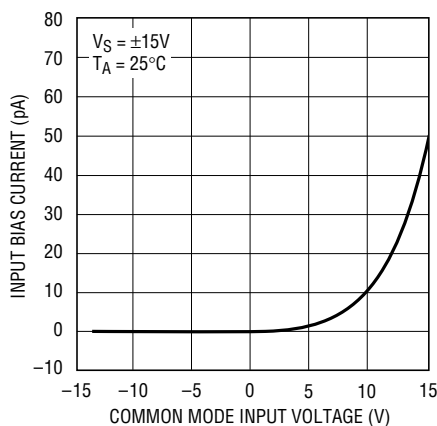
Note 7: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1465; between the two amplifiers on the LT1464.

TYPICAL PERFORMANCE CHARACTERISTICS

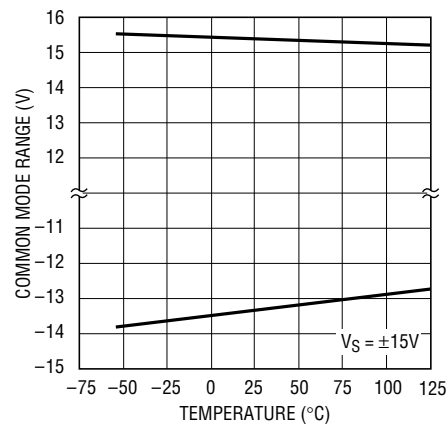
Input Bias and Offset Current vs Temperature



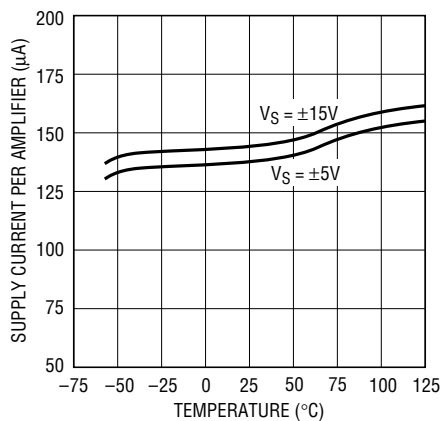
Input Bias Current Over the Common Mode Range



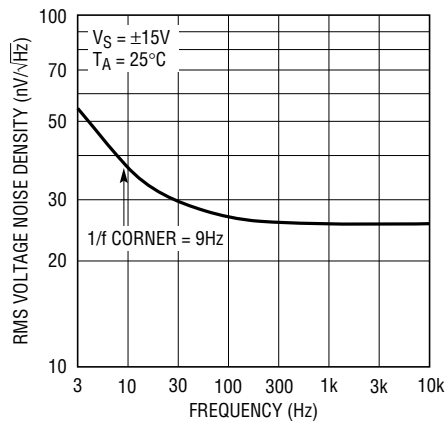
Common Mode Range vs Temperature



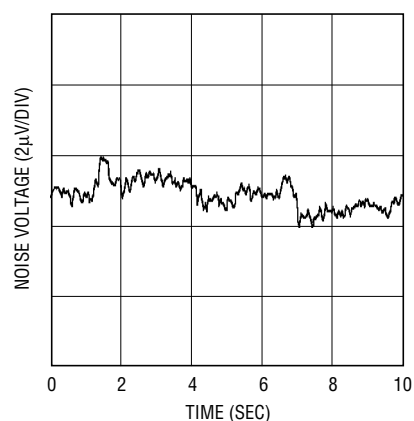
Supply Current vs Temperature



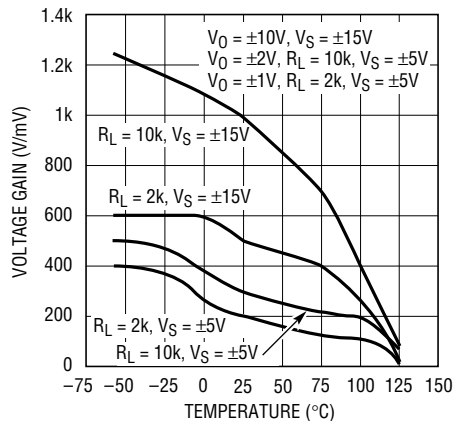
Voltage Noise vs Frequency



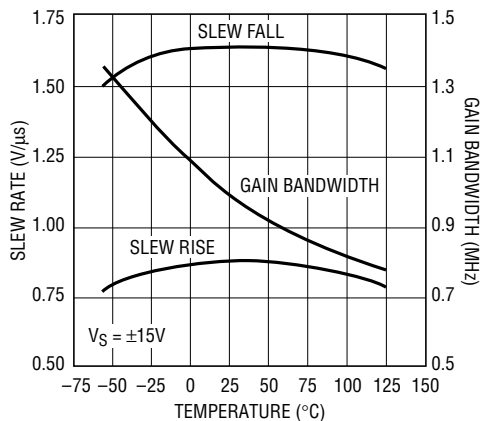
0.1Hz to 10Hz Noise



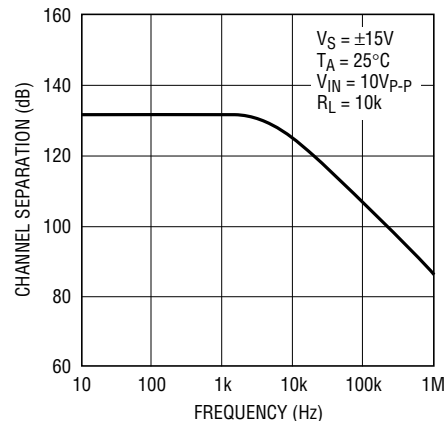
Voltage Gain vs Temperature



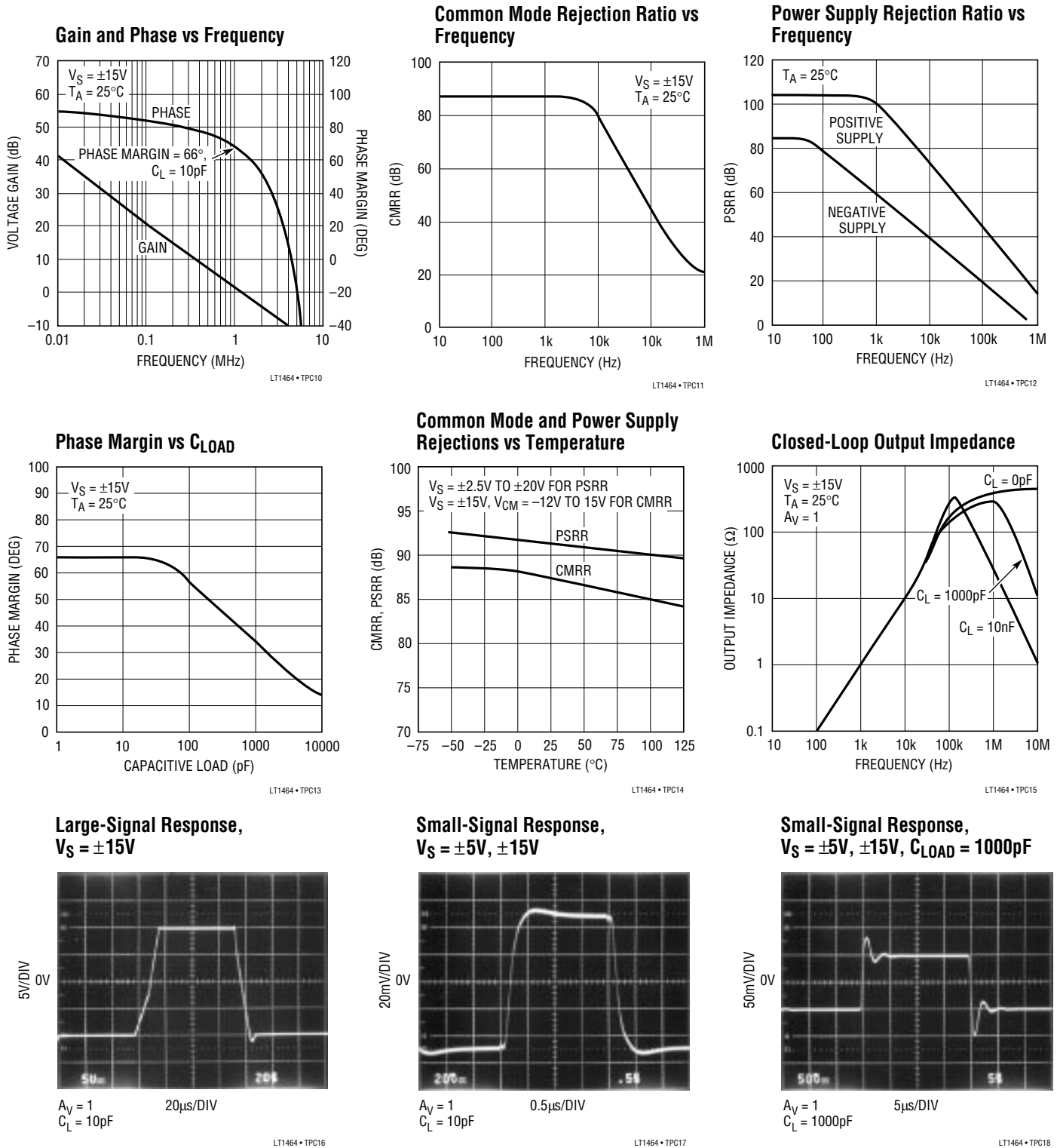
Slew Rate, Gain Bandwidth Product vs Temperature



Channel Separation vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS



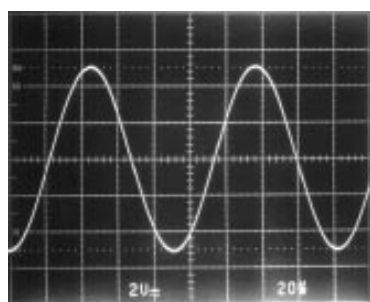
APPLICATIONS INFORMATION

Phase Reversal Protection

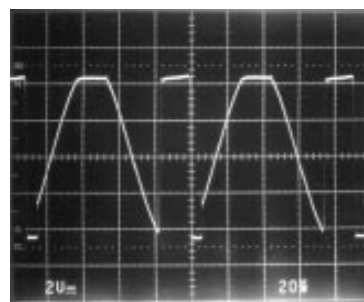
Most industry standard JFET input single, dual and quad op amps exhibit phase reversal at the output when the negative common mode limit at the input is exceeded. Common mode range is at a premium at $\pm 5V$ supplies. The Figures show a $\pm 5.2V$ sine wave input (Figure 1a), the response of a competing JFET input op amp in the unity-

gain follower mode (Figure 1b) and the response of the LT1464/LT1465 (Figure 1c).

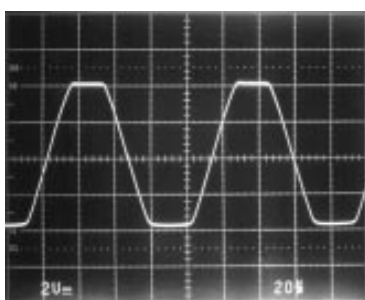
The phase reversal of Figure 1b can cause lock-up in servo systems. The LT1464/LT1465 does not phase-reverse when the common mode input is anywhere within the supplies.



(1a) $\pm 5.2V$ Sine Wave



(1b) Typical JFET Input Op Amp
with $\pm 5V$ Supplies



(1c) LT1464/LT1465 Output
with $\pm 5V$ Supplies

Figure 1. Voltage Follower with Input Exceeding the Common Mode Range ($V_S = \pm 5V$)

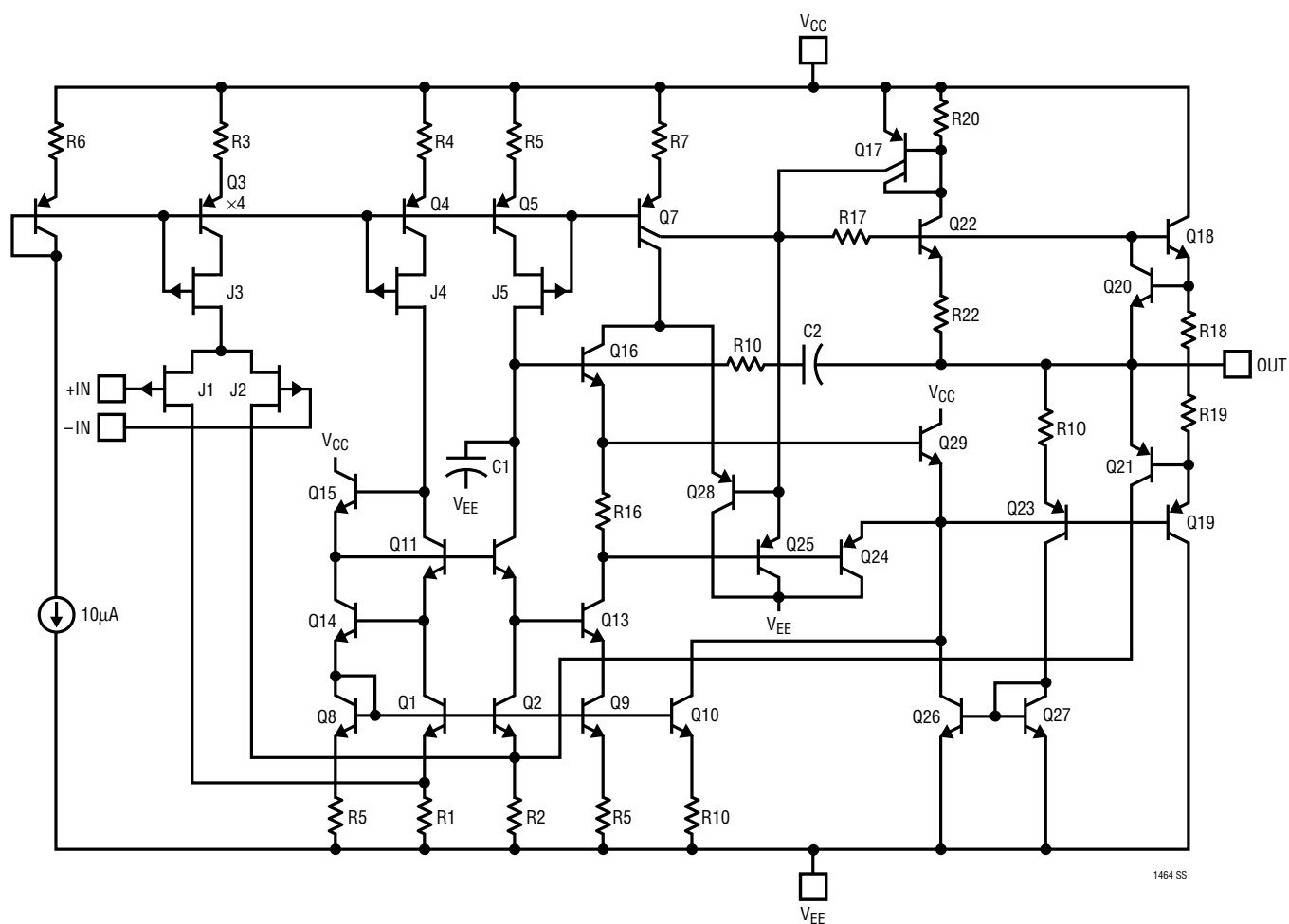
[illegible]

The circuit diagram shows a two-stage op-amp buffer using two 1/4 LT1465 op-amp sections. The first stage has a non-inverting input (pin 3) connected to ground (-15V), an inverting input (pin 2) connected to the input V_{IN} through resistor R1 (237k) and to the output (pin 1) through resistor R2 (237k), and a feedback capacitor C1 (33nF) between pins 2 and 1. The output of the first stage (pin 1) is connected to the non-inverting input (pin 12) of the second stage through resistor R4 (154k). The second stage has its inverting input (pin 13) connected to ground through resistor R6 (249k) and to the output (pin 14) through resistor R5 (154k) and capacitor C3 (10nF). The output of the second stage is V_{OUT} . The op-amp is powered by a 15V supply (pin 4) and a -15V supply (pin 11). A 100nF capacitor C2 is connected to the input node between R1 and R2. A 330nF capacitor C4 is connected to the output of the first stage (pin 1).

The frequency response plot shows the magnitude of the voltage gain $|V_{OUT}/V_{IN}|$ in dB versus frequency in Hz on a log-log scale. The gain is approximately 0 dB at low frequencies and decreases at a rate of -20 dB/decade starting around 100 Hz, reaching approximately -40 dB at 10 kHz. The plot is labeled "TYPICAL GAIN - 20 dB/DEC" and "LT1464 • TA05".

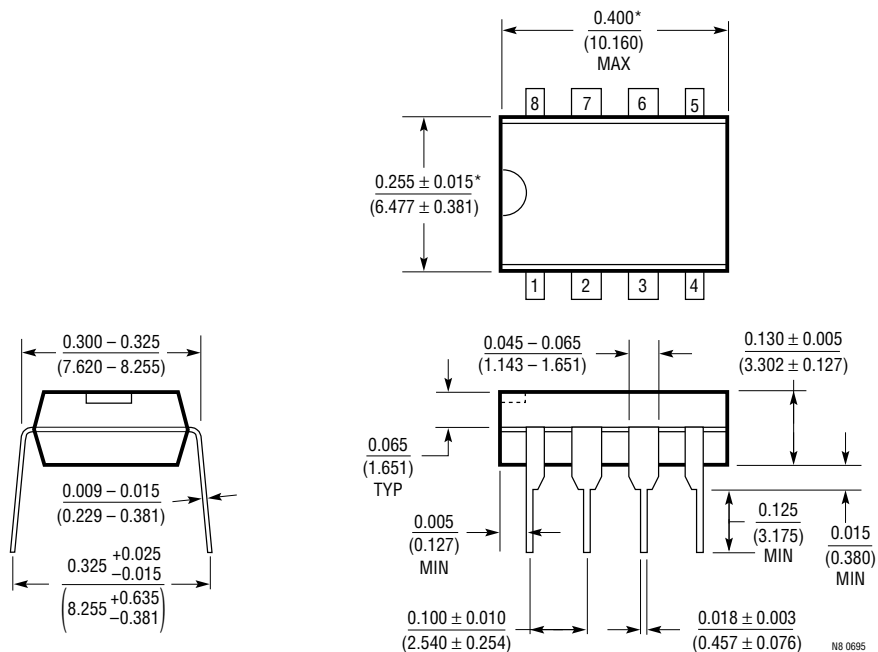
8

SIMPLIFIED SCHEMATIC



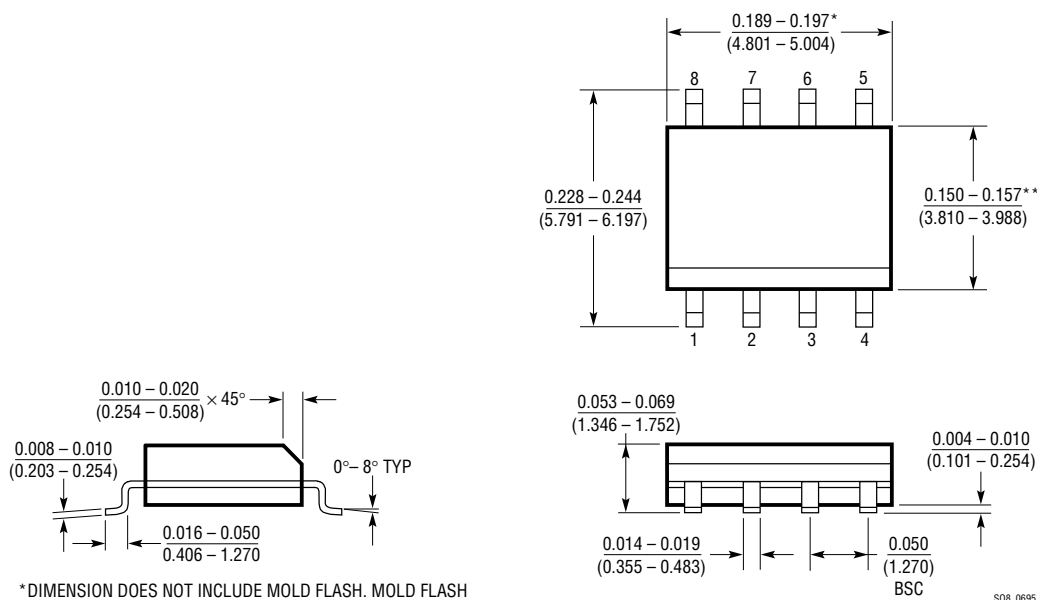
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)

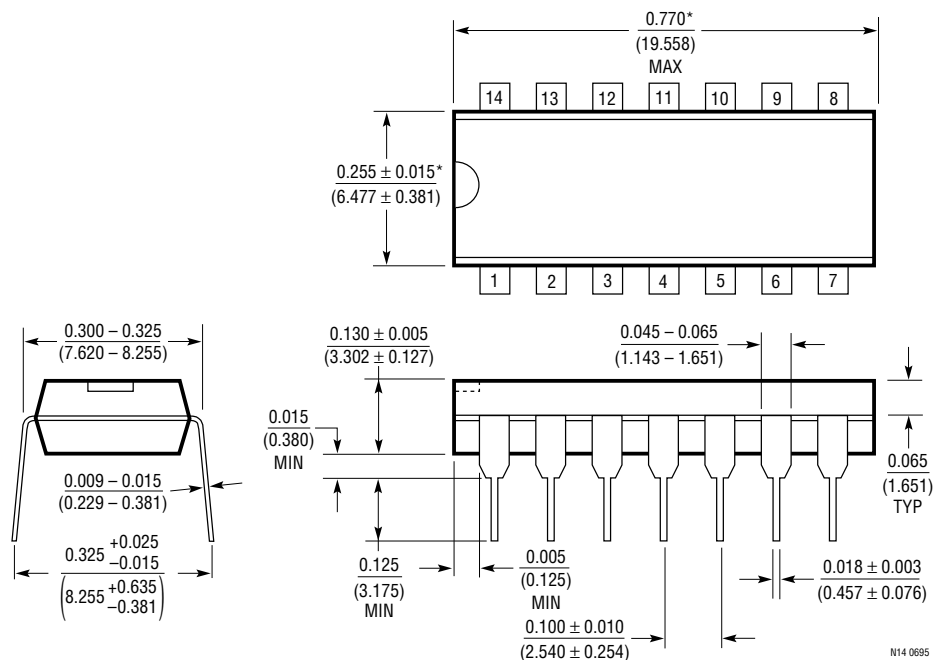


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

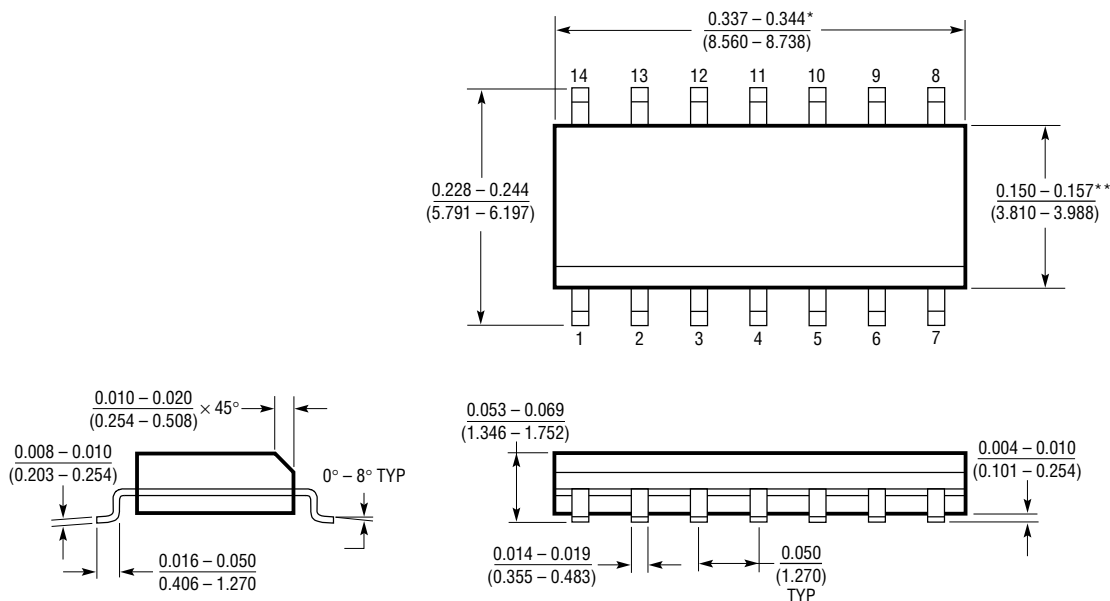
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N Package 14-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)

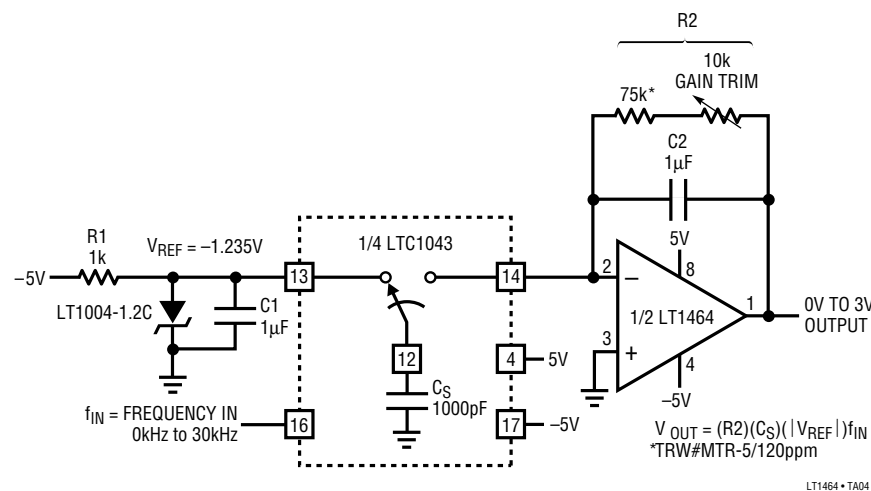


S Package 14-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



TYPICAL APPLICATION

Low Voltage 0.027% Frequency to Voltage Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1057	Dual JFET Input Precision, High Speed Op Amp	Fast Settling Time, 14V/μs Slew Rate, 5Mhz GBW, 450μV V _{OS} (Max), 50pA I _{OS} (Max)
LT1113	Dual Low Noise, Precision, JFET Input Op Amp	6nV/√Hz Input Noise Voltage Density, 480pA I _B , 6.3MHz GBW
LT1169	Dual Low Noise, Picoampere Bias Current, JFET Input Op Amp	20pA I _B , 8nV/√Hz e _n , 5.3MHz GBW, 1.5pF Input Capacitance
LT1457	Dual Precision JFET Input Op Amp C-Load	Drives 10,000pF Capacitive Load, 450μV V _{OS} (Max), 4μV/°C Drift
LT1462/LT1463	Dual/Quad Micropower, C-Load Picoampere Bias Current JFET Input Op Amps	28μA Supply Current Per Amplifiers Drives 10μF Capacitive Load, 175kHz GBW