



FDMS7620S

Dual N-Channel PowerTrench® MOSFET

Q1: 30 V, 13 A, 20.0 mΩ Q2: 30 V, 22 A, 11.2 mΩ

May 2014

Features

Q1: N-Channel

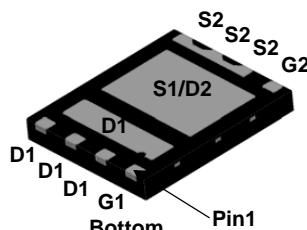
- Max $r_{DS(on)}$ = 20.0 mΩ at $V_{GS} = 10$ V, $I_D = 10.1$ A
- Max $r_{DS(on)}$ = 30.0 mΩ at $V_{GS} = 4.5$ V, $I_D = 7.5$ A

Q2: N-Channel

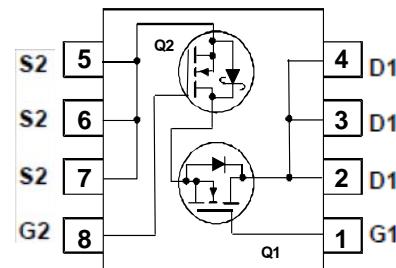
- Max $r_{DS(on)}$ = 11.2 mΩ at $V_{GS} = 10$ V, $I_D = 12.4$ A
- Max $r_{DS(on)}$ = 14.2 mΩ at $V_{GS} = 4.5$ V, $I_D = 10.9$ A
- Pinout optimized for simple PCB design
- Thermally efficient dual Power 56 Package
- RoHS Compliant



Top



Power 56



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	± 20	V
I_D	Drain Current -Continuous	$T_C = 25^\circ\text{C}$	13	A
	-Continuous	$T_A = 25^\circ\text{C}$	10.1	
	-Pulsed		27	
E_{AS}	Single Pulse Avalanche Energy	(Note 4)	9	mJ
P_D	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$	2.2 ^{1a}	W
	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$	1.0 ^{1c}	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57 ^{1a}	50 ^{1b}	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 ^{1c}	120 ^{1d}	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7620S	FDMS7620S	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}, \text{referenced to } 25^\circ\text{C}$ $I_D = 10 \text{ mA}, \text{referenced to } 25^\circ\text{C}$	Q1 Q2		19 19		$\text{mV/}^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2			1 500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2			100 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ $V_{GS} = V_{DS}, I_D = 1 \text{ mA}$	Q1 Q2	1.0 1.0	2.2 2.0	3.0 3.0	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}, \text{referenced to } 25^\circ\text{C}$ $I_D = 10 \text{ mA}, \text{referenced to } 25^\circ\text{C}$	Q1 Q2		-6 -5		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 10.1 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 7.5 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}, T_J = 125^\circ\text{C}$	Q1		15.2 22.7 18.7	20.0 30.0 22.5	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}, I_D = 12.4 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 10.9 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 12.4 \text{ A}, T_J = 125^\circ\text{C}$	Q2		8.3 10.5 8.9	11.2 14.2 15.1	
g_{FS}	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 10.1 \text{ A}$ $V_{DD} = 5 \text{ V}, I_D = 12.4 \text{ A}$	Q1 Q2		22 53		s

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$	Q1 Q2		457 1050	608 1400	pF
C_{oss}	Output Capacitance		Q1 Q2		167 358	222 477	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		22 35	31 49	pF
R_g	Gate Resistance		Q1 Q2	0.2 0.2	1.6 1.2	4.4 3.5	Ω

Switching Characteristics

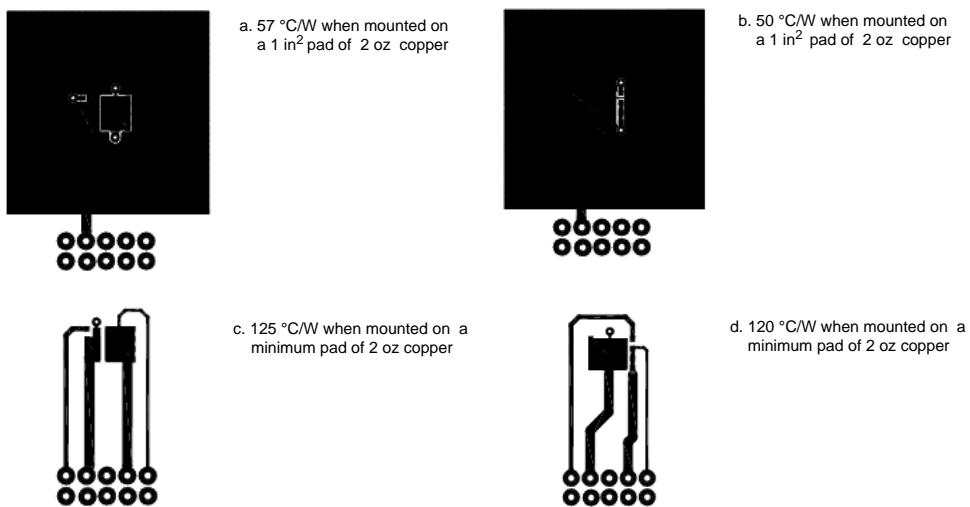
$t_{d(\text{on})}$	Turn-On Delay Time	$Q1$ $V_{DD} = 15 \text{ V}, I_D = 10.1 \text{ A}, R_{\text{GEN}} = 6 \Omega$	Q1 Q2		5.2 6.6	10 14	ns
t_r	Rise Time		Q1 Q2		1.2 1.8	10 10	ns
$t_{d(\text{off})}$	Turn-Off Delay Time	$Q2$ $V_{DD} = 15 \text{ V}, I_D = 12.4 \text{ A}, R_{\text{GEN}} = 6 \Omega$	Q1 Q2		11.9 17.4	22 32	ns
t_f	Fall Time		Q1 Q2		1.4 1.5	10 10	ns
$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0\text{V} \text{ to } 10 \text{ V}$	Q1		7.2 15.6	11 23	nC
$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0\text{V} \text{ to } 5 \text{ V}$	Q1 Q2		3.8 7.9	6 12	nC
Q_{gs}	Gate to Source Charge	$Q2$ $V_{DD} = 15 \text{ V}, I_D = 12.4 \text{ A}$	Q1 Q2		1.6 3.2		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		1.1 1.6		nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 10.1 \text{ A}$ (Note 2) $V_{GS} = 0 \text{ V}$, $I_S = 12.4 \text{ A}$ (Note 2)	Q1 Q2		0.90 0.83	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 10.1 \text{ A}$, $di/dt = 100 \text{ A/s}$ Q2	Q1 Q2		16 18	28 32	ns
Q_{rr}	Reverse Recovery Charge	$I_F = 12.4 \text{ A}$, $di/dt = 300 \text{ A/s}$	Q1 Q2		4 13	10 23	nC

Notes:

1. R_{thJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{thJC} is guaranteed by design while R_{thCA} is determined by the user's board design.



2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

4. Q1: E_{AS} of 9 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3 \text{ mH}$, $I_{AS} = 8 \text{ A}$, $V_{DD} = 27 \text{ V}$, $V_{GS} = 10 \text{ V}$. 100% test at $L = 0.1 \text{ mH}$, $I_{AS} = 12 \text{ A}$.

Q2: E_{AS} of 21 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3 \text{ mH}$, $I_{AS} = 12 \text{ A}$, $V_{DD} = 27 \text{ V}$, $V_{GS} = 10 \text{ V}$. 100% test at $L = 0.1 \text{ mH}$, $I_{AS} = 18 \text{ A}$.

Typical Characteristics (Q1 N-Channel)

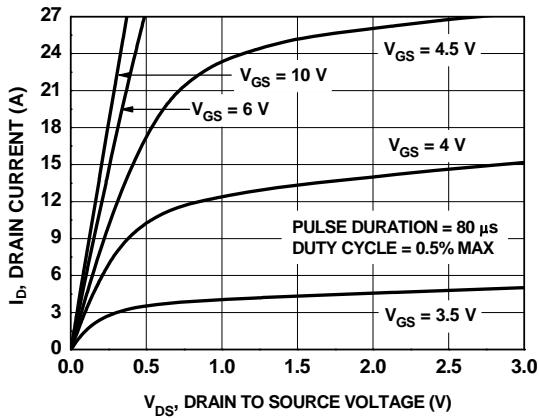


Figure 1. On Region Characteristics

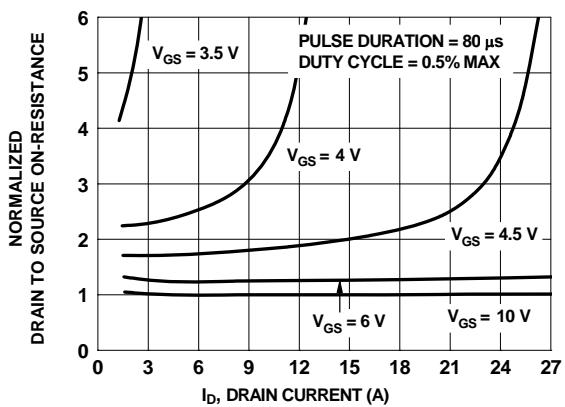


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

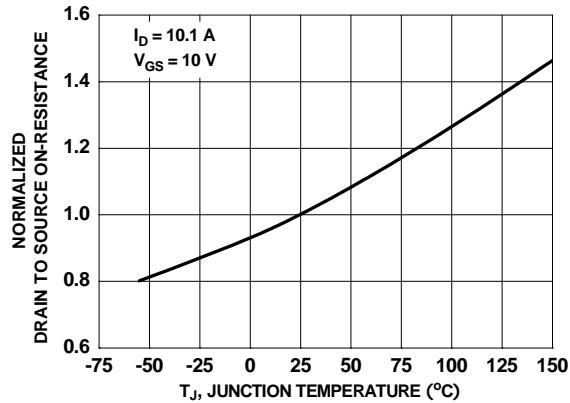


Figure 3. Normalized On Resistance vs Junction Temperature

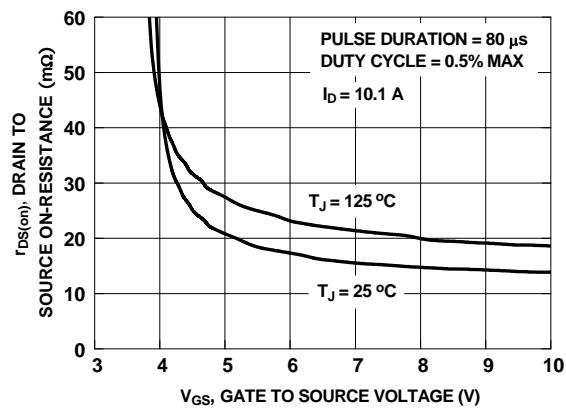


Figure 4. On-Resistance vs Gate to Source Voltage

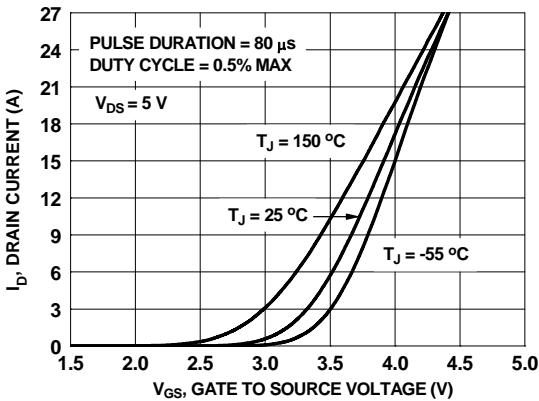


Figure 5. Transfer Characteristics

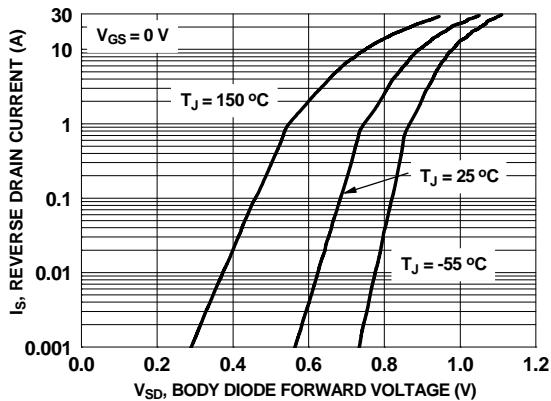


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

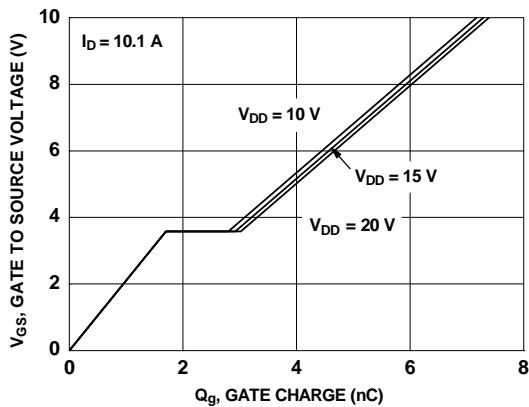


Figure 7. Gate Charge Characteristics

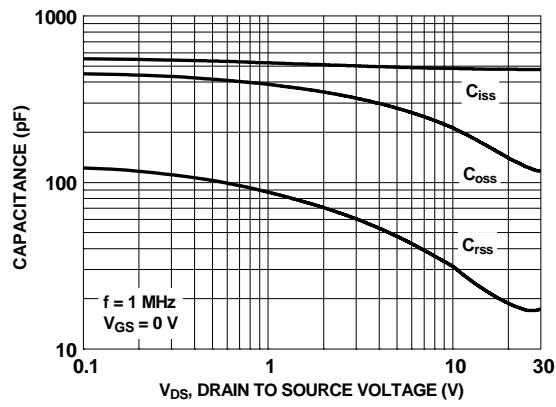


Figure 8. Capacitance vs Drain to Source Voltage

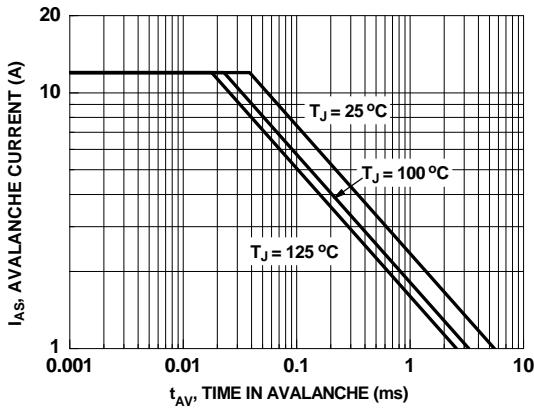


Figure 9. Unclamped Inductive Switching Capability

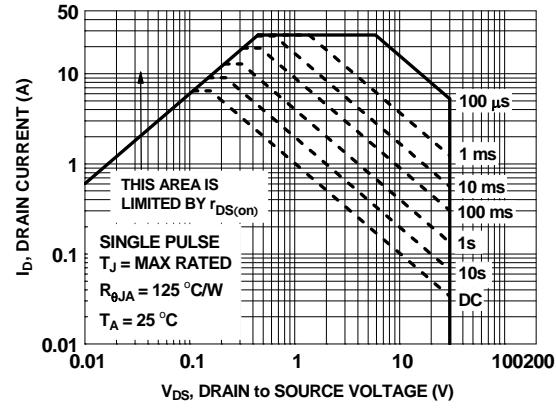


Figure 10. Forward Bias Safe Operating Area

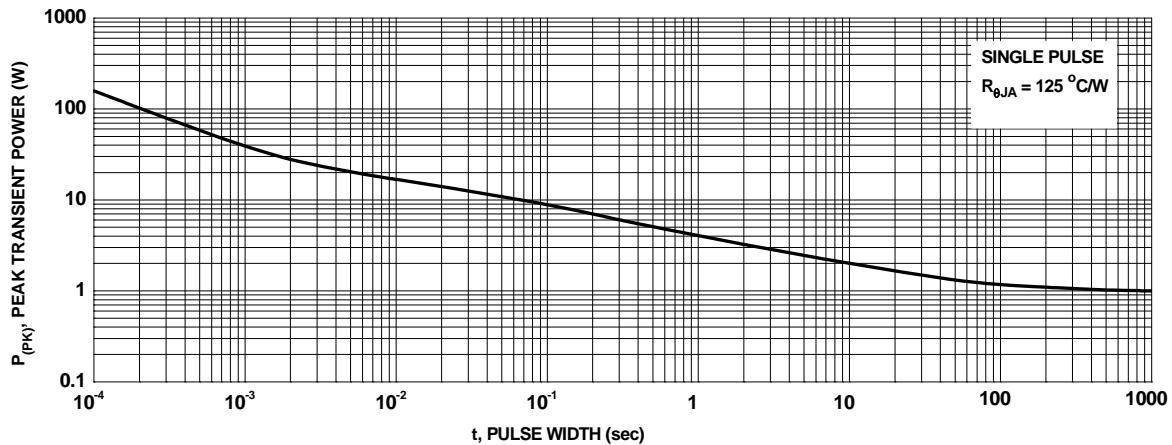


Figure 11. Single Pulse Maximum Power Dissipation

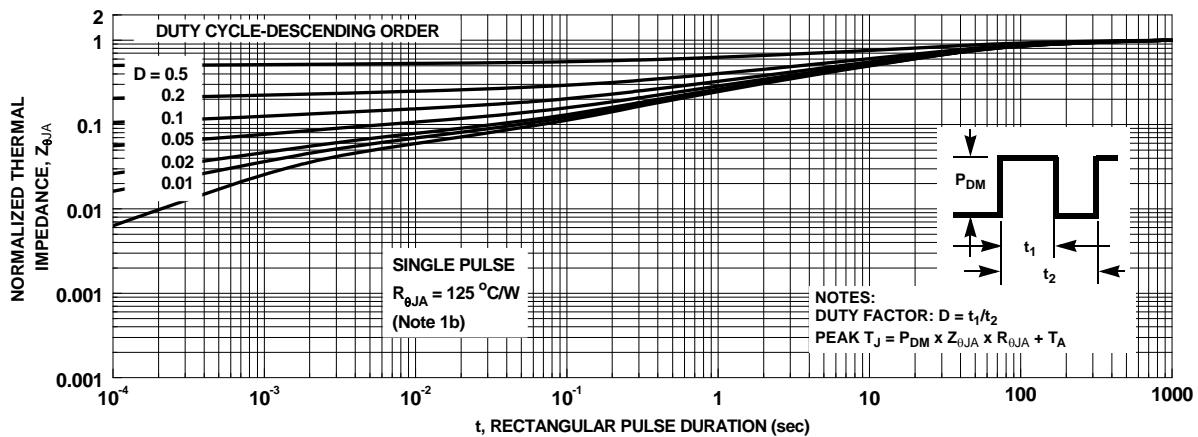
Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

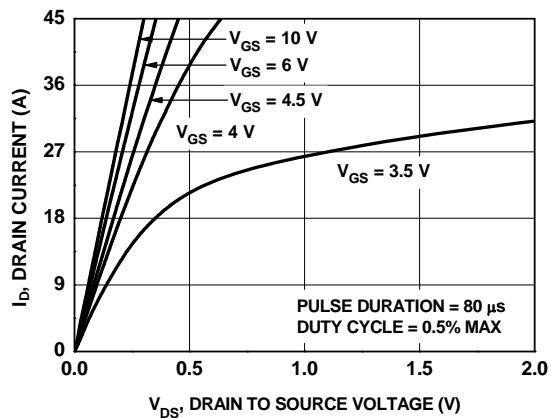


Figure 13. On-Region Characteristics

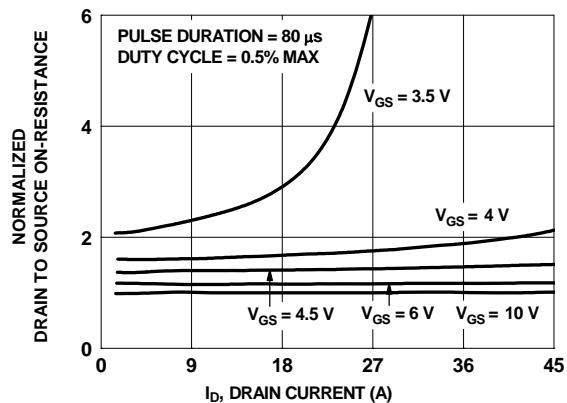


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

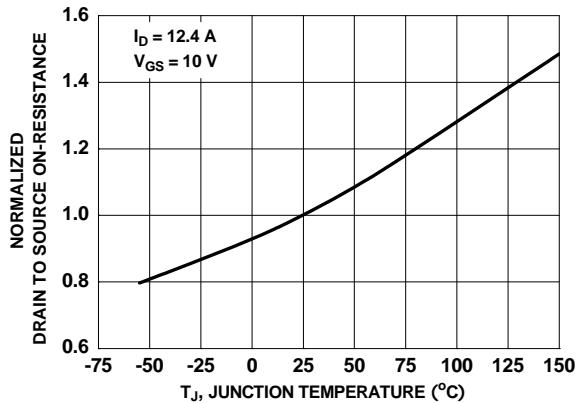


Figure 15. Normalized On-Resistance vs Junction Temperature

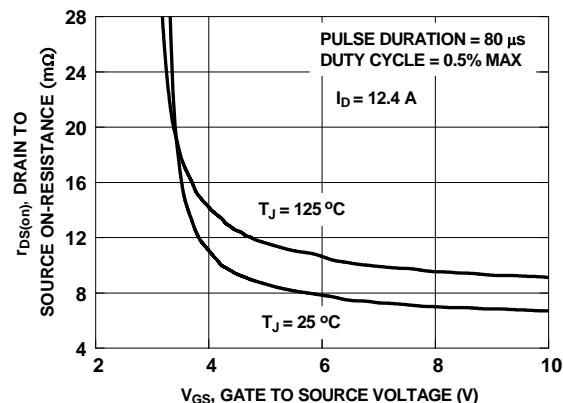


Figure 16. On-Resistance vs Gate to Source Voltage

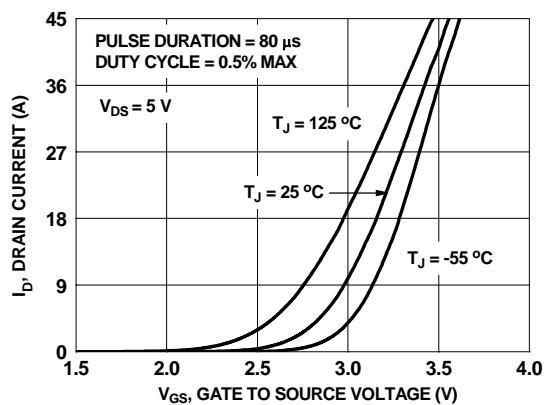


Figure 17. Transfer Characteristics

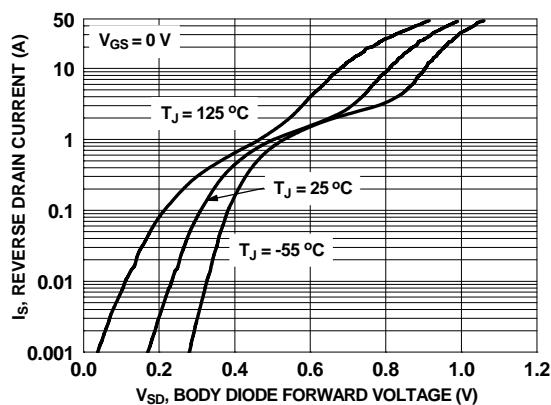


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

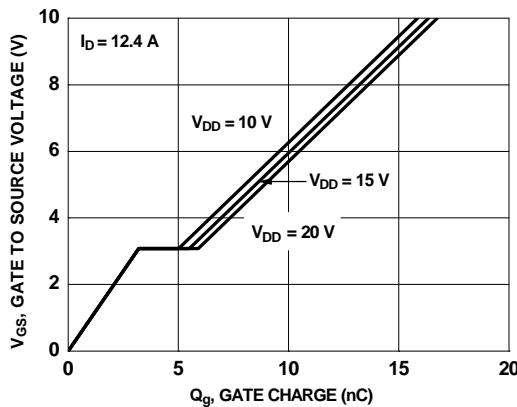


Figure 19. Gate Charge Characteristics

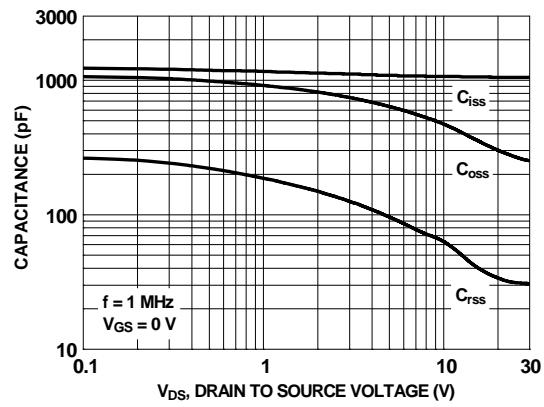


Figure 20. Capacitance vs Drain to Source Voltage

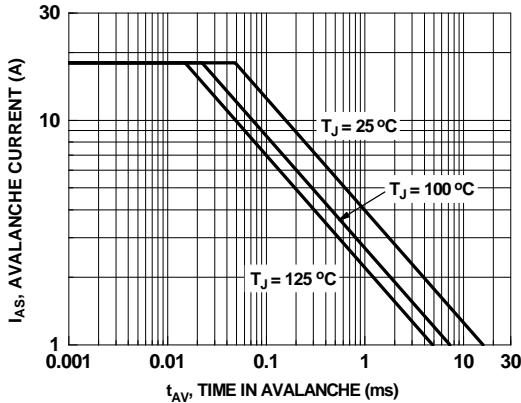


Figure 21. Unclamped Inductive Switching Capability

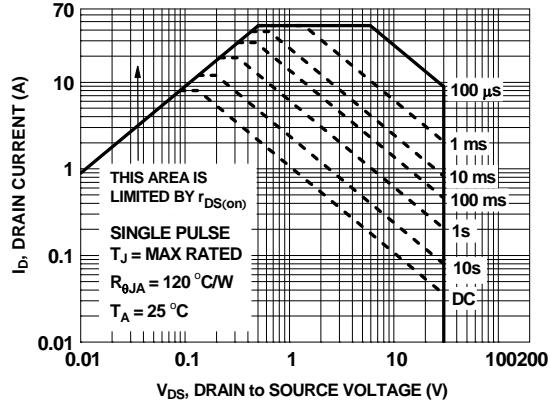


Figure 22. Forward Bias Safe Operating Area

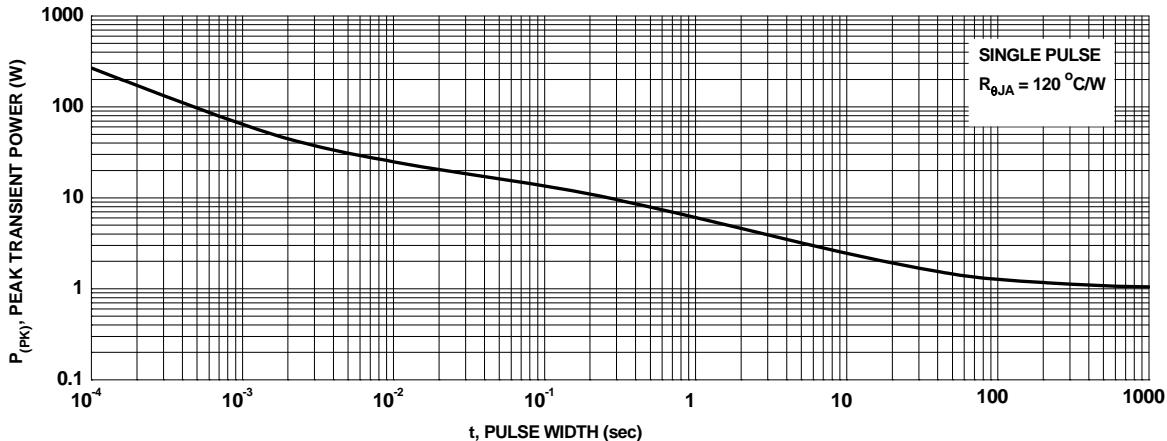


Figure 23. Single Pulse Maximum Power Dissipation

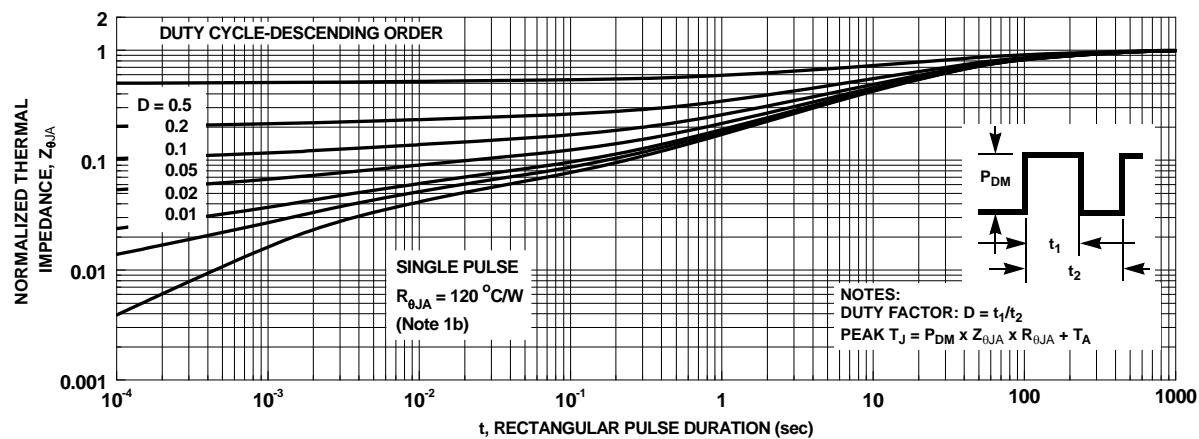
Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

Figure 24. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench® MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 26 shows the reverse recovery characteristic of the FDMS7620S.

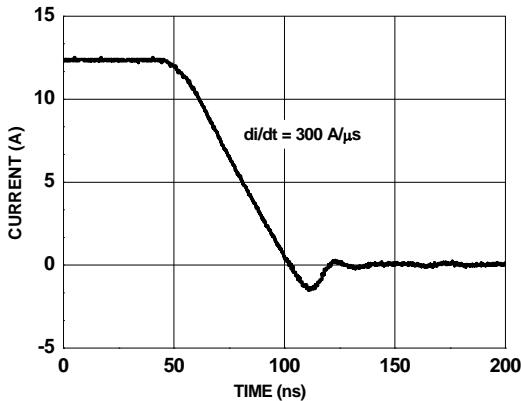


Figure 25. FDMS7620S SyncFET™ Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

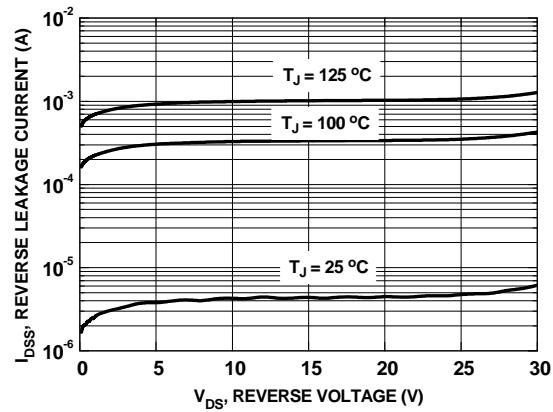
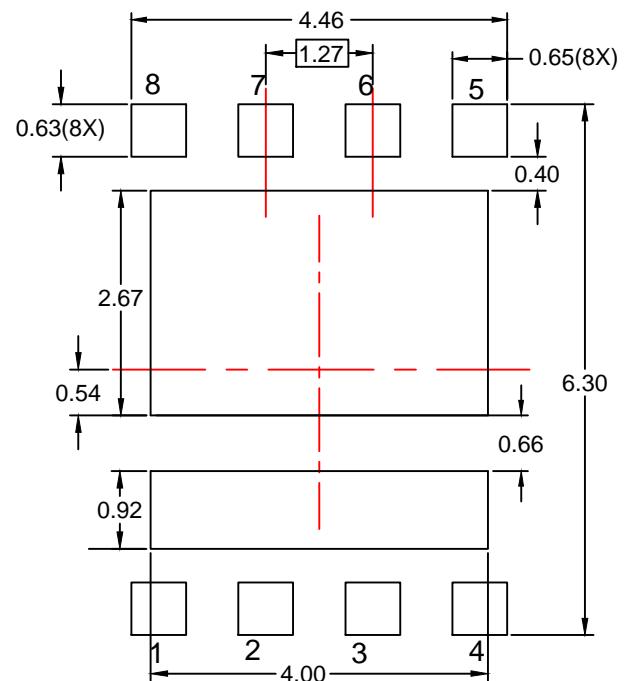
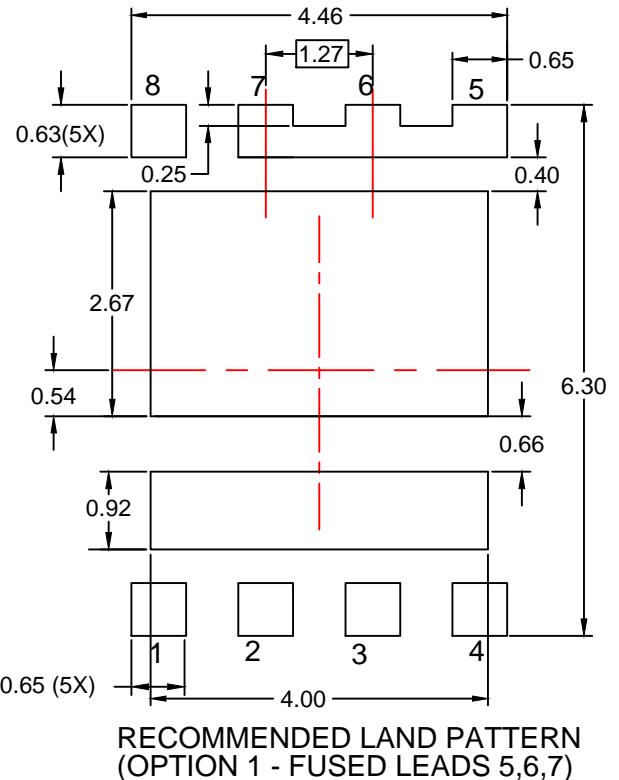
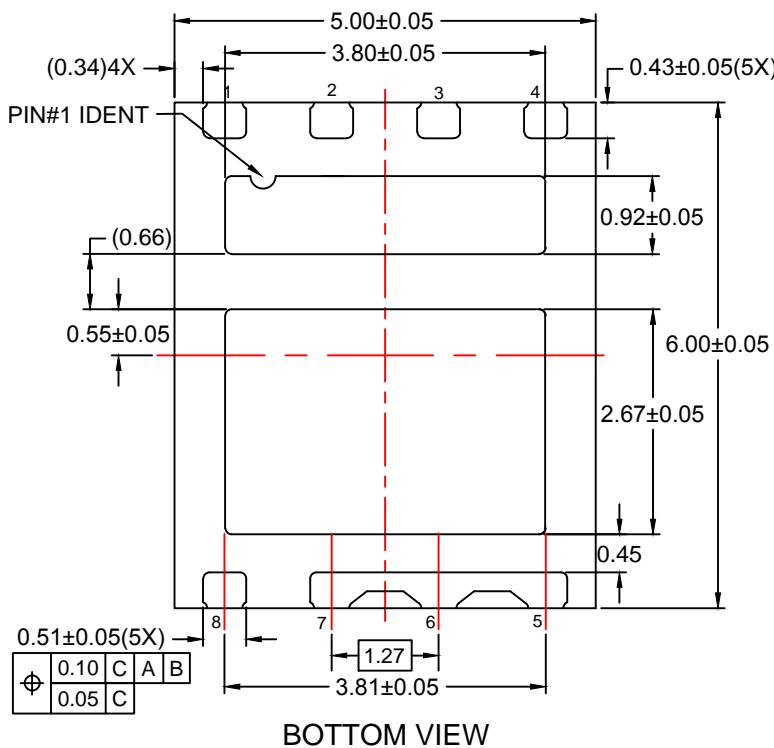
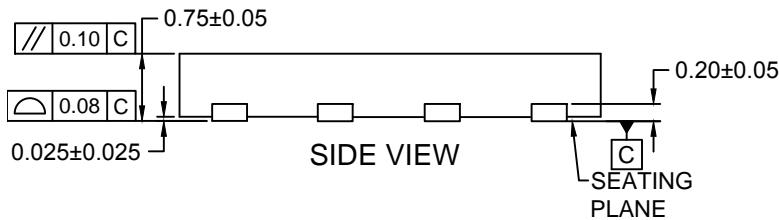
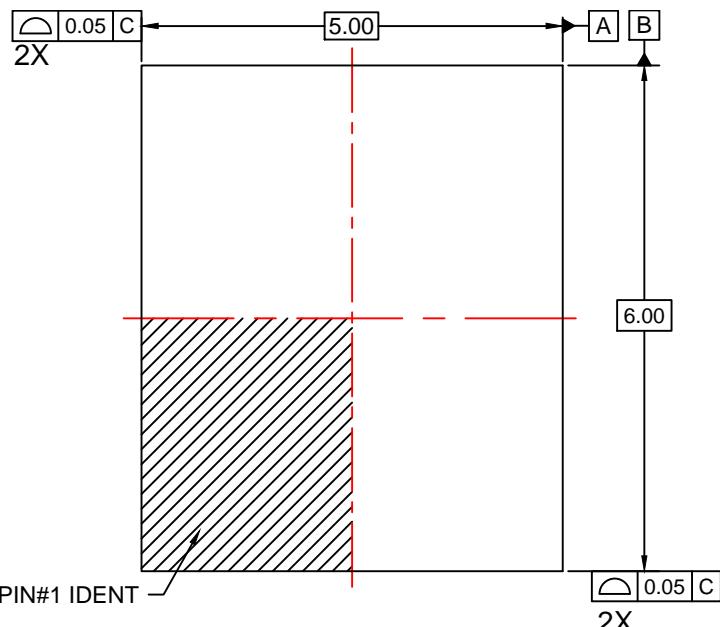


Figure 26. SyncFET™ Body Diode Reverse Leakage vs. Drain-Source Voltage



RECOMMENDED LAND PATTERN
(OPTION 2 - ISOLATED LEADS)

NOTES:

- PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- DRAWING FILENAME: MKT-MLP08Prev2.



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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