

# PSMN1R8-40YLC

N-channel 40 V 1.8 mΩ logic level MOSFET in LFPAK using  
NextPower technology

22 August 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low Rdson and low parasitic inductance

### 1.3 Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$		-	-	40	V
$I_D$	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}; V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 1</a>	[1]	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 2</a>		-	-	272	W
$T_j$	junction temperature			-55	-	175	$^{\circ}\text{C}$
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 12</a>		-	1.8	2.1	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 12</a>		-	1.5	1.8	$\text{m}\Omega$
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; V_{DS} = 20\text{ V}$ ; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>		-	10.9	-	nC



Scan or click this QR code to view the latest information for this product

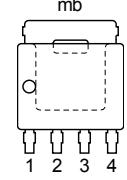
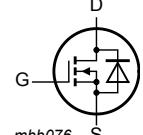


Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 4.5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $V_{DS} = 20 \text{ V}$ ; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>		-	45	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 LFPAK; Power-SO8 (SOT669)	 mbb076

## 3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description	Version	
PSMN1R8-40YLC	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads		SOT669

## 4. Limiting values

Table 4. Limiting values

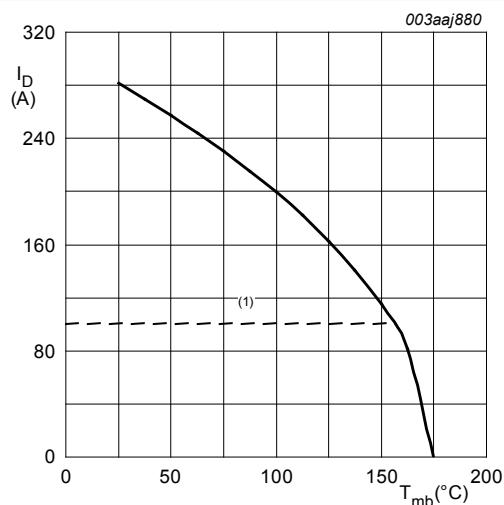
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25^\circ\text{C} \leq T_j \leq 175^\circ\text{C}$		-	40	V
$V_{DGR}$	drain-gate voltage	$25^\circ\text{C} \leq T_j \leq 175^\circ\text{C}$ ; $R_{GS} = 20 \text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage			-20	20	V
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25^\circ\text{C}$ ; <a href="#">Fig. 1</a>	[1]	-	100	A
		$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 100^\circ\text{C}$ ; <a href="#">Fig. 1</a>	[1]	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \mu\text{s}$ ; $T_{mb} = 25^\circ\text{C}$ ; <a href="#">Fig. 4</a>		-	1128	A
$P_{\text{tot}}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; <a href="#">Fig. 2</a>		-	272	W
$T_{\text{stg}}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
$T_{\text{sld(M)}}$	peak soldering temperature			-	260	°C

## N-channel 40 V 1.8 mΩ logic level MOSFET in LFPAK using NextPower technology

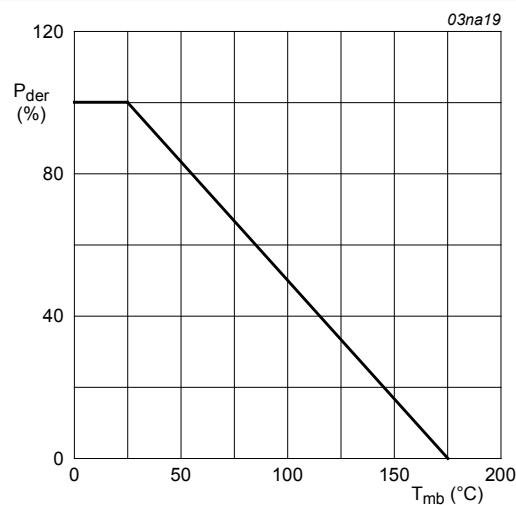
Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>ESD</sub>	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		890	-	V
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 µs; T <sub>mb</sub> = 25 °C		-	1128	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; unclamped; Fig. 3		-	248	mJ

[1] Continuous current is limited by package.



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$V_{GS} \geq 10 V$   
(1) Capped at 100 A due to package.



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100 \%$$

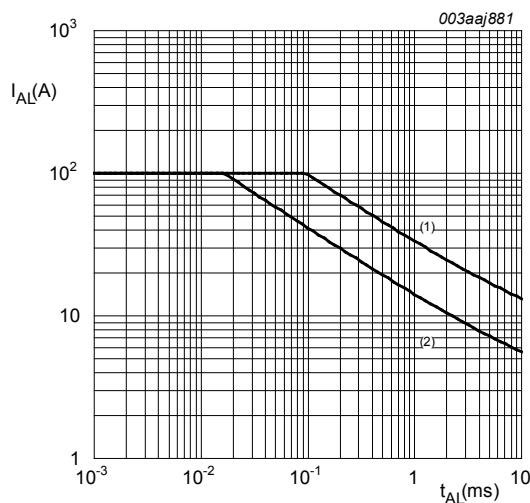


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

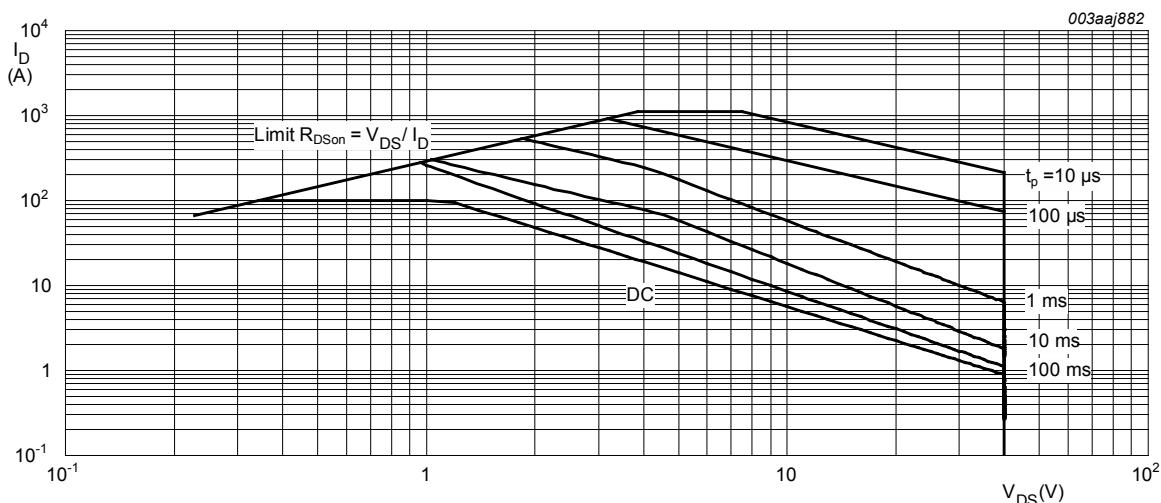
(1)  $T_j \text{ (init)} = 25^\circ\text{C}$ ; (2)  $T_j \text{ (init)} = 100^\circ\text{C}$ 

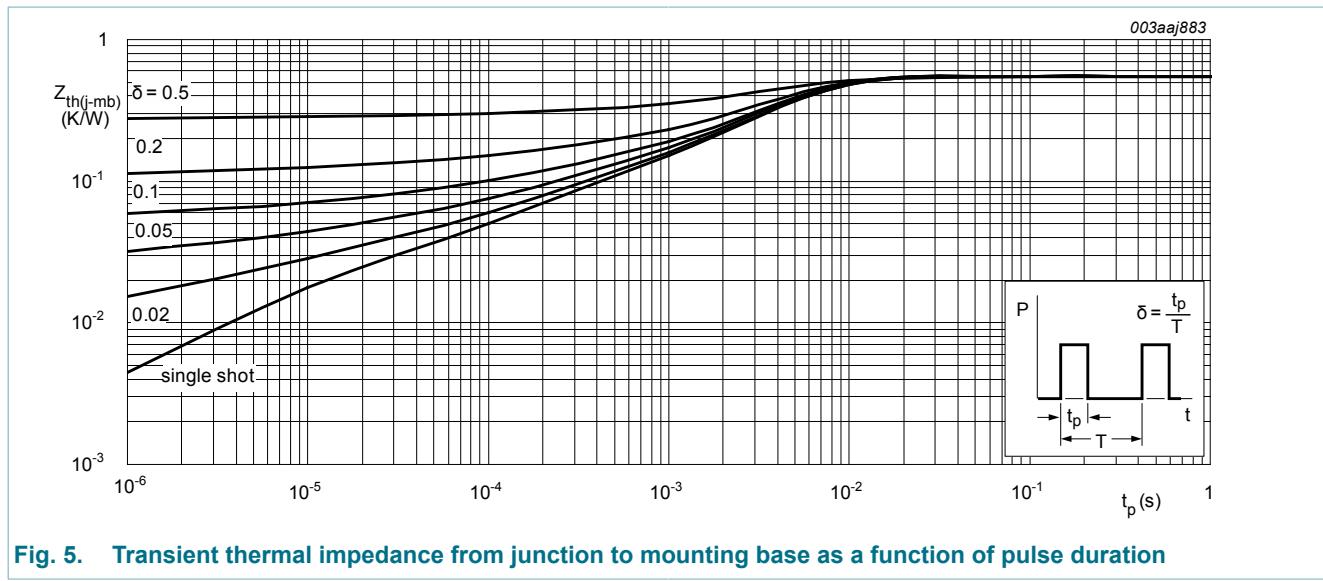
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is a single pulse

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>		-	0.45	0.55	K/W



## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		40	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C		36	-	-	V
<b>Dynamic characteristics</b>							
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		1.05	1.45	1.95	V
		I <sub>D</sub> = 10 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 150 °C; <a href="#">Fig. 11</a>		0.5	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; <a href="#">Fig. 11</a>		-	-	2.25	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C		-	-	100	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a>		-	1.8	2.1	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 150 °C; <a href="#">Fig. 12; Fig. 13</a>		-	-	3.6	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a>		-	1.5	1.8	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 150 °C; <a href="#">Fig. 12; Fig. 13</a>		-	-	3.25	mΩ

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_G$	gate resistance	$f = 1 \text{ MHz}$		0.5	1	2	Ω
<b>Dynamic characteristics</b>							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	96	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V};$ <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>		-	45	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$		-	88	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V};$ <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>		-	15.5	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge			-	8.4	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge			-	7.1	-	nC
$Q_{GD}$	gate-drain charge			-	10.9	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V};$ <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>		-	2.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25^\circ\text{C}$ ; <a href="#">Fig. 16</a>		-	6680	-	pF
$C_{oss}$	output capacitance			-	825	-	pF
$C_{rss}$	reverse transfer capacitance			-	310	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 0.8 \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(\text{ext})} = 5 \Omega$		-	32.2	-	ns
$t_r$	rise time			-	37	-	ns
$t_{d(\text{off})}$	turn-off delay time			-	62.5	-	ns
$t_f$	fall time			-	31.7	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25^\circ\text{C}$		-	30	-	nC
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C};$ <a href="#">Fig. 17</a>		-	0.77	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}$		-	37	-	ns
$Q_r$	recovered charge			-	43	-	nC
$t_a$	reverse recovery rise time	$V_{GS} = 0 \text{ V}; I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$ $V_{DS} = 20 \text{ V};$ <a href="#">Fig. 18</a>		-	21	-	ns
$t_b$	reverse recovery fall time			-	16	-	ns

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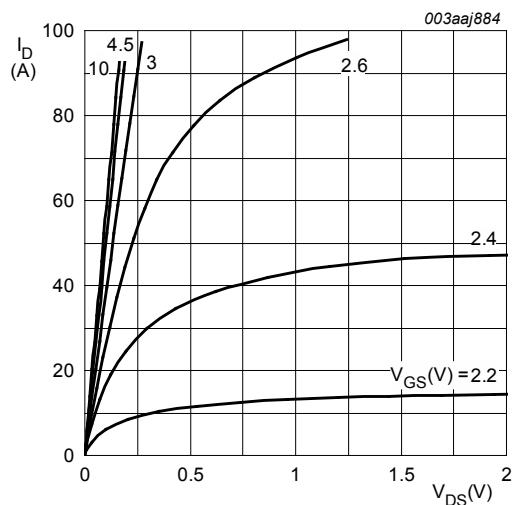


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ C$

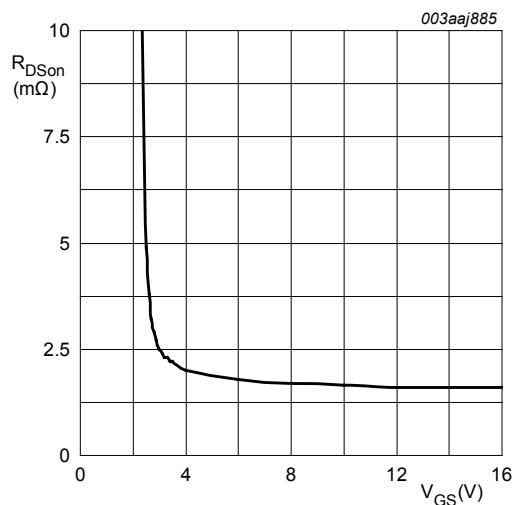


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ C; I_D = 25A$

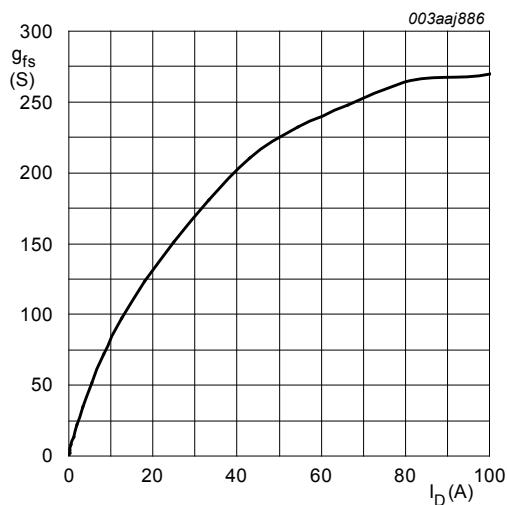


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ C; V_{DS} = 10V$

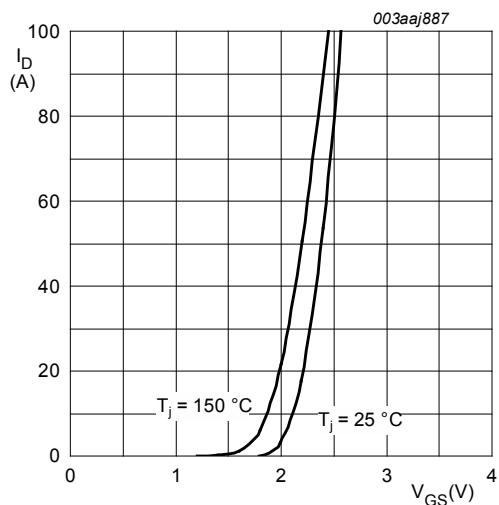


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

## N-channel 40 V 1.8 mΩ logic level MOSFET in LFPAK using NextPower technology

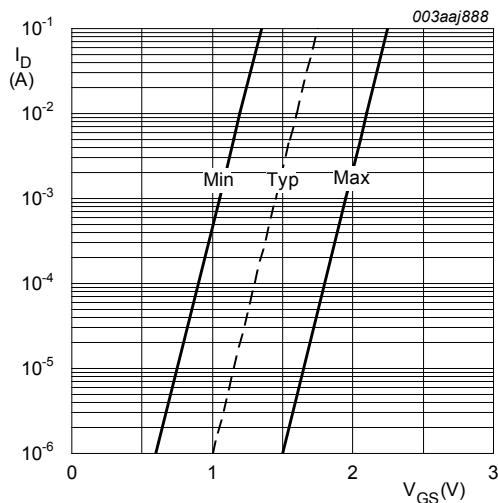


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}$ ;  $V_{DS} = 5\text{V}$

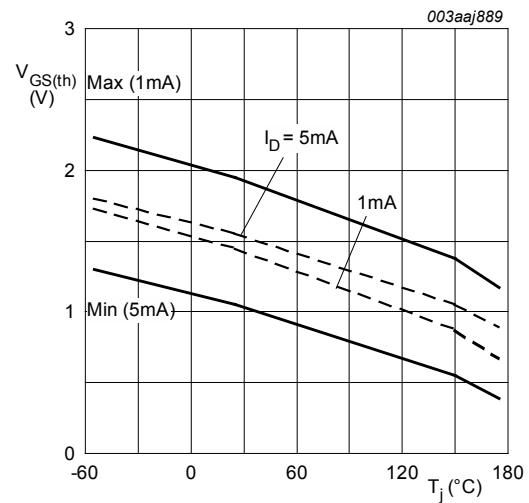


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$V_{DS} = V_{GS}$

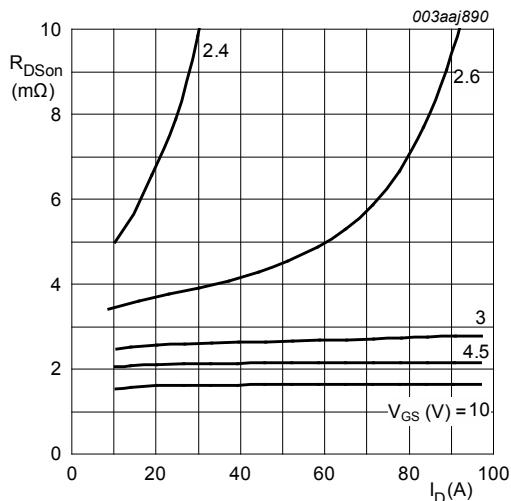


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

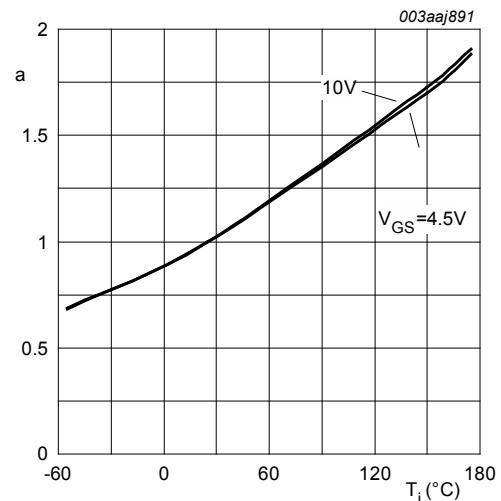


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

## N-channel 40 V 1.8 mΩ logic level MOSFET in LFPAK using NextPower technology

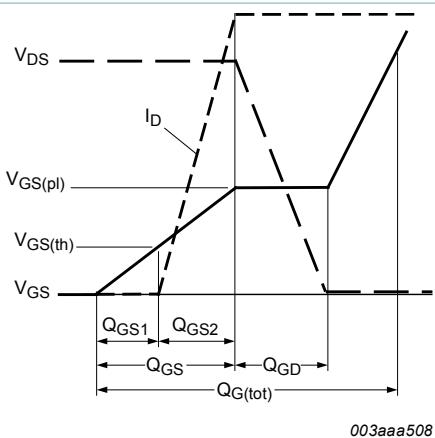


Fig. 14. Gate charge waveform definitions

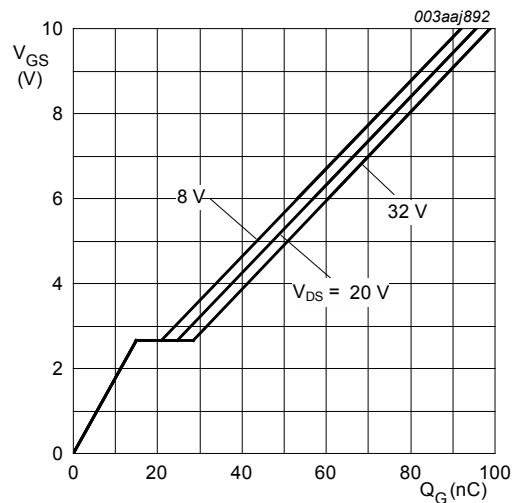


Fig. 15. Gate-source voltage as a function of gate charge; typical values

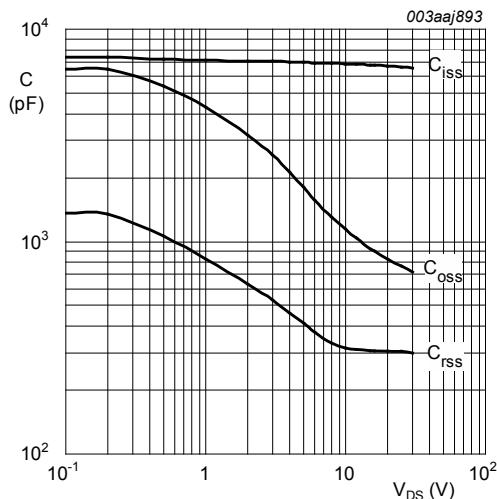
 $T_j = 25^\circ\text{C}$ ;  $I_D = 25\text{A}$ 

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

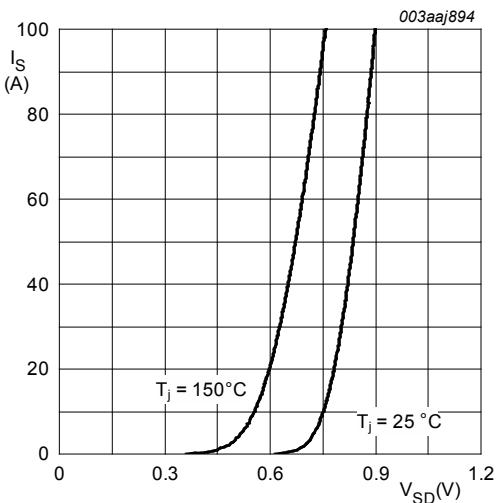
 $V_{GS} = 0\text{V}$ ;  $f = 1\text{MHz}$ 

Fig. 17. Source current as a function of source-drain voltage; typical values

 $V_{GS} = 0\text{V}$

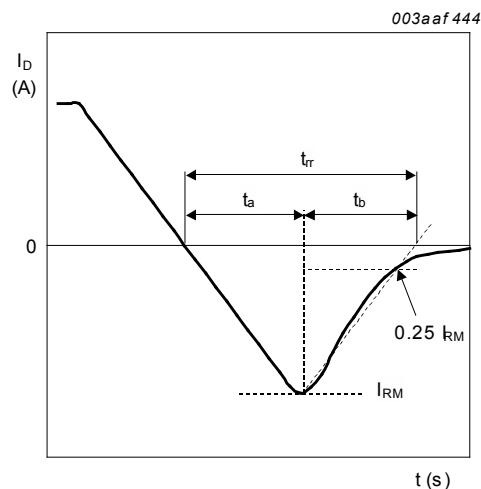
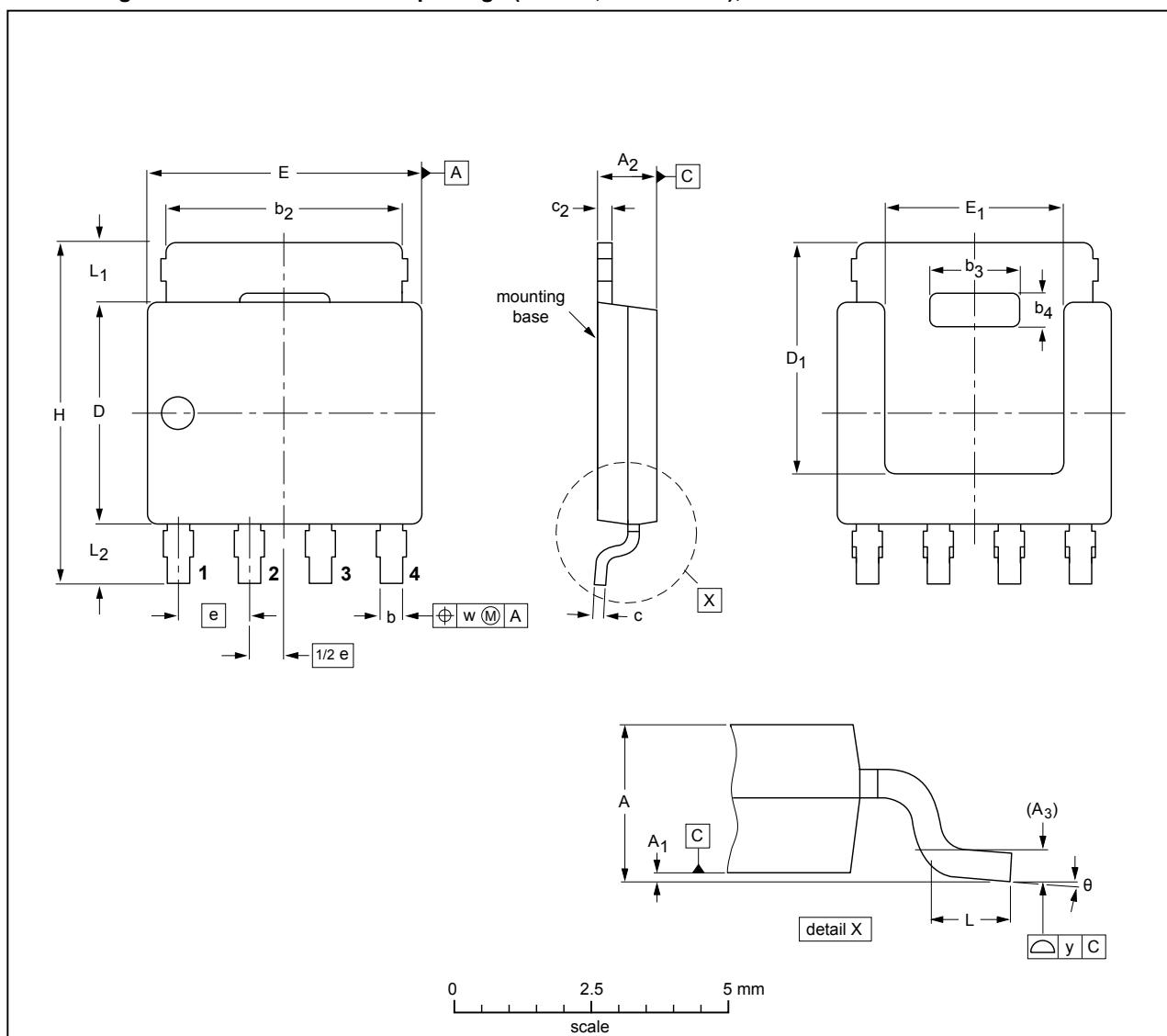


Fig. 18. Reverse recovery timing definition

## 7. Package outline

Plastic single-ended surface-mounted package (LFPAK; Power-SO8); 4 leads

SOT669



### DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup> max	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT669		MO-235			06-03-16 11-03-25

Fig. 19. Package outline LFPAK; Power-SO8 (SOT669)

## 8. Legal information

### 8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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