

HD74LS174 / HD74LS175

Hex / Quadruple D-type Flip-Flops (with clear)

REJ03D0451-0300

Rev.3.00

Jul.15.2005

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the HD74LS175 features complementary outputs from each flip-flops. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the outputs.

Features

- Ordering Information

• HD74LS174

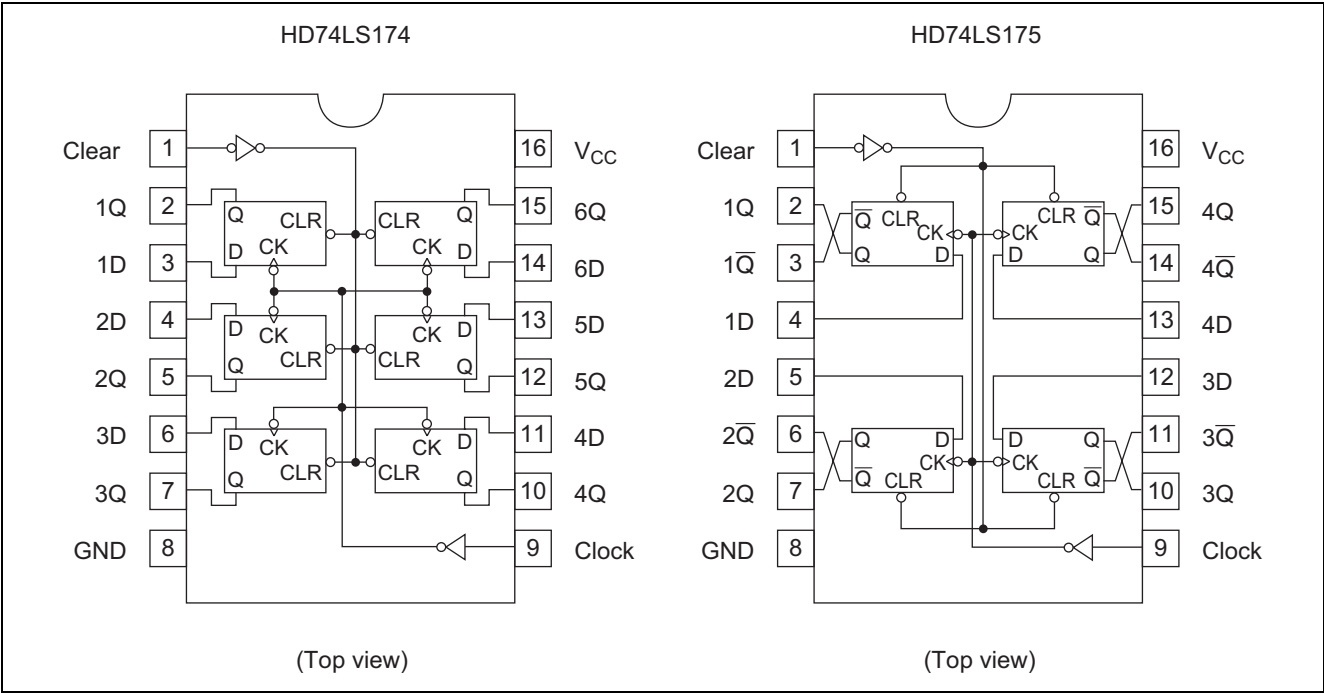
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS174P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS174FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS174RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

• HD74LS175

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS175P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS175FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS175RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

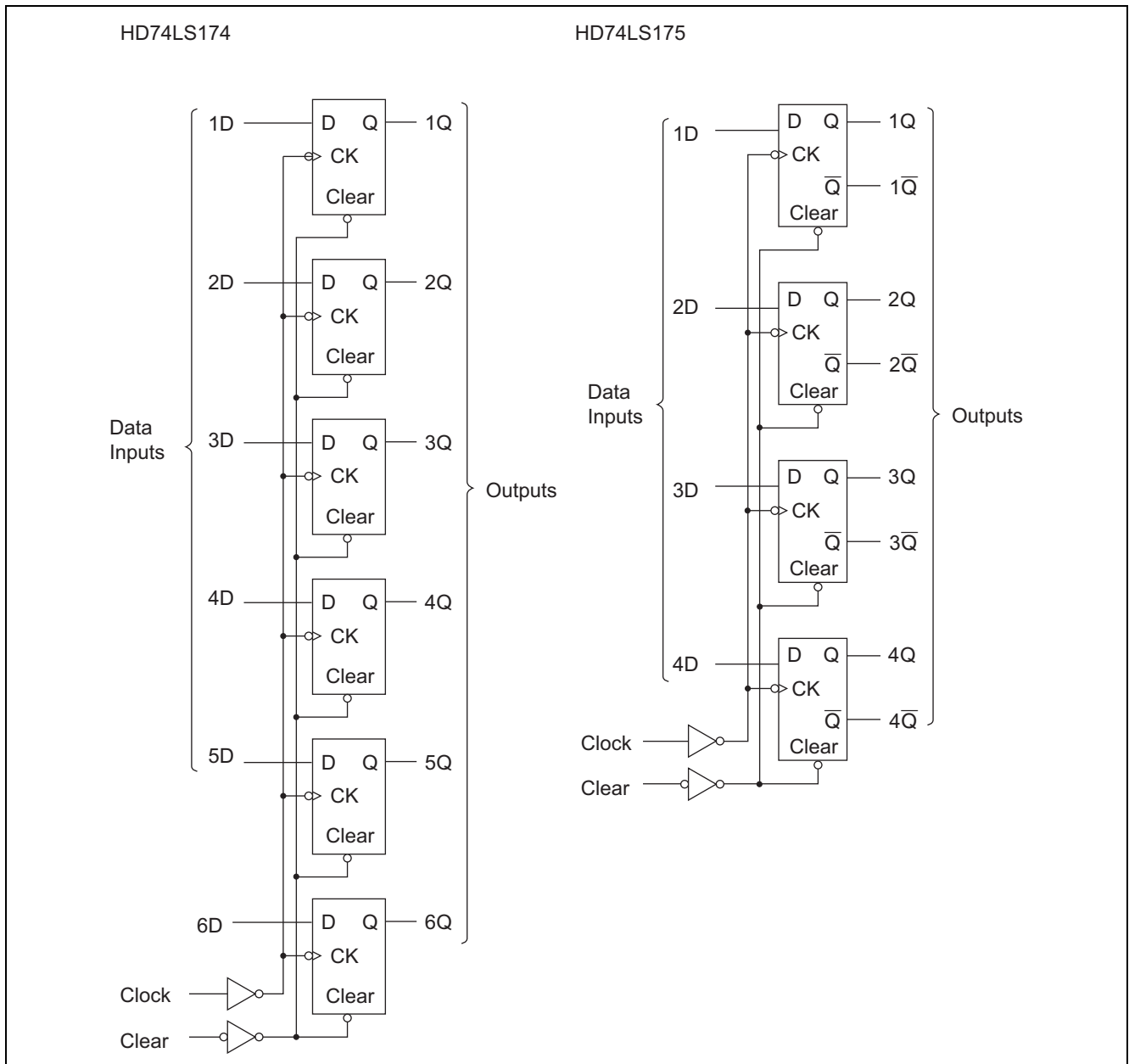


Function Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	L	X	Q ₀	$\overline{Q}_0$

- Notes:
1. H; high level, L; low level, X; irrelevant
 2. $\uparrow$; transition from low to high level
 3. Q₀; the level of Q before the indicated steady-state input conditions were established.
 4. $\overline{Q}$ is applied to HD74LS175 only.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

• HD74LS174

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	−400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	−20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Clock pulse width	$t_w (CK)$	20	—	—	ns
Clear pulse width	$t_w (CLR)$	20	—	—	ns
Setup time	Data input	$t_{su} (data)$	20	—	ns
	Clear inactive-state	$t_{su} (CLR)$	25	—	ns
Data hold time	$t_h (data)$	5	—	—	ns

• HD74LS175

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	−400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	−20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Clock pulse width	$t_w (CK)$	20	—	—	ns
Clear pulse width	$t_w (CLR)$	20	—	—	ns
Setup time	Data input	$t_{su} (data)$	20	—	ns
	Clear inactive-state	$t_{su} (CLR)$	25	—	ns
Data hold time	$t_h (data)$	5	—	—	ns

Electrical Characteristics

(Ta = −20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	$V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -400 \mu A$
	V_{OL}	—	—	0.5	V	$I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V$
Input current	I_{IH}	—	—	20	μA	$V_{CC} = 5.25 V, V_I = 2.7 V$
	I_{IL}	—	—	−0.4	mA	$V_{CC} = 5.25 V, V_I = 0.4 V$
	I_I	—	—	0.1	mA	$V_{CC} = 5.25 V, V_I = 7 V$
Short-circuit output current	I_{OS}	−20	—	−100	mA	$V_{CC} = 5.25 V$
Supply current**	I_{CC}	—	16	26	mA	HD74LS174
		—	11	18	mA	HD74LS175
Input clamp voltage	V_{IK}	—	—	−1.5	V	$V_{CC} = 4.75 V, I_{IN} = -18 mA$

Notes: * $V_{CC} = 5 V, T_a = 25^\circ C$ ** With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary grounded, then 4.5 V, is applied to clock.

Switching Characteristics

• HD74LS174

($V_{CC} = 5\text{ V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{\max}$	Clock	Q	30	40	—	MHz	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$
Propagation delay time	t_{PHL}	Clear	Q	—	23	35	ns	
	t_{PLH}	Clock	Q	—	20	30		
	t_{PHL}	Clock	Q	—	21	30		

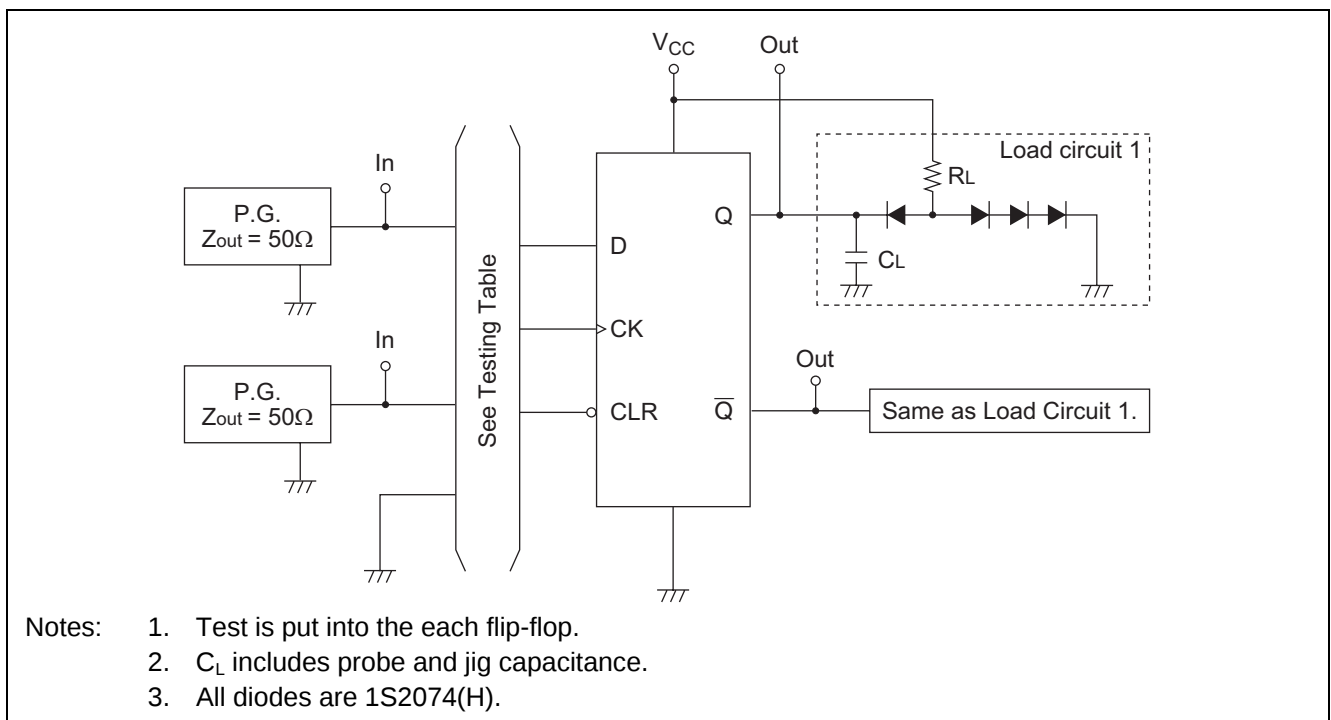
• HD74LS175

($V_{CC} = 5\text{ V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{\max}$	Clock	Q, $\overline{Q}$	30	40	—	MHz	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$
Propagation delay time	t_{PLH}	Clear	$\overline{Q}$	—	16	25	ns	
	t_{PHL}		Q	—	20	30		
	t_{PLH}	Clock	Q, $\overline{Q}$	—	13	25		
	t_{PHL}	Clock	Q, $\overline{Q}$	—	16	25		

Testing Method

Test Circuit

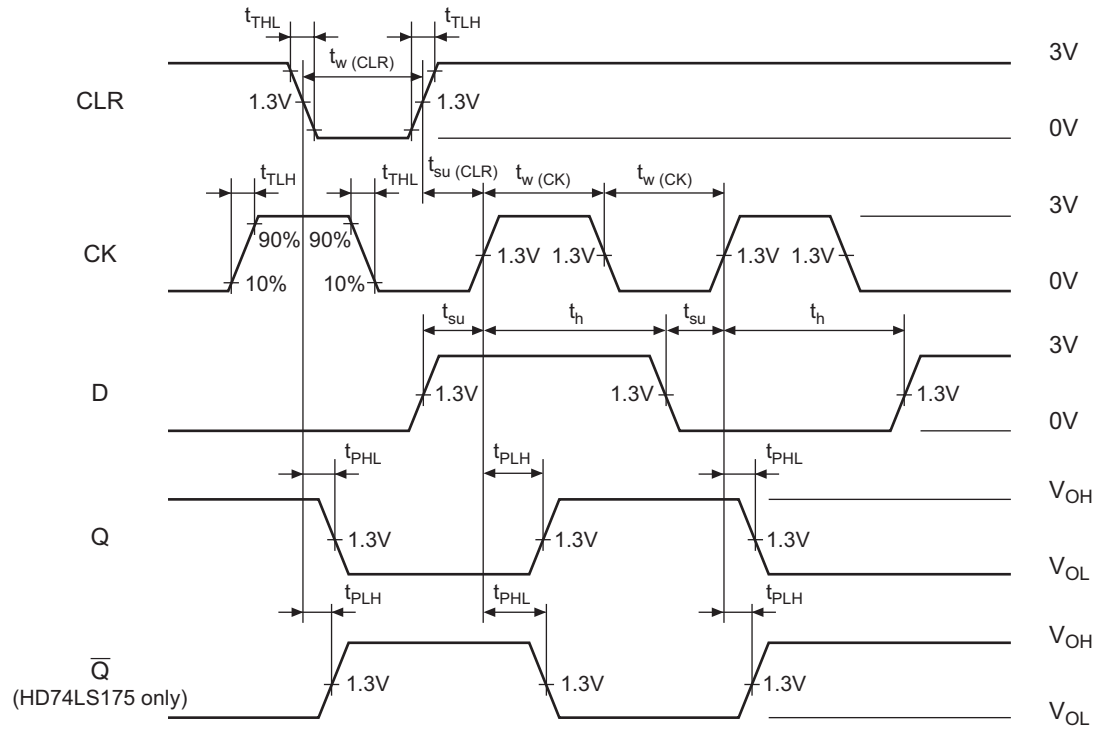


Testing Table

Item	From input to output	Inputs			Outputs	
		CLR	CK	D	Q	$\bar{Q}$
$f_{\max}$	CK→Q, $\bar{Q}^*$	4.5 V	IN	IN	OUT	OUT
t_{PLH}	CK→Q, $\bar{Q}^*$	4.5 V	IN	IN		
t_{PHL}	CLR→Q, $\bar{Q}^*$	IN	IN	4.5 V		

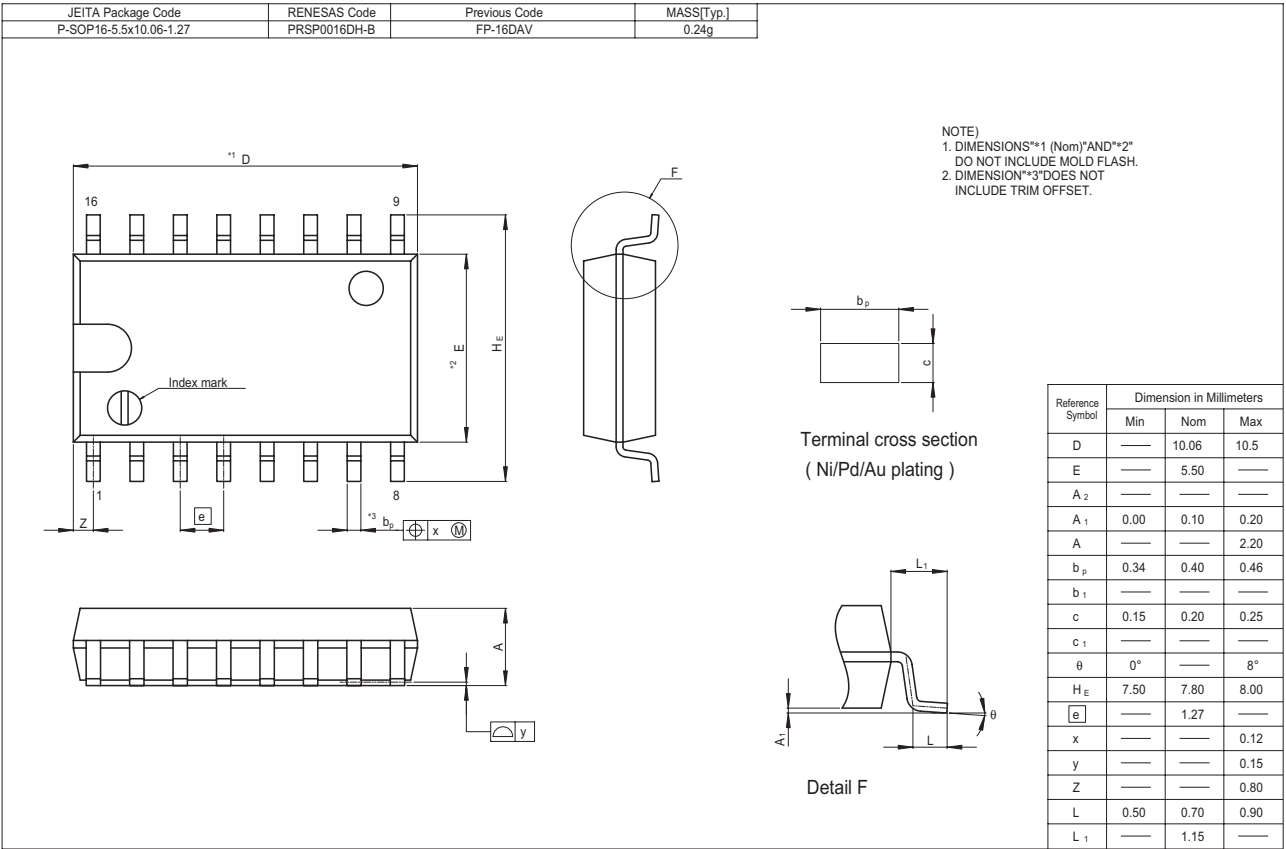
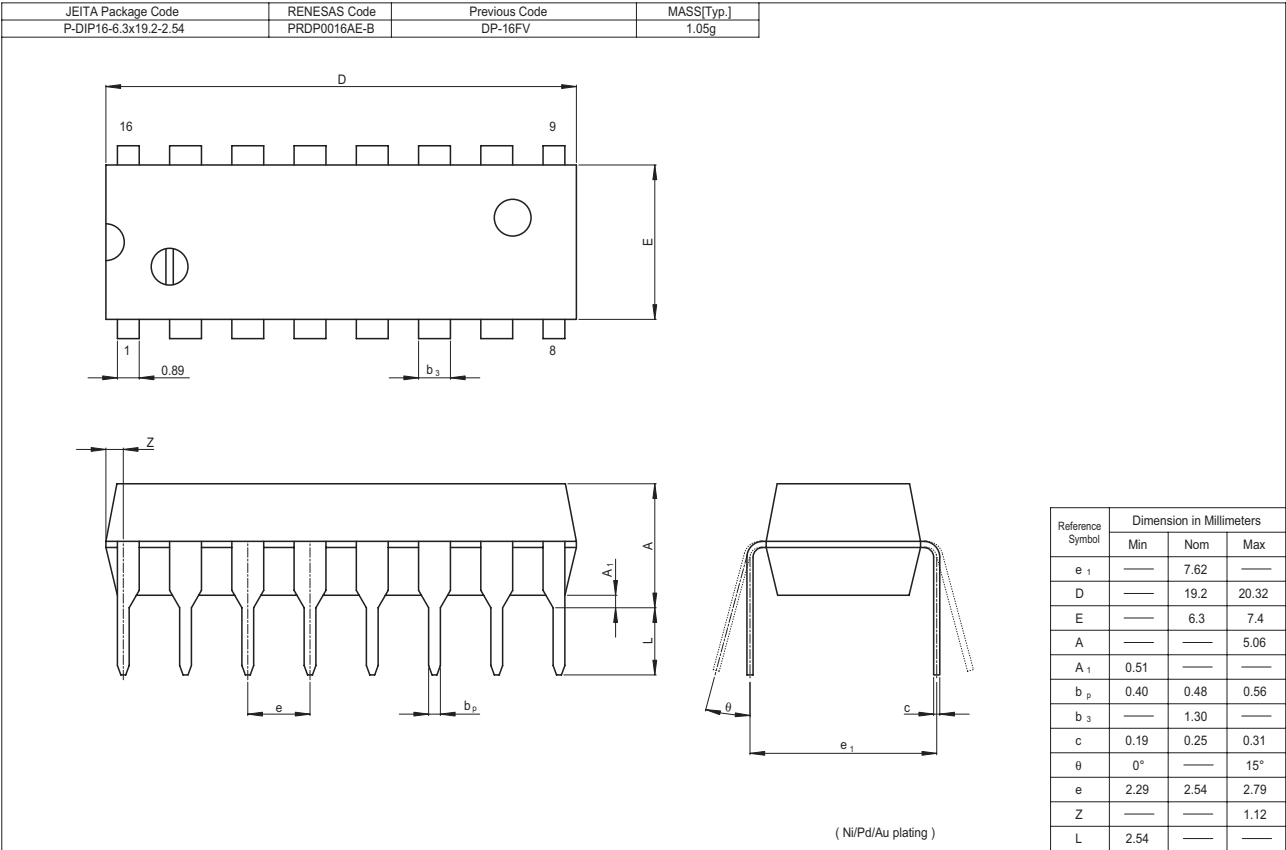
Note: *. HD74LS175 only

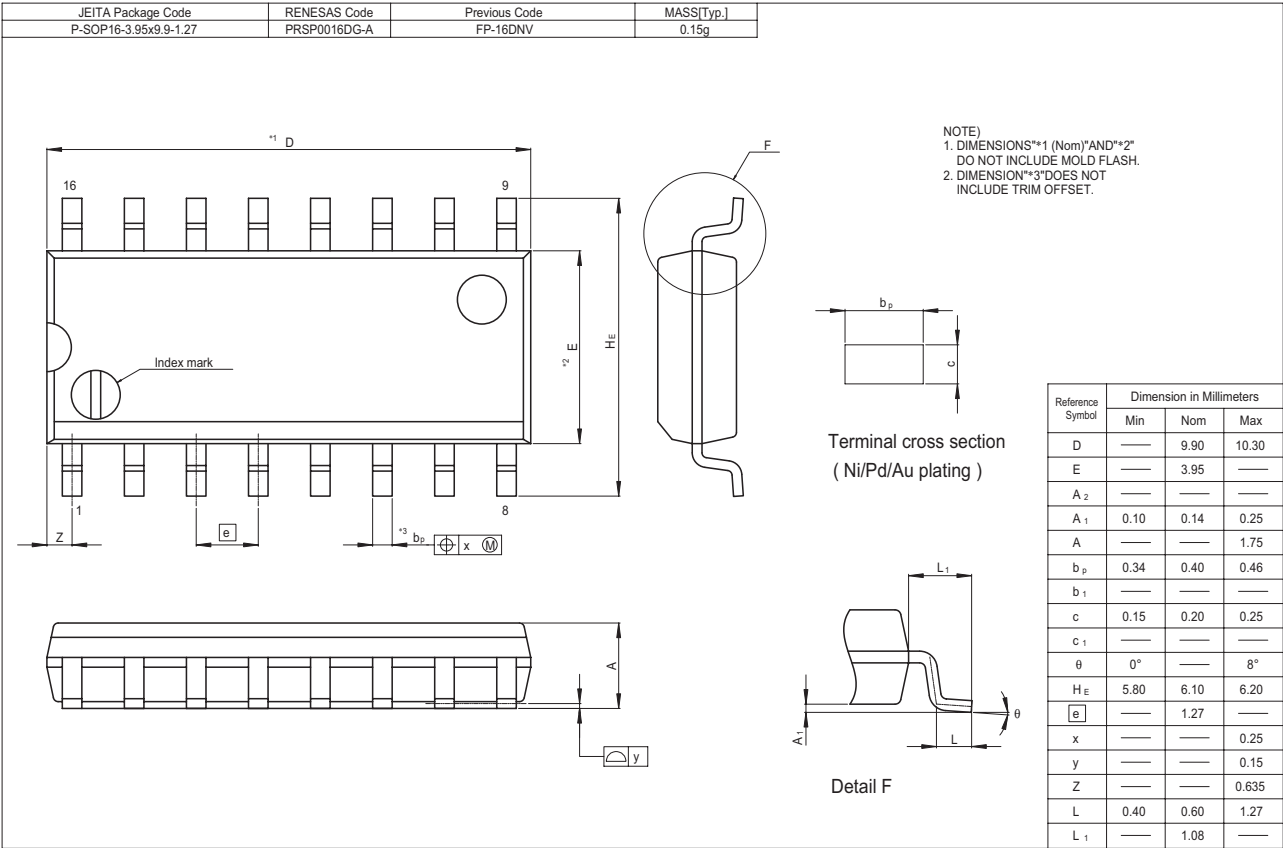
Waveform



Note: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, and: for f_{max} , $t_{TLH} = t_{THL} \leq 2.5$ ns.

Package Dimensions





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