- **Converts Light Intensity to Digital Signal**
- **Infrared Compensation to Approximate Human Eye Response**
- **Companding A/D for Wide Dynamic Range**
- **Rejects 50 Hz/60 Hz Lighting Ripple**
- **Two-Wire SMBus Serial Interface**
- **Single Supply Operation (2.7 V to 5.5 V)**
- **Low Active Power (1 mW typ)**
- **Power Down Mode**
- **Low-Profile Surface-Mount Package**

PACKAGE D
8-LEAD SOIC
(TOP VIEW)

V_{DD} 1	8 SMBData
NC 2	7 NC
NC 3	6 NC
GND 4	5 SMBCLK

PACKAGE T
4-LEAD SMD
(TOP VIEW)

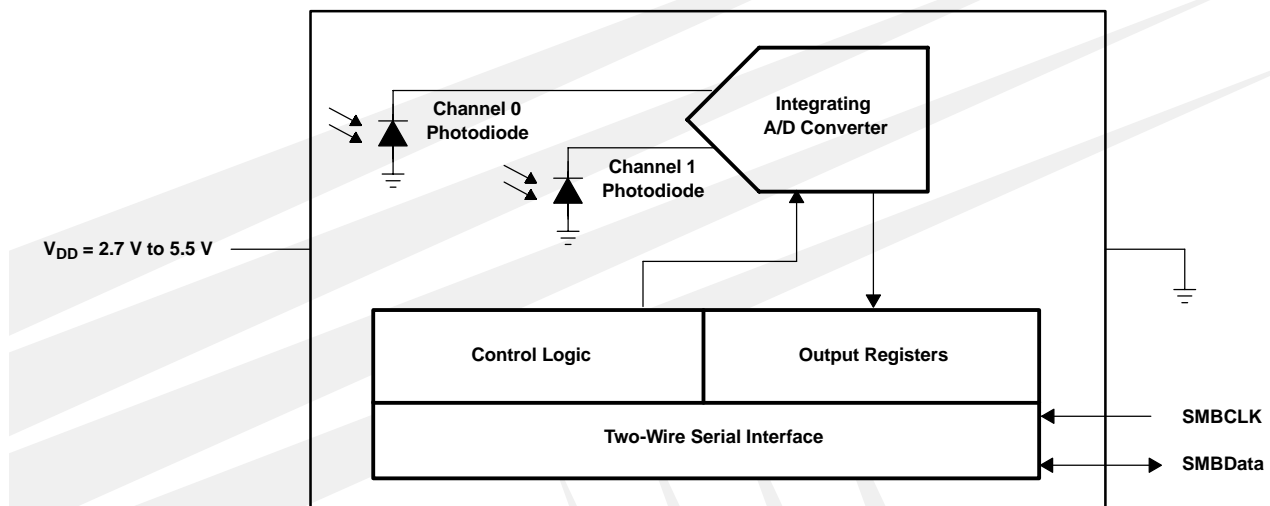|	
V_{DD} 1	4 SMBData
GND 2	3 SMBCLK

Description

The TSL2550 is a digital light sensor with a two-wire, SMBus serial interface. It combines two photodiodes and a companding analog-to-digital converter (ADC) on a single CMOS integrated circuit to provide light measurements over an effective 12-bit dynamic range.
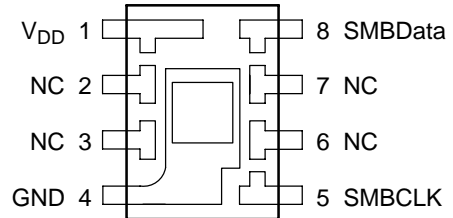
The TSL2550 is designed for use with broad wavelength light sources. One of the photodiodes (Channel 0) is sensitive to visible and infrared light, while the second photodiode (Channel 1) is sensitive primarily to infrared light. An integrating ADC converts the photodiode currents to Channel 0 and Channel 1 digital outputs. Channel 1 digital output is used to compensate for the effect of the infrared component of ambient light on Channel 0 digital output. The ADC digital outputs of the two channels are used to obtain a value that approximates the human eye response in the commonly used unit of Lux.

This device is intended primarily for use in applications in which measurement of ambient light is used to control display backlighting such as laptop computers, PDAs, camcorders, and GPS systems. Other applications include contrast control in LED signs and displays, camera exposure control, lighting controls, etc. The integrating conversion technique used by the TSL2550 effectively eliminates the effect of flicker from AC-powered lamps, increasing the stability of the measurement.
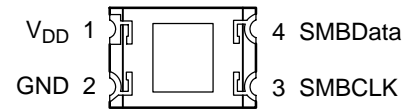
Functional Block Diagram

Texas Advanced Optoelectronic Solutions Inc.
800 Jupiter Road, Suite 205 • Plano, TX 75074 • (972) 673-0759

Terminal Functions

TERMINAL			TYPE	DESCRIPTION
NAME	D PKG NO.	T PKG NO.		
GND	4	2		Power supply ground. All voltages are referenced to GND.
SMBCLK	5	3	I	SMBus serial clock input terminal — clock signal for SMBus serial data.
SMBData	8	4	I/O	SMBus serial data I/O terminal — serial data I/O for SMBus.
V_{DD}	1	1		Supply voltage.

Available Options

DEVICE	T_A	PACKAGE - LEADS	PACKAGE DESIGNATOR	ORDERING NUMBER
TSL2550	- 25°C to 85°	SOIC-8	D	TSL2550D
TSL2550	- 25°C to 85°	T-4	T	TSL2550T

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1) . . . . 6 V
Digital output voltage range, V_O . . . . -0.3 V to +6 V
Digital output current, I_O . . . . ±10 mA
SMBus input/output current, $I_{(SMBIN)}$ . . . . -1 mA to 20 mA
Operating free-air temperature range, T_A . . . . -25 °C to 85°C
Storage temperature range, T_{stg} . . . . - 25°C to 85°C
ESD tolerance, human body model . . . . 2000 V

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:   All voltages are with respect to GND.

Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	5.5	V
Operating free-air temperature, T_A	0	70	°C
SMBus input low voltage @ V_{DD} = 3.3 V ± 5%, V_{IL}		0.8	V
SMBus input high voltage @ V_{DD} = 3.3 V ± 5%, V_{IH}	2.1		V
SMBus operating frequency, $f_{(SMBCLK)}$	10	100	kHz

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Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	SMBus output low voltage	$I_O = 50\ \mu A$		0.01		V
		$I_O = 4\ mA$			0.4	
I_{DD}	Supply current	Active, VSMBCLK and VSMDATA = V_{DD}, $V_{DD} = 3.3\ V \pm 5\%$		0.35	0.6	mA
		Power down, VSMBCLK and VSMDATA = V_{DD}, $V_{DD} = 3.3\ V \pm 5\%$			10	μA
I_{IH}	High level input current	$VI = V_{DD}$			5	μA
I_{IL}	Low level input current	$VI = 0$			-5	μA

Operating Characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted) (see Notes 2, 3, 4)

PARAMETER		TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
ADC count value		$E_e = 0$	Ch0			1	counts
			Ch1			1	
		$\lambda_p = 640\ nm$ $E_e = 77\ \mu W/cm^2$	Ch0	639	799	959	
			Ch1		85		
		$\lambda_p = 940\ nm$ $E_e = 150\ \mu W/cm^2$	Ch0	511	799	1039	
			Ch1		703		
ADC count value ratio: Ch1/Ch0		$\lambda_p = 640\ nm, E_e = 77\ \mu W/cm^2$		0.070	0.106	0.175	
		$\lambda_p = 940\ nm, E_e = 150\ \mu W/cm^2$		0.70	0.88	1.20	
R_e	Irradiance responsivity	$\lambda_p = 640\ nm$ $E_e = 77\ \mu W/cm^2$	Ch0		10.4		counts/ ($\mu W/cm^2$)
			Ch1		1.1		
		$\lambda_p = 940\ nm$ $E_e = 150\ \mu W/cm^2$	Ch0		5.3		
			Ch1		4.7		
R_v	Illuminance responsivity	Fluorescent light source: 300 Lux	Ch0		2.8		counts/ lux
			Ch1		0.23		
		Incandescent light source: 50 Lux	Ch0		19		
			Ch1		13		
(Sensor Lux) / (actual Lux) (Note 5)		Fluorescent light source: 300 Lux		0.65	1	1.35	
		Incandescent light source: 50 Lux		0.5	1	1.5	

NOTES: 2. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 640 nm LEDs and infrared 940 nm LEDs are used for final product testing for compatibility with high volume production.

3. The 640 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following characteristics: peak wavelength $\lambda p = 640$ nm and spectral halfwidth $\Delta\lambda\frac{1}{2} = 17$ nm.

4. The 940 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following characteristics: peak wavelength $\lambda p = 940$ nm and spectral halfwidth $\Delta\lambda\frac{1}{2} = 40$ nm.

5. The sensor Lux is calculated using the empirical formula shown on p. 12 of this data sheet based on measured Ch0 and Ch1 ADC count values for the light source specified. Actual Lux is obtained with a commercial luxmeter. The range of the (sensor Lux) / (actual Lux) ratio is estimated based on the variation of the 640 nm and 940 nm optical parameters. Devices are not 100% tested with fluorescent or incandescent light sources.

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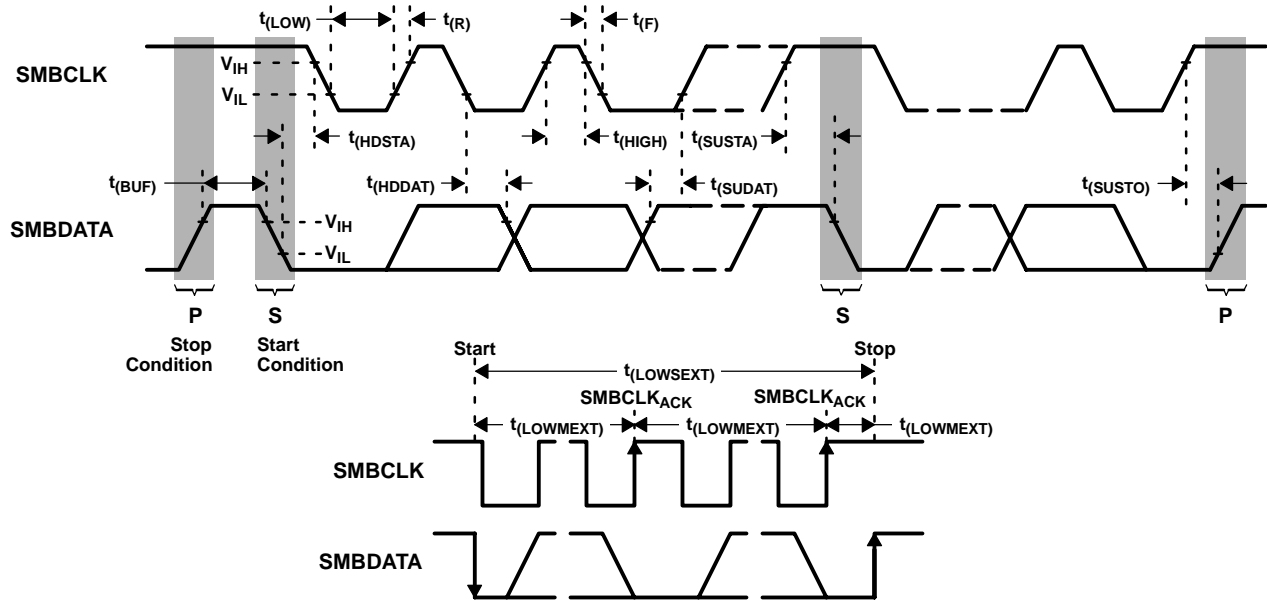Copyright © 2003, TAOS Inc.
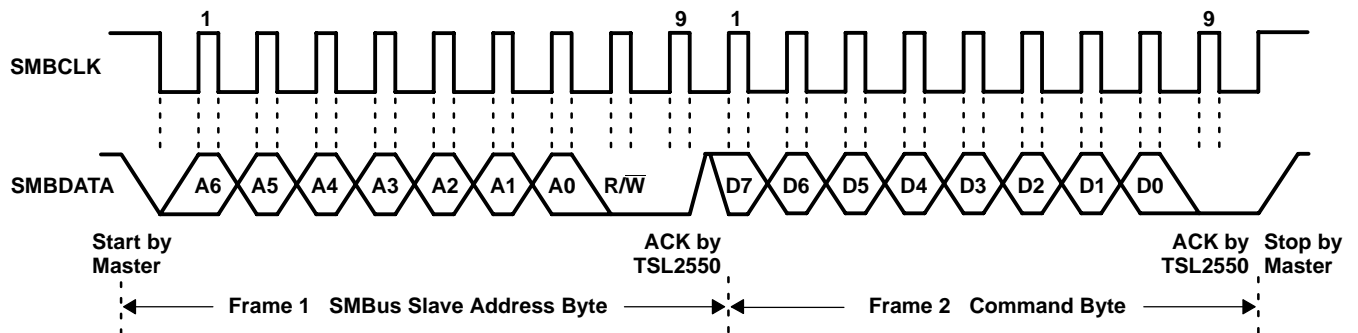
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AC Electrical Characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CONV)}$	Conversion time, per channel			400		ms
$f_{(SMBCLK)}$	Clock frequency				100	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		4.7			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		4			µs
$t_{(SUSTA)}$	Repeated start condition setup time		4.7			µs
$t_{(SUSTO)}$	Stop condition setup time		4			µs
$t_{(HDDAT)}$	Data hold time		300			ns
$t_{(SUDAT)}$	Data setup time		250			ns
$t_{(LOW)}$	SMBCLK clock low period		4.7			µs
$t_{(HIGH)}$	SMBCLK clock high period		4			µs
$t_{(TIMEOUT)}$	Detect clock/data low timeout		25		35	ms
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				1000	ns
C_i	Input pin capacitance				10	pF

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PARAMETER MEASUREMENT INFORMATION

Figure 1. SMBus Timing Diagrams

Figure 2. SMBus Timing Diagram for Send Byte Format
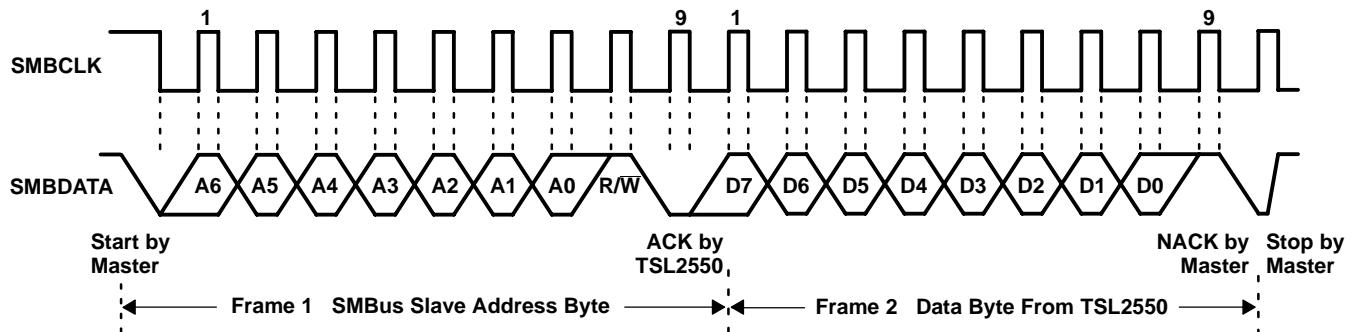
Figure 3. SMBus Timing Diagram for Receive Byte Format

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TYPICAL CHARACTERISTICS

SPECTRAL RESPONSIVITY

Figure 4

NORMALIZED ADC OUTPUT
vs.
SUPPLY VOLTAGE

Figure 5

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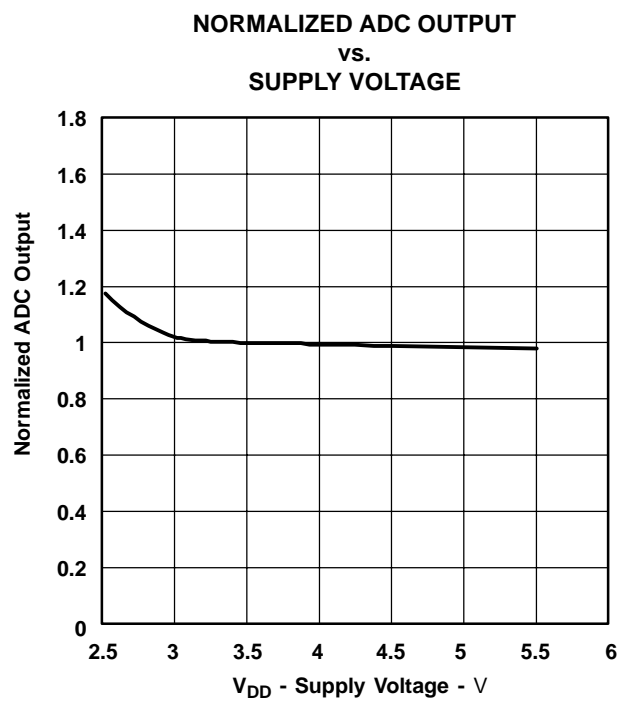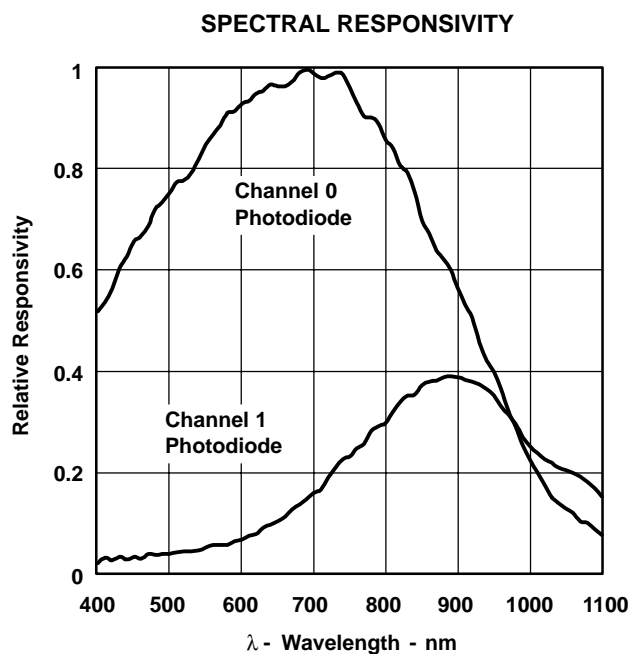
PRINCIPLES OF OPERATION

Analog-to-Digital Converter

The TSL2550 contains an integrating analog-to-digital converter (ADC) that integrates a photodiode current. First it integrates channel 0 photodiode current and then it integrates channel 1 photodiode current. At the end of the conversion cycle for each channel (approximately 400 ms), the conversion result is transferred to the appropriate channel 0 or channel 1 ADC register. The transfer is double-buffered to ensure that invalid data is not read during the transfer. After the data is transferred, the TSL2550 automatically begins the next conversion cycle. Approximately 800 ms is required for both Channel 0 and Channel 1 ADC registers to be updated. A VALID bit is used to indicate that data has been written to the ADC register after ADC is enabled.

Interface to the ADC and control of other device functions is accomplished using the standard 2-wire System Management Bus (SMBus) interface. Both versions 1.1 and 2.0 of the SMBus are supported.

Digital Interface

The TSL2550 contains an 8-bit command register that can be written and read via the SMBus. The command register controls the overall operation of the device. There are two read-only registers that contain the latest converted value of each of the two ADC channels. The SMBus slave address is hardwired internally as 0111001 (MSB to LSB, A6 to A0).

Both the *send byte protocol* and the *receive byte protocol* are implemented in the TSL2550. The send byte protocol allows single bytes of data to be written to the device (see Figure 6). The written byte is called the COMMAND byte. The receive byte protocol allows single bytes of data to be read from the device (see Figure 7). The receive data can be either the previously written COMMAND byte or the data from one of the ADC channels. In Figure 6 and Figure 7, the clear area represents data sent by the host and the shaded area represents data returned by the ambient light sensor or slave device.

1	7	1	1	8	1	1
S	Slave Address	WR	A	Data Byte	A	P
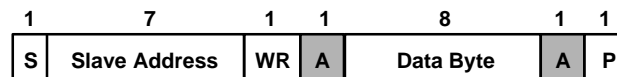
S = Start Condition   P = Stop Condition   Shaded = Slave Transmission

Figure 6. Send Byte Protocol

1	7	1	1	8	1	1
S	Slave Address	RD	A	Data Byte	A	P

S = Start Condition   P = Stop Condition   Shaded = Slave Transmission

Figure 7. Receive Byte Protocol

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Command Register

The command register contains eight bits as described in Table 1 and defaults to 0 (0x00) at power-up. A command summary appears in Table 2.

Table 1. Command Register Data Format

RSEL			RESERVED			ADCEN	PON
B7	B6	B5	B4	B3	B2	B1	B0
RSEL2	RSEL1	RSEL0	0	0	0	ADCEN	PON

FIELD	BITS	DESCRIPTION
RSEL	7 to 5	Read Data Select. This field determines the data output by the TSL2550 during read. **Field Value** **Read Value** 000 Command register 010 ADC channel 0 100 ADC channel 1
RESERVED	4 to 2	Reserved for factory test. These bits should always be written to 0.
ADCEN	1	ADC Enable. This field actives the ADC. Writing a 1 activates the ADC. Writing a 0 disables the ADC. ADCEN is normally used in conjunction with PON. *Note: Both ADCEN and PON must be asserted before the ADC channels will operate correctly.*
PON	0	Power ON. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. PON is normally used in conjunction with ADCEN. *Note: For the Duration of writes and reads over the SMB interface, this bit is overridden and the oscillator is enabled, independent of the state of PON.* *Note: Both ADCEN and PON must be asserted before the ADC channels will operate correctly.*

The command register is used primarily to select which register will be read during a read cycle (RSEL) and to control the power consumption of the device (ADCEN and PON). When ADCEN and PON are high, the device is in the full powered-up state and is fully operational. When ADCEN and PON are low, both the ADC and the internal oscillator are powered down, resulting in minimum power consumption. *Both ADCEN and PON should always be asserted and de-asserted together*. The remaining bits (B4, B3, and B2) in the command register should always be written 0. For details on using the command register, see the *Operation* section, below.

Table 2. Command Summary

COMMAND	FUNCTION
00h	Place device in power-down state
03h	Read command register
43h	Read ADC Channel 0
83h	Read ADC Channel 1

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ADC Register

The TSL2550 contains two ADC registers (channel 0 and channel 1). Each ADC register contains two components to determine the logarithmic ADC count value: CHORD bits and STEP bits. The CHORD bits correspond to the most significant portion of the ADC value and specifies a segment of the piece-wise linear approximation. The STEP bits correspond to the least significant portion of the ADC count value and specifies a linear value within a segment. CHORD and STEP bits all equal to 0 corresponds to a condition in which the light level is below the detection limit of the sensor. CHORD and STEP bits all equal to 1 corresponds to an overflow condition.

Each of the two ADC value registers contain seven bits as described in Table 3. The specific ADC value register read depends on the last written RSEL field to the command register, as described above and in the *Operation* section, below.

Table 3. ADC Register Data Format

VALID	CHORD BITS			STEP BITS			
B7	B6	B5	B4	B3	B2	B1	B0
VALID	C2	C1	C0	S3	S2	S1	S0

FIELD	BITS	DESCRIPTION
VALID	7	ADC channel data is valid. One indicates that the ADC has written data into the channel data register, since ADCEN was asserted in the COMMAND register.
CHORD	6 to 4	CHORD number.
STEP	3 to 0	STEP number.

The MSB of the ADC register (VALID bit B7) is used to indicate that data has been written to the ADC register after the ADC and internal oscillator are activated as described in *Command Register* section.

Bits 6 through 0 contain the 7-bit code representing the ADC count value, which is proportional to a photodetector current. In this code, the ADC count value is represented by a piece-wise linear approximation to a log function. The transfer function is broken into 8 chords of 16 steps each. (This code is very similar to μ-law code used in audio compression — it differs in that it does not have a sign bit and it is not inverted.) Table 4 shows the relationship between the CHORD and STEP bits and the CHORD and STEP numbers and values. These are used to calculate the ADC count value.

Table 4. CHORD and STEP Numbers and Values vs Register Bits

CHORD BITS B6, B5, B4	C, CHORD NUMBER	CHORD VALUE (Note A)	STEP VALUE (Note B)
000	0	0	1
001	1	16	2
010	2	49	4
011	3	115	8
100	4	247	16
101	5	511	32
110	6	1039	64
111	7	2095	128

STEP BITS B3, B2, B1, B0	S, STEP NUMBER
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

NOTES: A. CHORD VALUE $= \text{INT} (16.5 \times ((2^C) - 1))$
B. STEP VALUE $= 2^C$

The ADC count value is obtained by adding the CHORD VALUE and the product of the STEP NUMBER and STEP VALUE (which depends on CHORD NUMBER).

$$\text{ADC Count Value} = ((\text{Chord Value}) + (\text{Step Size}) \times (\text{Number of Steps}))$$

The ADC count value is as a formula:

$$\text{ADC Count Value} = (\text{INT} (16.5 \times ((2^c - 1))) + (S \times (2^c))$$

where:

C   is the CHORD NUMBER (0 to 7)
S   is the STEP NUMBER (0 to 15)
as defined in Table 4.

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Operation

After applying VDD, the device will initially be in the power down state. To operate the device, issue an SMBus Send Byte protocol with the device address and the appropriate command byte to read ADC channel 0 or ADC channel 1 (see Table 2). To obtain the conversion result, issue an SMBus Receive Byte protocol with the device address. The data byte received will correspond to the value in the ADC register (0 or 1) specified by the previous command. If a conversion has not been completed since power up (either through V_{DD} or ADCEN/PON), the valid bit will be 0, and the data will not be valid. If there is a valid conversion result available, the valid bit will be set (1), and the remaining 7 bits will represent valid data from the previously selected ADC register. Data may be read repeatedly from the currently selected ADC register, and although it will remain valid, the ADC register will not be updated until a new conversion completes for that channel (800 ms total since there are two serial 400 ms per channel conversion times). Note also that the command register itself may be read, as a check to be sure that the device is communicating properly.

To power down the device for reduced power consumption, issue an SMBus Send Byte protocol with the device address followed by 0 to clear the ADCEN and PON bits.

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APPLICATION INFORMATION

The TSL2550 is intended for use in ambient light detection applications, such as display backlight control, where adjustments are made to display brightness or contrast based on the brightness of the ambient light, as perceived by the human eye. Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high, such as with incandescent lighting, due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome in the TSL2550 through the use of two photodiodes. One of the photodiodes (Channel 0) is sensitive to both visible and infrared light, while the second photodiode (Channel 1) is sensitive primarily to infrared light. An integrating ADC converts the photodiode currents to Channel 0 and Channel 1 digital outputs. Channel 1 digital output is used to compensate for the effect of the infrared component of light on the Channel 0 digital output. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in the commonly used Illuminance unit of Lux:

$$\text{Light Level (lux)} = (\text{Ch0 Counts}) \times (0.46) \times (e^{(-3.13R)})$$

where:

$$R = (\text{Ch1 Counts}) / (\text{Ch0 Counts})$$

The formula above was obtained by optical testing with fluorescent and incandescent light sources. The light level calculated from the formula will be slightly higher than the actual light level for sunlight and will be slightly lower than the actual light level for composite fluorescent and incandescent light sources.

Table 5 contains a summary of the typical sensor outputs for several common light sources.

Table 5. Sensor Output Summary

LIGHT SOURCE	ILLUMINANCE (LUX)	CHANNEL 0 (COUNTS)	CHANNEL 1 (COUNTS)	RATIO: CH1/CH0	LUX per CH0 COUNT
Fluorescent	300	831	68	0.082	0.36
Daylight (shade)	100	895	343	0.38	0.11
Incandescent	50	959	671	0.7	0.052

Light from 50 or 60 Hz sources, and especially fluorescent lighting, has a high harmonic content. Since the TSL2550 integrates the ambient light over an approximately 400 millisecond interval (per channel), this light ripple is typically reduced to less than ¼ LSB.

Power Supply Decoupling

The power supply lines must be decoupled with a 0.1 μF capacitor placed as close to the device package as possible. The bypass capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

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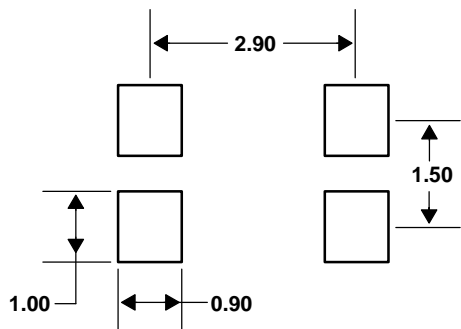SOLUTIONS™

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APPLICATION INFORMATION

PCB Pad Layout

Suggested PCB pad layout guidelines for the D package and T package are shown in Figure 8 and Figure 9.
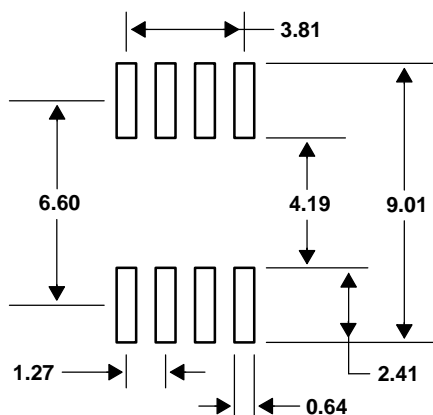
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Figure 8. Suggested D Package PCB Layout

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
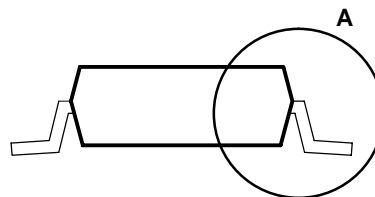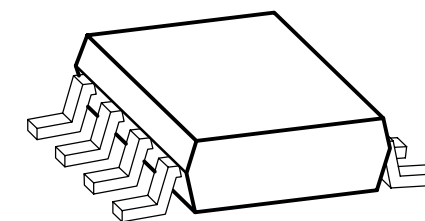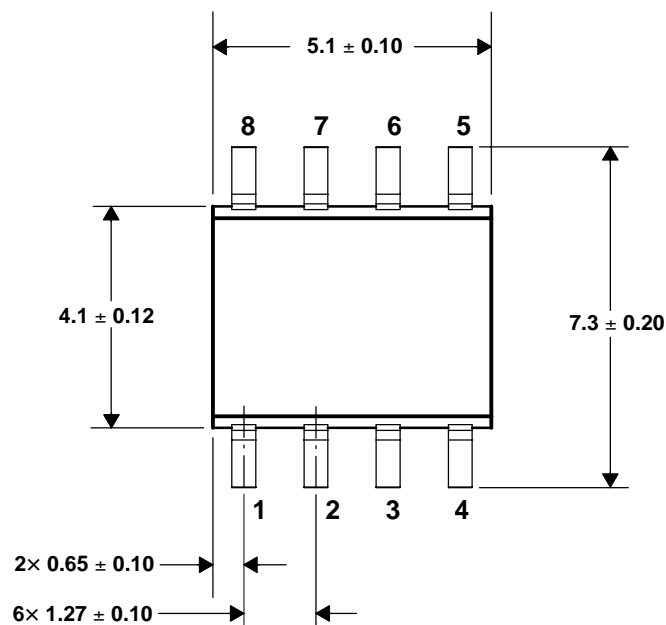
Figure 9. Suggested T Package PCB Layout

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MECHANICAL DATA

PACKAGE D   **PLASTIC SMALL-OUTLINE**

DETAIL A
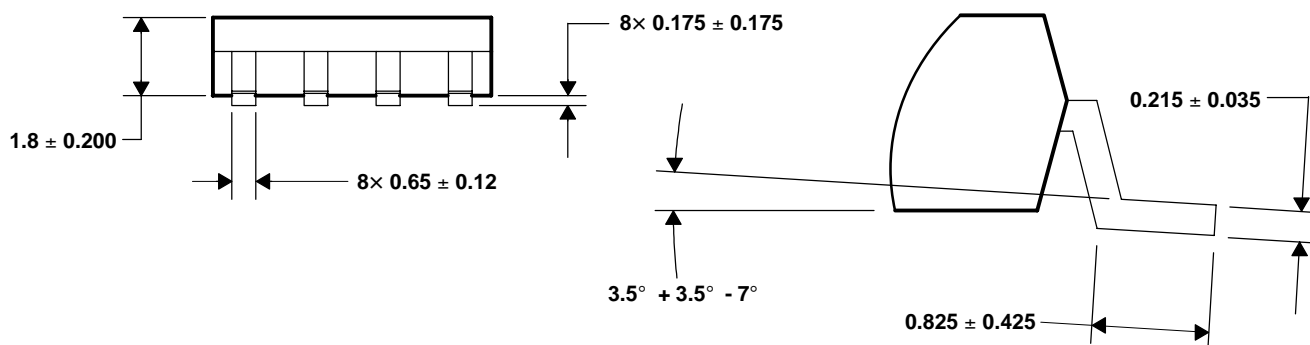
NOTES: A. All linear dimensions are in millimeters.
           B. Package is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
           C. Actual product will vary within the mechanical tolerances shown on this specification. Designs for use of this product MUST allow
               for the data sheet tolerances.
           D. This drawing is subject to change without notice.

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MECHANICAL DATA

PACKAGE T   **Four-Lead Surface Mount Device**

BOTTOM VIEW

A

PIN 1

2.60

3.80

PIN 1

PIN 4

SIDE VIEW

0.50

1.35

0.35

3.10

2 × 7°
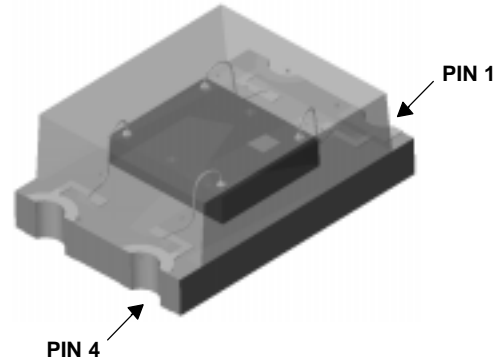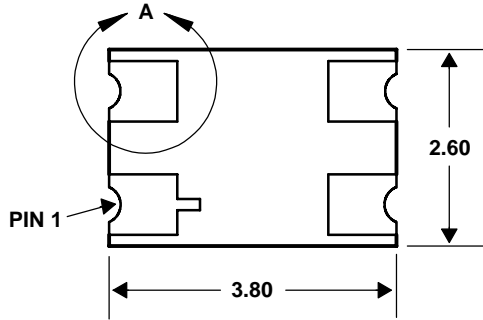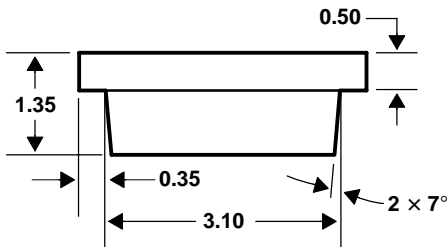
PHOTODIODE ACTIVE AREA LOCATION

1.46

0.28

0.67

1.23

TOP VIEW

1.50

0.55
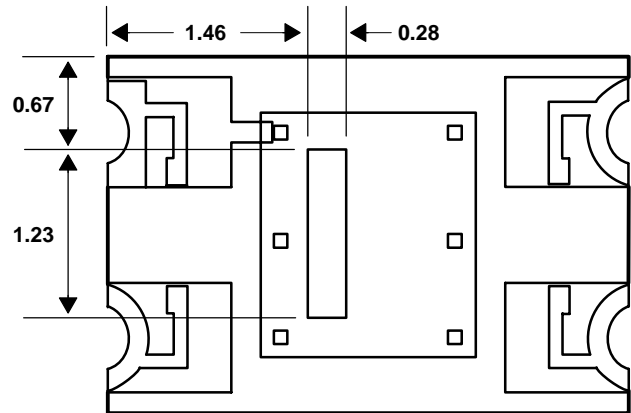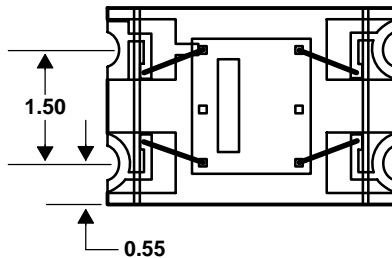
DETAIL A: TYPICAL PACKAGE TERMINAL

0.10

0.90

0.78

0.78

R 0.25
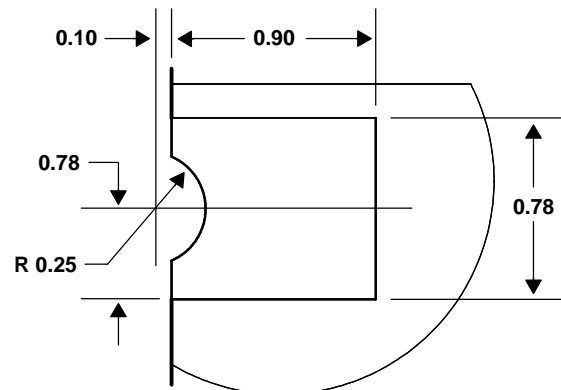
NOTES: A. All linear dimensions are in millimeters.
        B. Terminal finish is gold.
        C. Dimension tolerance is ± 0.15 mm.
        D. This drawing is subject to change without notice.

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NOTICE