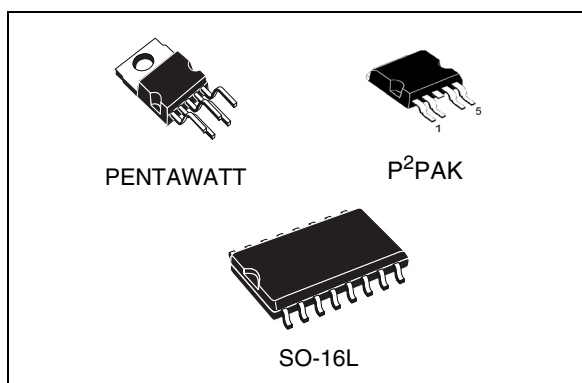


Single channel high-side solid-state relay

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920 VN920-B5 VN920SO	16 mΩ	30 A	36 V

- CMOS compatible input
- Proportional load current sense
- Shorted load protection
- Under-voltage and over-voltage shutdown
- Over-voltage clamp
- Thermal shutdown
- Current limitation
- Protection against loss of ground and loss of V_{CC}
- Very low standby power dissipation
- Reverse battery protected (see [Application schematic](#))



Description

The VN920 is a monolithic device designed in STMicroelectronics VIPower M0-3 technology. The VN920 is intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against over-load.

The device integrates an analog current sense output which delivers a current proportional to the load current. The device automatically turns off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PENTAWATT	VN920	-
P²PAK	VN920-B5	VN920-B513TR
SO-16L	VN920SO	VN920SO13TR

Contents

1	Block diagram and pin description	5
2	Electrical specifications	6
2.1	Absolute maximum ratings	6
2.2	Thermal data	7
2.3	Electrical characteristics	8
2.4	Electrical characteristics curves	14
3	Application information	16
3.1	GND protection network against reverse battery	16
3.1.1	Solution 1: resistor in the ground line (RGND only)	16
3.1.2	Solution 2: diode (DGND) in the ground line	17
3.2	Load dump protection	17
3.3	MCU I/Os protection	17
3.4	P ² PAK maximum demagnetization energy (VCC = 13.5V)	18
3.5	SO-16L maximum demagnetization energy (VCC = 13.5V)	19
4	Package and PCB thermal data	20
4.1	SO-16L thermal data	20
4.2	P ² PAK thermal data	22
5	Package and packing information	25
5.1	ECOPACK [®] packages	25
5.2	PENTAWATT mechanical data	26
5.3	P ² PAK mechanical data	28
5.4	SO-16L packing information	30
5.5	PENTAWATT packing information	31
5.6	P ² PAK packing information	31
6	Revision history	33

List of tables

Table 1.	Device summary	1
Table 2.	Suggested connections for unused and not connected pins	5
Table 3.	Absolute maximum ratings	6
Table 4.	Thermal data.	7
Table 5.	Power	8
Table 6.	Switching ($V_{CC}=13V$)	8
Table 7.	Logic inputs.	9
Table 8.	Current sense ($9V \leq V_{CC} \leq 16V$)	9
Table 9.	V_{CC} output diode.	10
Table 10.	Protections	10
Table 11.	Truth table.	11
Table 12.	Electrical transient requirements	11
Table 13.	SO-16L thermal parameters	22
Table 14.	P ² PAK thermal parameter	24
Table 15.	SO-16L mechanical data	25
Table 16.	PENTAWATT mechanical data	27
Table 17.	P ² PAK mechanical data	29
Table 18.	Document revision history	33

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	5
Figure 3.	Current and voltage conventions	6
Figure 4.	Switching characteristics	12
Figure 5.	I_{OUT}/I_{SENSE} versus I_{OUT}	12
Figure 6.	Waveforms	13
Figure 7.	Off-state output current	14
Figure 8.	High-level input current	14
Figure 9.	Input clamp voltage	14
Figure 10.	Turn-on voltage slope	14
Figure 11.	Over-voltage shutdown	14
Figure 12.	Turn-off voltage slope	14
Figure 13.	ILIM vs Tcase	15
Figure 14.	On-state resistance vs VCC	15
Figure 15.	Input high-level	15
Figure 16.	Input hysteresis voltage	15
Figure 17.	On-state resistance vs Tcase	15
Figure 18.	Input low level	15
Figure 19.	Application schematic	16
Figure 20.	P ² PAK maximum turn-off current versus inductance	18
Figure 21.	SO-16L maximum turn-off current versus inductance	19
Figure 22.	SO-16L PC board	20
Figure 23.	SO-16L Rthj-amb Vs PCB copper area in open box free air condition	20
Figure 24.	SO-16L thermal impedance junction ambient single pulse	21
Figure 25.	Thermal fitting model of a single channel HSD in SO-16L	21
Figure 26.	P ² PAK PC board	22
Figure 27.	P ² PAK Rthj-amb Vs. PCB copper area in open box free air condition	23
Figure 28.	P ² PAK thermal impedance junction ambient single pulse	23
Figure 29.	Thermal fitting model of a single channel HSD in P ² PAK	24
Figure 30.	SO-16L package dimensions	25
Figure 31.	PENTAWATT package dimensions	26
Figure 32.	P ² PAK package dimensions	28
Figure 33.	SO-16L tube shipment (no suffix)	30
Figure 34.	SO-16L tape and reel shipment (suffix "TR")	30
Figure 35.	PENTAWATT tube shipment (no suffix)	31
Figure 36.	P ² PAK tube shipment (no suffix)	31
Figure 37.	P ² PAK tape and reel (suffix "13TR")	32

1 Block diagram and pin description

Figure 1. Block diagram

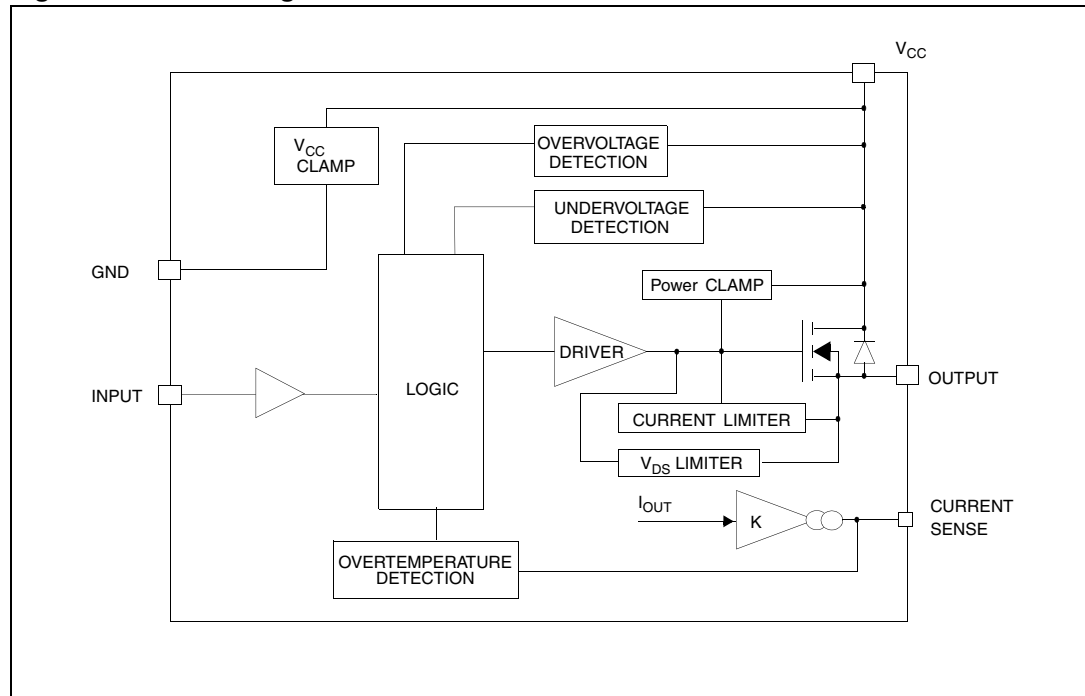


Figure 2. Configuration diagram (top view)

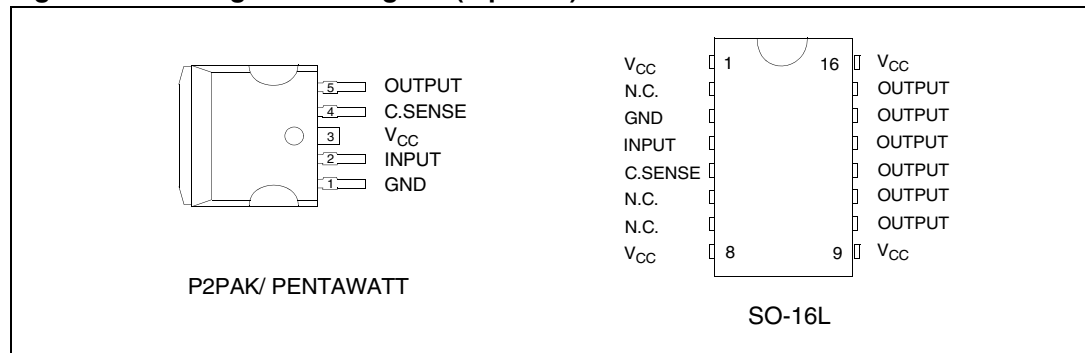
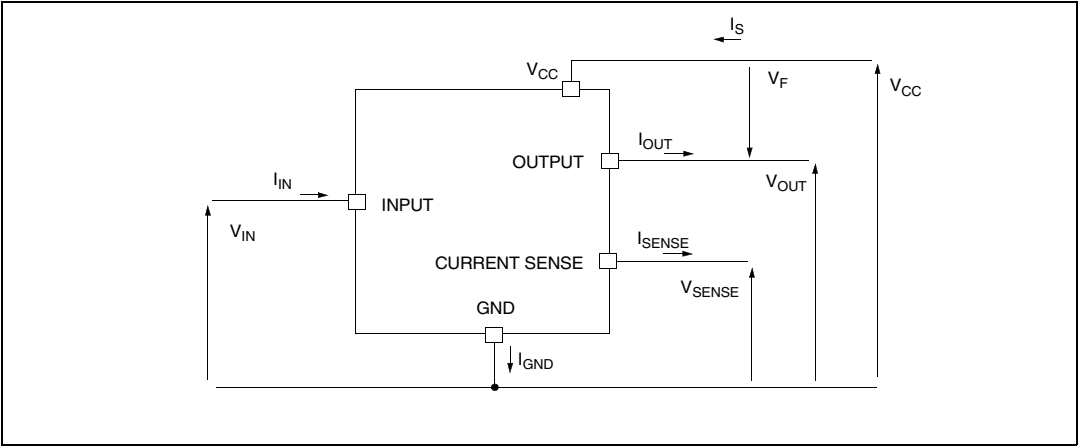


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1K Ω resistor	X		Through 10K Ω resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		SO-16L	PENTAWATT	P ² PAK	
V_{CC}	DC supply voltage	41			V
$-V_{CC}$	Reverse DC supply voltage	- 0.3			V
$-I_{gnd}$	DC reverse ground pin current	- 200			mA
I_{OUT}	DC output current	Internally limited			A
$-I_{OUT}$	Reverse DC output current	- 21			A
I_{IN}	DC input current	+/- 10			mA
V_{CSENSE}	Current sense maximum voltage	- 3 + 15			V V
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5K\Omega$ $C = 100pF$)				
	INPUT	4000			V
	CURRENT SENSE	2000			V
	OUTPUT	5000			V
	V_{CC}	5000			V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value			Unit
		SO-16L	PENTAWATT	P ² PAK	
E_{MAX}	Maximum switching energy ($L = 0.25\text{mH}$; $R_L = 0\Omega$; $V_{bat} = 13.5\text{V}$; $T_{jstart} = 150^\circ\text{C}$; $I_L = 45\text{A}$)	352		364	mJ
P_{tot}	Power dissipation $T_C \leq 25^\circ\text{C}$	8.3	96.1	96.1	W
T_j	Junction operating temperature	Internally limited			$^\circ\text{C}$
T_C	Case operating temperature	- 40 to 150			$^\circ\text{C}$
T_{stg}	Storage temperature	- 55 to 150			$^\circ\text{C}$

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value			Unit
		SO-16L	PENTAWATT	P ² PAK	
$R_{thj-case}$	Thermalresistance junction-case	-	1.3	1.3	$^\circ\text{C/W}$
$R_{thj-lead}$	Thermalresistance junction-lead	15	-		$^\circ\text{C/W}$
$R_{thj-amb}$	Thermalresistance junction-ambient	65 ⁽¹⁾	61.3	51.3 ⁽²⁾	$^\circ\text{C/W}$
		48 ⁽³⁾		37 ⁽⁴⁾	$^\circ\text{C/W}$

1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick) connected to all VCC pins.
2. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick).
3. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35μm thick) connected to all VCC pins.
4. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35μm thick).

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Under-voltage shutdown		3	4	5.5	V
V_{OV}	Over-voltage shutdown		36			V
R_{ON}	On-state resistance	$I_{OUT} = 10A$; $T_j = 25^{\circ}C$; $I_{OUT} = 10A$; $I_{OUT} = 3A$; $V_{CC} = 6V$			16 32 55	$m\Omega$ $m\Omega$ $m\Omega$
V_{CLAMP}	Clamp voltage	$I_{CC} = 20mA$	41	48	55	V
I_S	Supply current	Off-state; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$		10	25	μA
		Off-state; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$; $T_j = 25^{\circ}C$		10	20	μA
		On-state; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$; $R_{SENSE} = 3.9 k\Omega$			5	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0V$; $V_{OUT} = 3.5V$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$			3	μA

Note: V_{CLAMP} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Switching ($V_{CC}=13V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 1.3\Omega$ (see Figure 4.)		50		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 1.3\Omega$ (see Figure 4.)		50		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 1.3\Omega$ (see Figure 4.)	See Figure 10.			V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 1.3\Omega$ (see Figure 4.)	See Figure 12.			V/ μs

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25V$	1			μA
V_{IH}	Input high-level voltage		3.25			V
I_{IH}	High-level input current	$V_{IN} = 3.25V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 - 0.7	8	V V

Table 8. Current sense ($9V \leq V_{CC} \leq 16V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	$I_{OUT} = 1A$; $V_{SENSE} = 0.5V$; $T_j = -40^\circ C \dots 150^\circ C$	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	$I_{OUT} = 1A$; $V_{SENSE} = 0.5V$; $T_j = -40^\circ C \dots 150^\circ C$	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT} = 10A$; $V_{SENSE} = 4V$; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current sense ratio drift	$I_{OUT} = 10A$; $V_{SENSE} = 4V$; $T_j = -40^\circ C \dots 150^\circ C$	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT} = 30A$; $V_{SENSE} = 4V$; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current sense ratio drift	$I_{OUT} = 30A$; $V_{SENSE} = 4V$; $T_j = -40^\circ C \dots 150^\circ C$	-6		+6	%
I_{SENSE0}	Analog sense current	$V_{CC} = 6 \dots 16V$; $I_{OUT} = 0A$; $V_{SENSE} = 0V$; $T_j = -40^\circ C \dots 150^\circ C$	0		10	μA
V_{SENSE}	Max analog sense output voltage	$V_{CC} = 5.5V$; $I_{OUT} = 5A$; $R_{SENSE} = 10k\Omega$ $V_{CC} > 8V$, $I_{OUT} = 10A$; $R_{SENSE} = 10k\Omega$	2 4			V V
V_{SENSEH}	Sense voltage in over-temperature condition	$V_{CC} = 13V$; $R_{SENSE} = 3.9k\Omega$		5.5		V

Table 8. Current sense ($9V \leq V_{CC} \leq 16V$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{VSENSEH}$	Analog sense output impedance in over-temperature condition	$V_{CC} = 13V$; $T_j > T_{TSD}$; output open		400		Ω
t_{DSENSE}	Current sense delay response	To 90% $I_{SENSE}^{(1)}$			500	μs

1. Current sense signal delay after positive input slope.

Table 9. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT} = 5A$; $T_j = 150^\circ C$			0.6	V

Table 10. Protections⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	$^\circ C$
T_R	Reset temperature		135			$^\circ C$
T_{hyst}	Thermal hysteresis		7	15		$^\circ C$
I_{lim}	Current limitation	$V_{CC} = 13V$ $5V < V_{CC} < 36V$	30	45	75 75	A A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 2 A$; $V_{IN} = 0V$; $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 1 A$; $T_j = -40^\circ C \dots 150^\circ C$		50		mV

1. To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Over-temperature	L H	L L	0 V_{SENSEH}
Under-voltage	L H	L L	0 0
Over-voltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 ($T_j < T_{TSD}$) 0 ($T_j > T_{TSD}$) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V ⁽¹⁾	- 50V ⁽¹⁾	- 75V ⁽¹⁾	- 100V ⁽¹⁾	2ms, 10Ω
2	+ 25V ⁽¹⁾	+ 50V ⁽¹⁾	+ 75V ⁽¹⁾	+ 100V ⁽¹⁾	0.2ms, 10Ω
3a	- 25V ⁽¹⁾	- 50V ⁽¹⁾	- 100V ⁽¹⁾	- 150V ⁽¹⁾	0.1μs, 50Ω
3b	+ 25V ⁽¹⁾	+ 50V ⁽¹⁾	+ 75V ⁽¹⁾	+ 100V ⁽¹⁾	0.1μs, 50Ω
4	- 4V ⁽¹⁾	- 5V ⁽¹⁾	- 6V ⁽¹⁾	- 7V ⁽¹⁾	100ms, 0.01Ω
5	+ 26.5V ⁽¹⁾	+ 46.5V ⁽²⁾	+ 66.5V ⁽²⁾	+ 86.5V ⁽²⁾	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 4. Switching characteristics

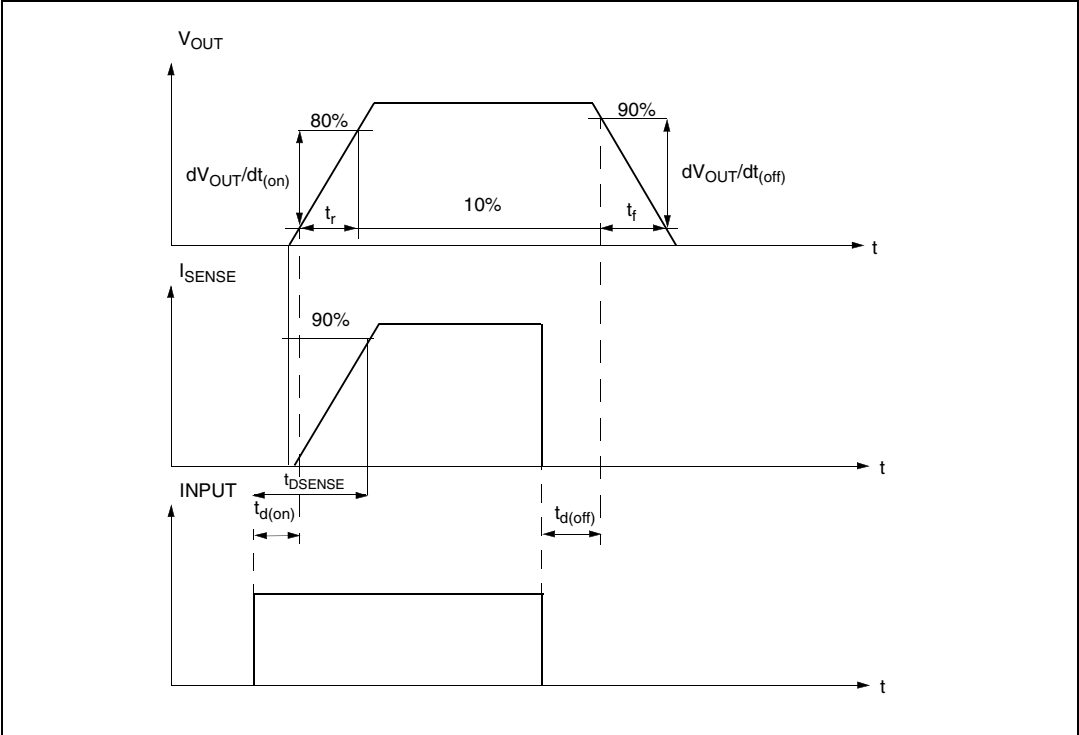


Figure 5. I_{OUT}/I_{SENSE} versus I_{OUT}

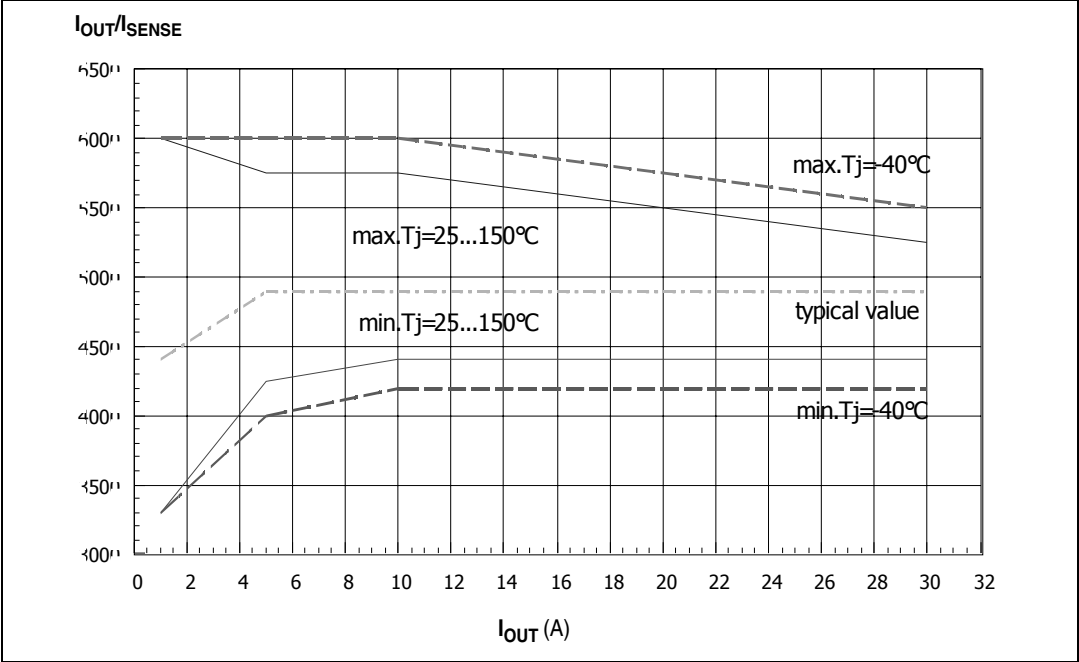
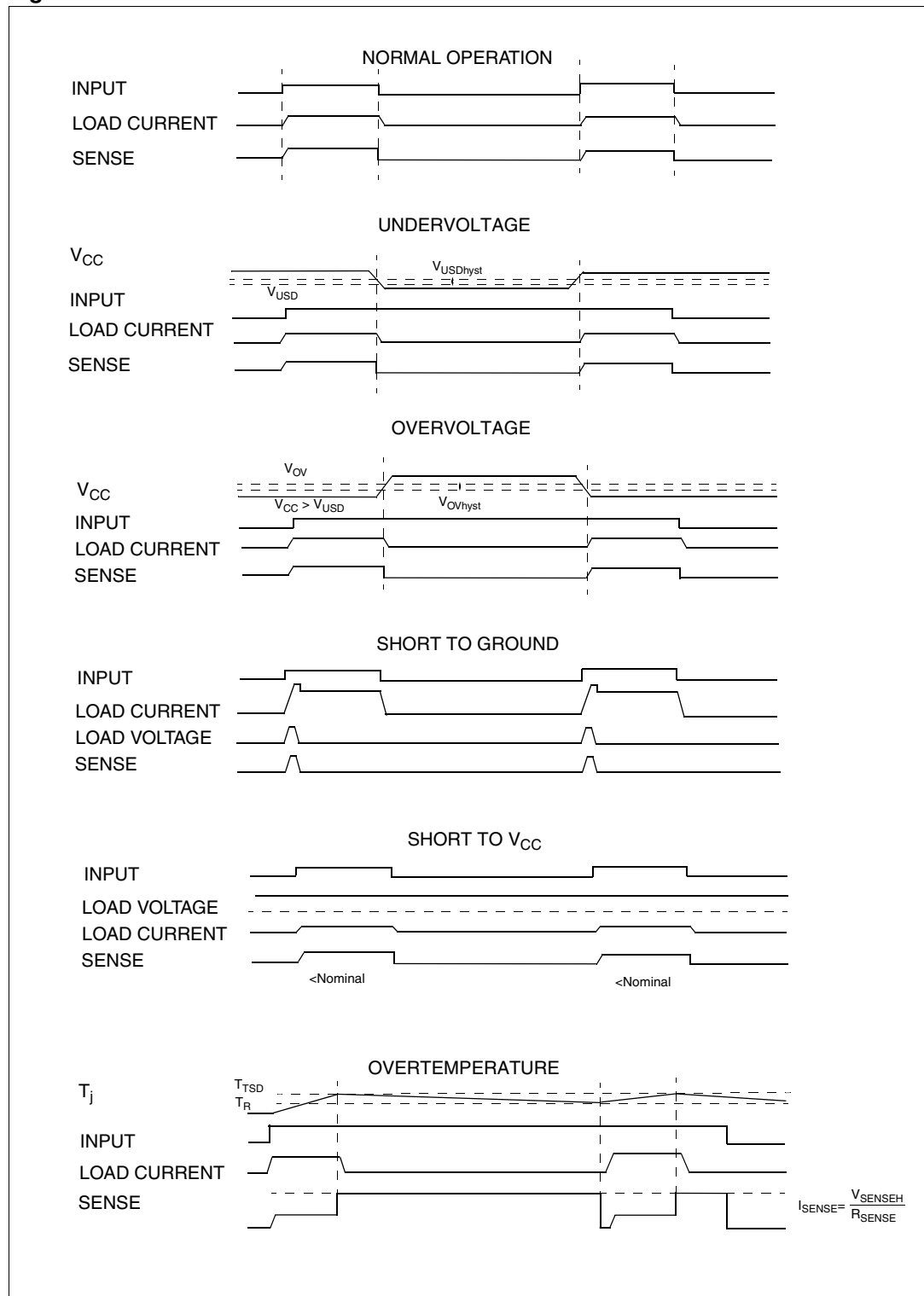


Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

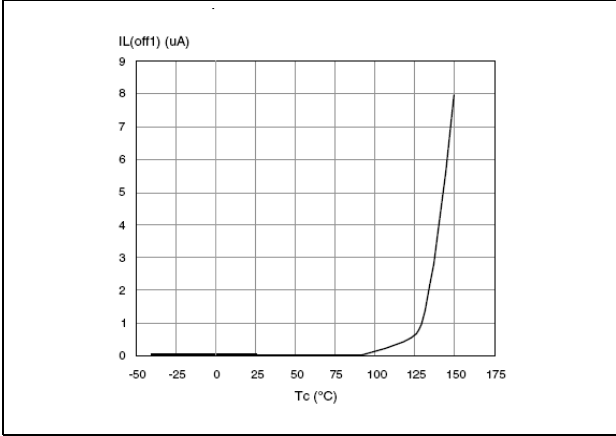


Figure 8. High-level input current

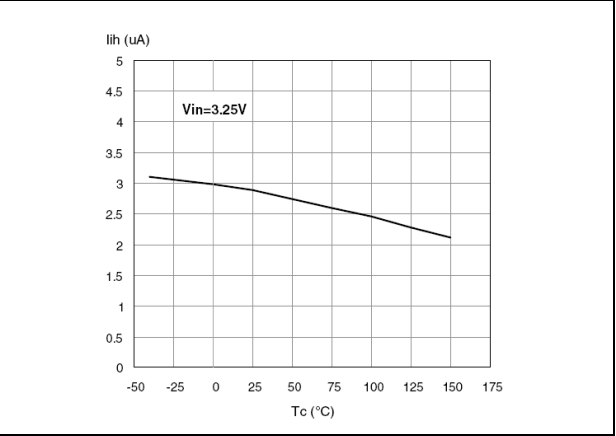


Figure 9. Input clamp voltage

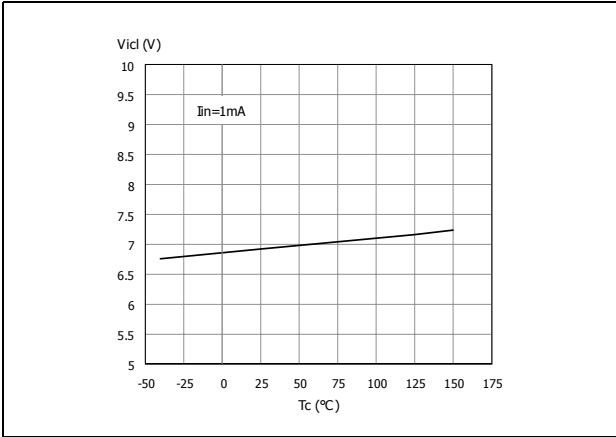


Figure 10. Turn-on voltage slope

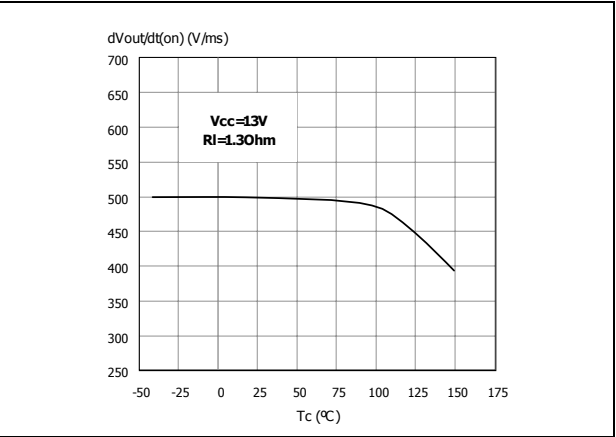


Figure 11. Over-voltage shutdown

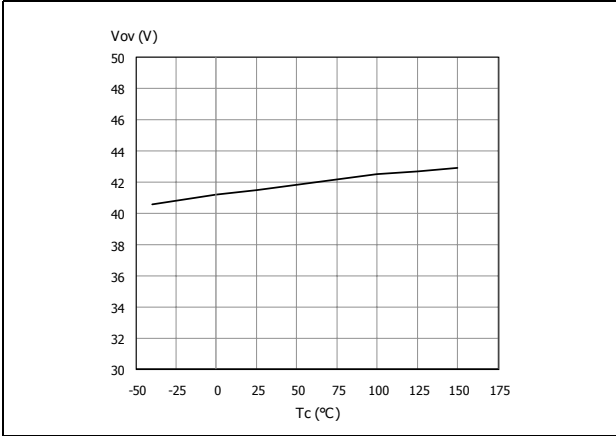


Figure 12. Turn-off voltage slope

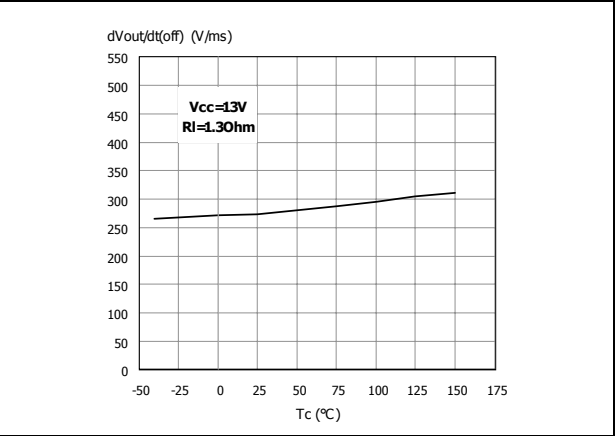


Figure 13. I_{LIM} vs T_{case}

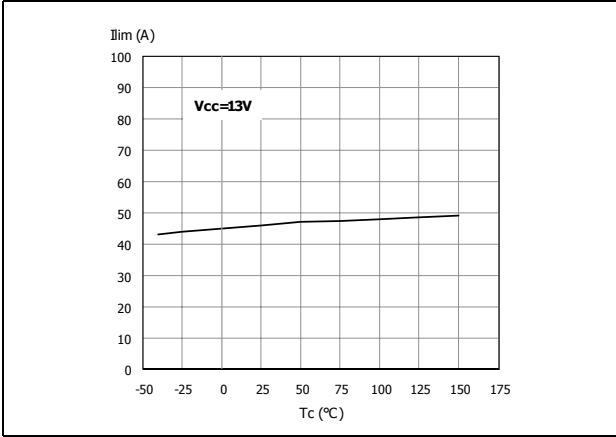


Figure 14. On-state resistance vs V_{CC}

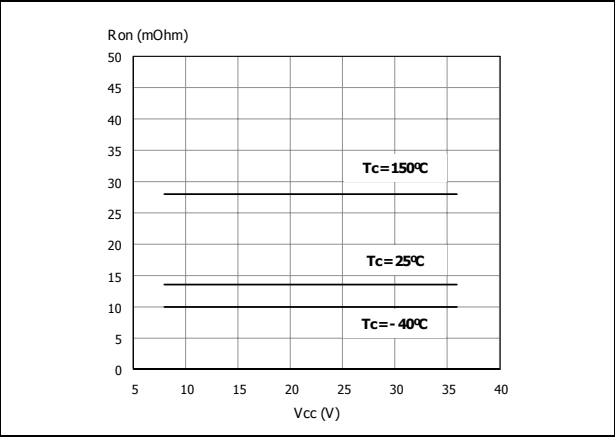


Figure 15. Input high-level

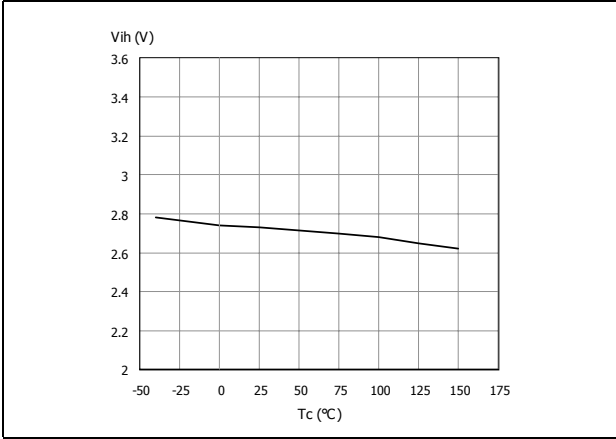


Figure 16. Input hysteresis voltage

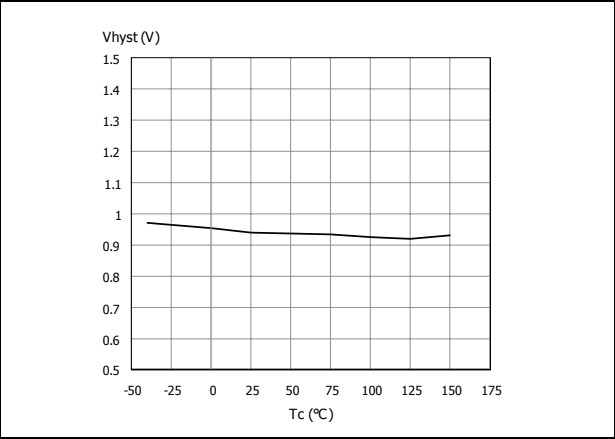


Figure 17. On-state resistance vs T_{case}

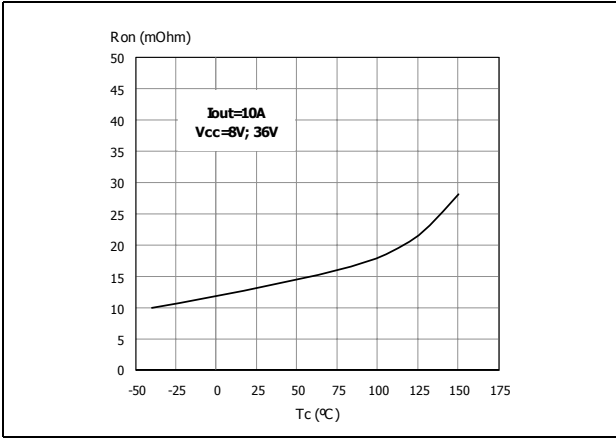
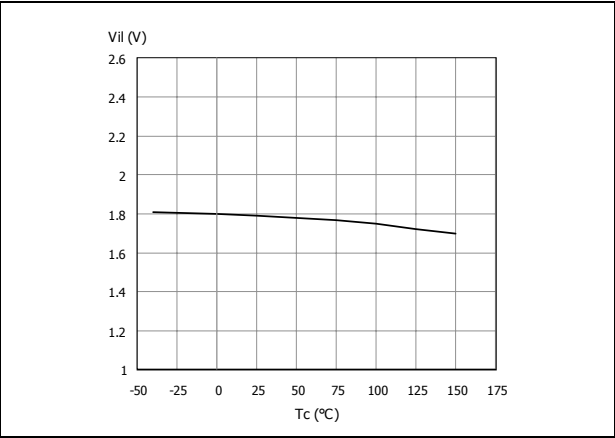


Figure 18. Input low level



3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

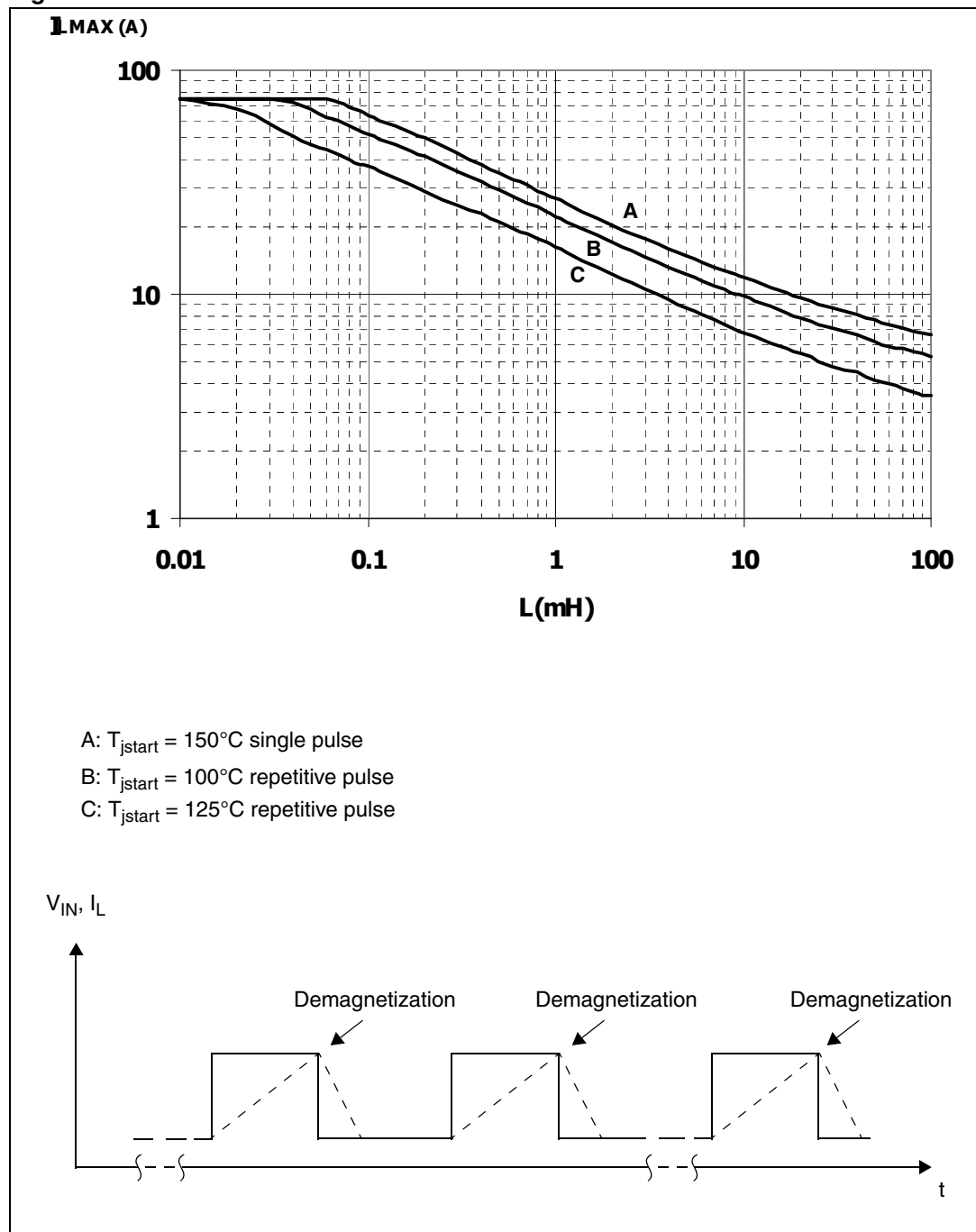
For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$.

3.4 P²PAK maximum demagnetization energy ($V_{CC} = 13.5V$)

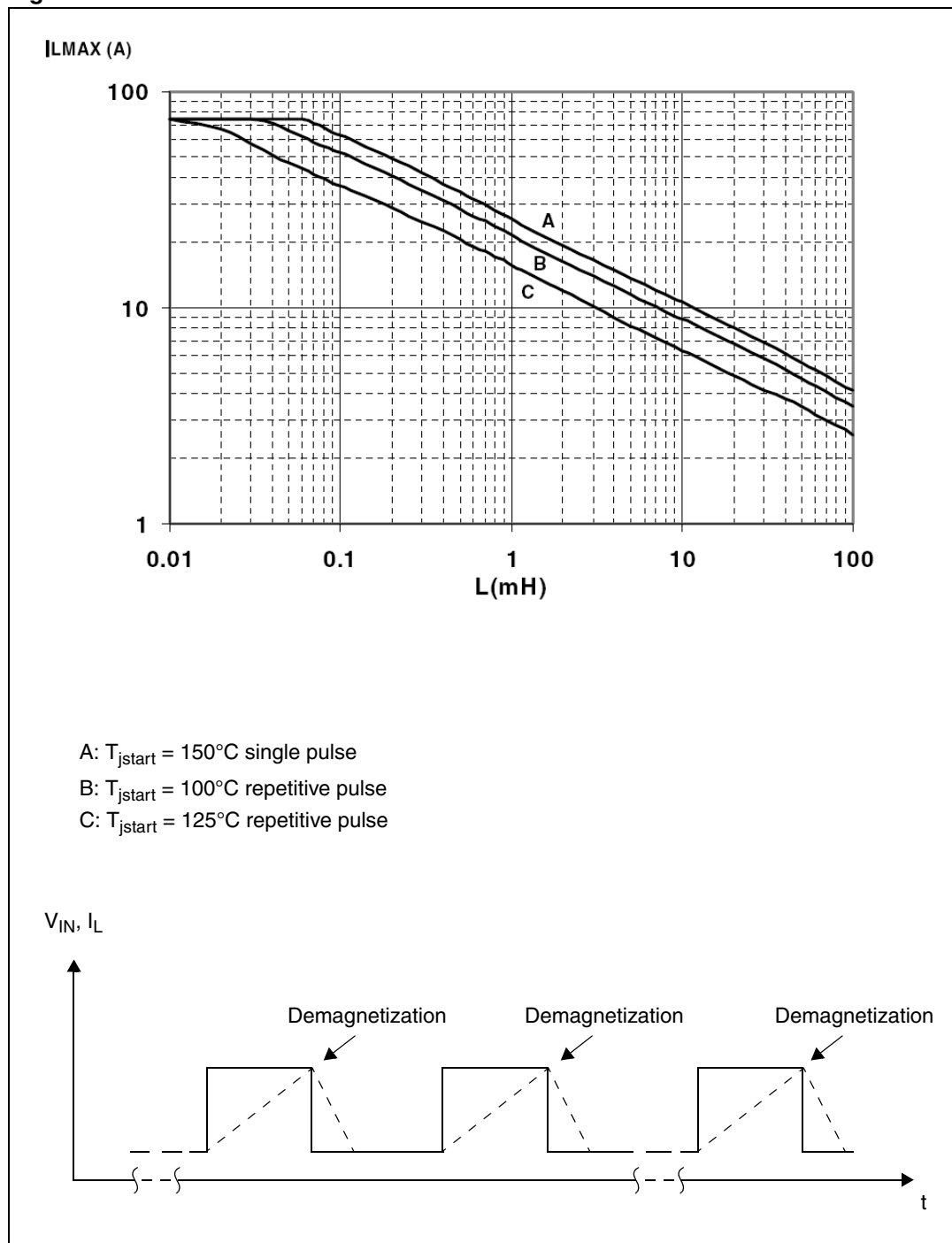
Figure 20. P²PAK maximum turn-off current versus inductance



Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3.5 SO-16L maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 21. SO-16L maximum turn-off current versus inductance

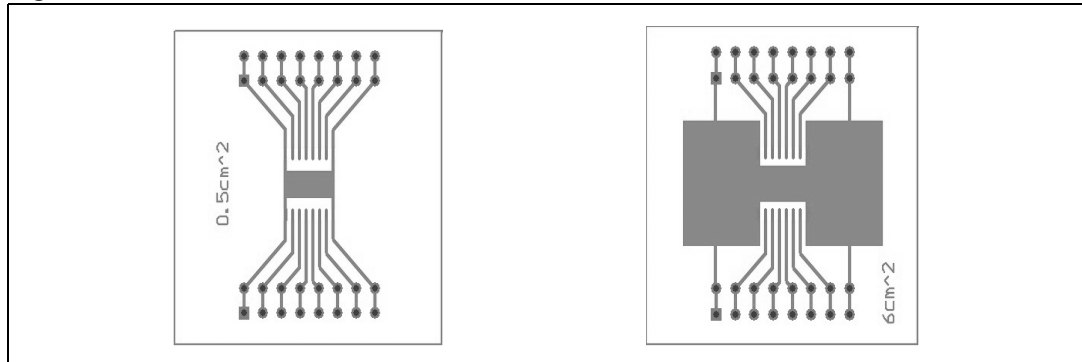


Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-16L thermal data

Figure 22. SO-16L PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 41mm x 48mm, PCB thickness = 2mm, Cu thickness = 35 μ m, Copper areas: 0.5cm², 6cm²).

Figure 23. SO-16L $R_{thj-amb}$ Vs PCB copper area in open box free air condition

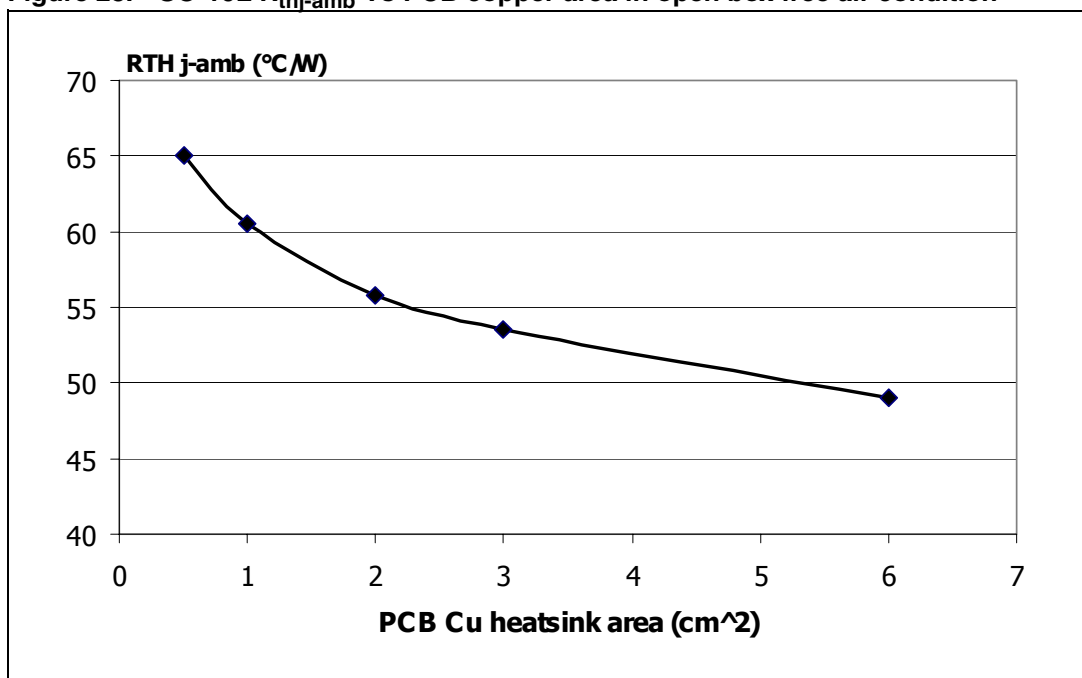
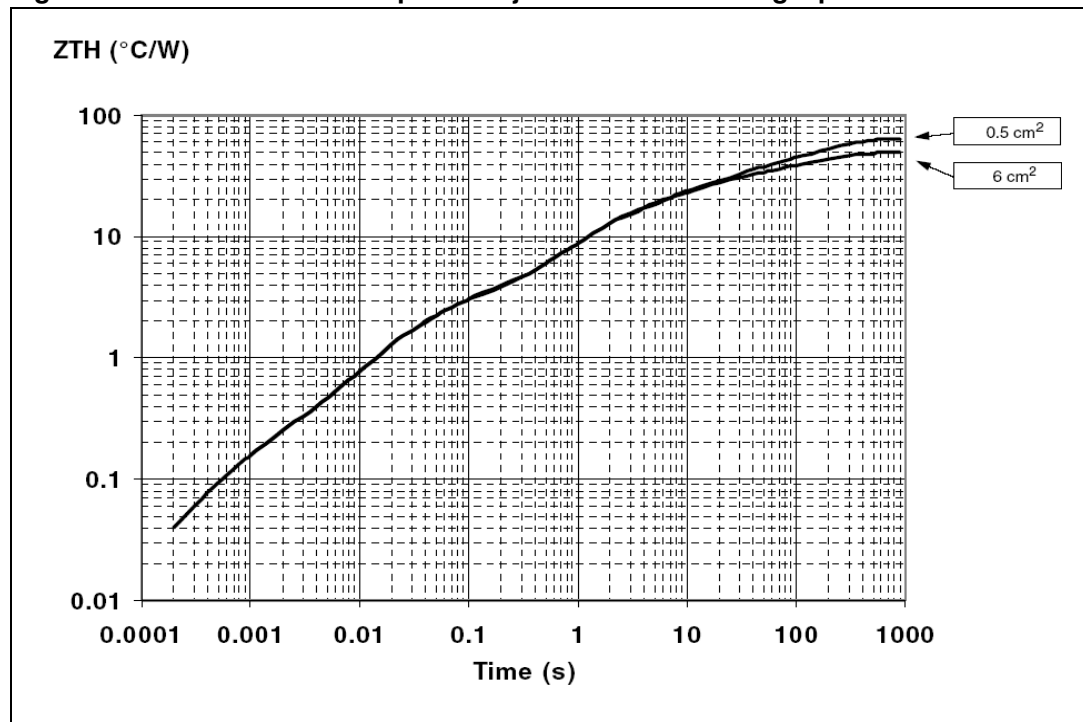


Figure 24. SO-16L thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Figure 25. Thermal fitting model of a single channel HSD in SO-16L

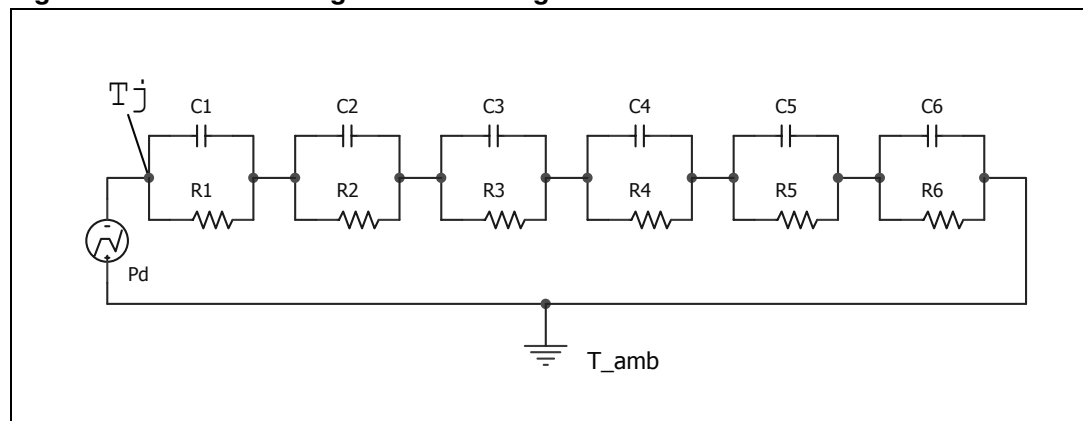
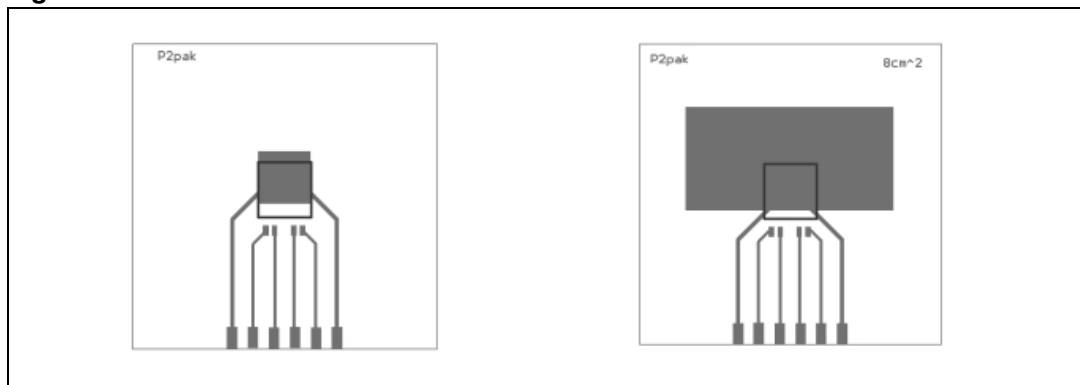


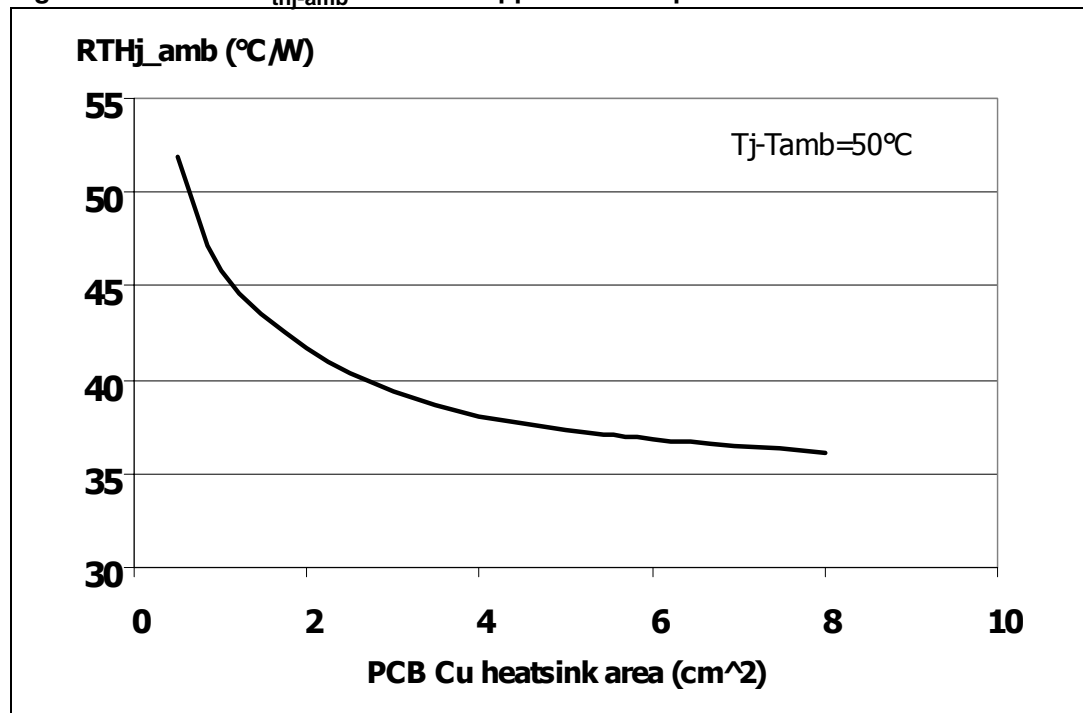
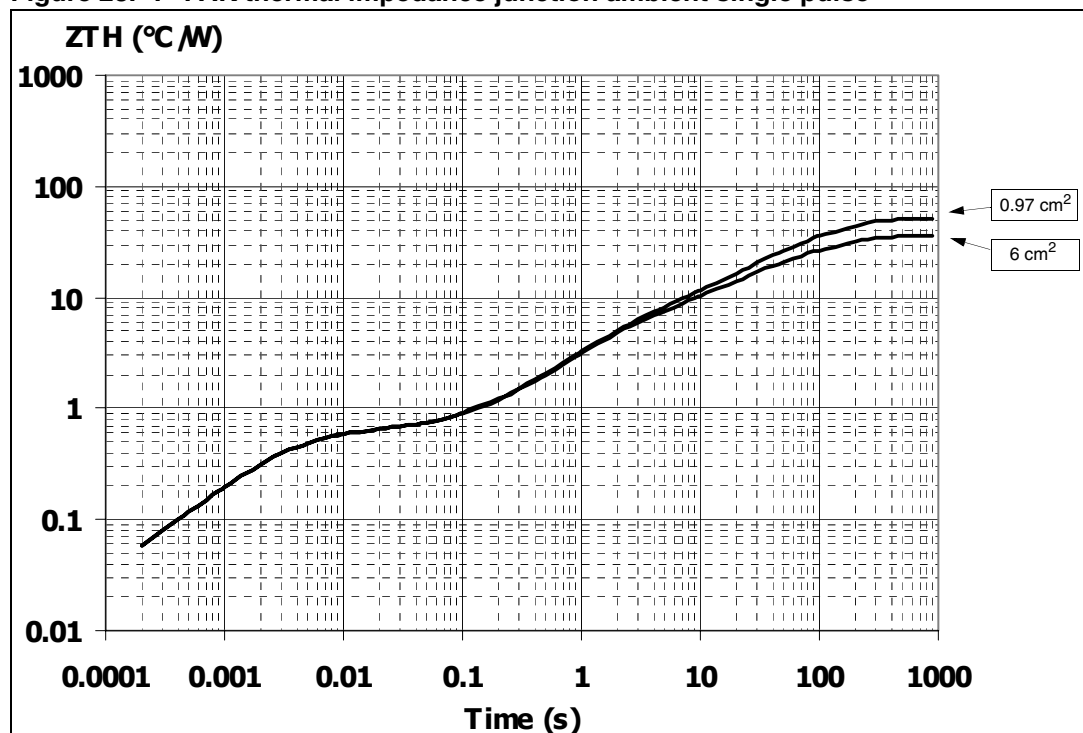
Table 13. SO-16L thermal parameters

Area / island (cm ²)	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	35	20
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	1.5E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	5	8

4.2 P²PAK thermal data

Figure 26. P²PAK PC board

Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness = 35μm, Copper areas: 0.97cm², 8cm²).

Figure 27. P²PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air conditionFigure 28. P²PAK thermal impedance junction ambient single pulse

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 29. Thermal fitting model of a single channel HSD in P²PAK

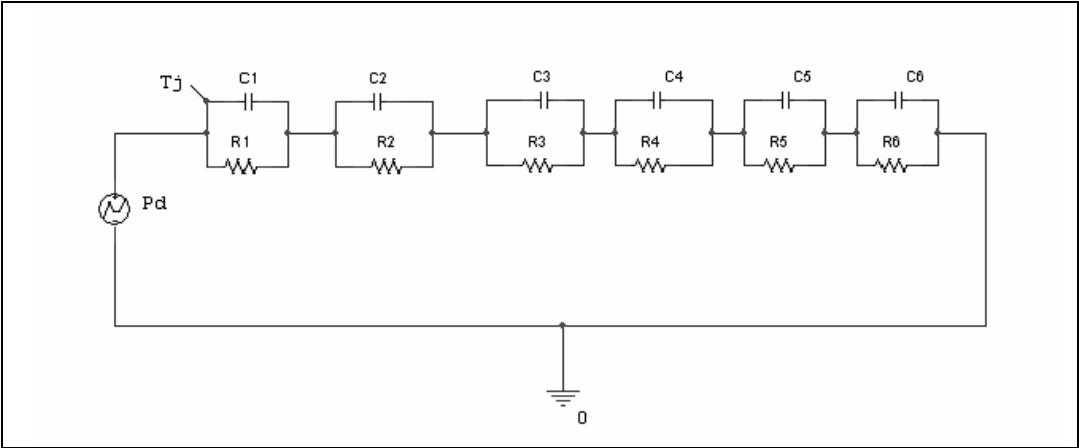


Table 14. P²PAK thermal parameter

Area/island (cm ²)	0.97	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.22	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0015	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 30. SO-16L package dimensions

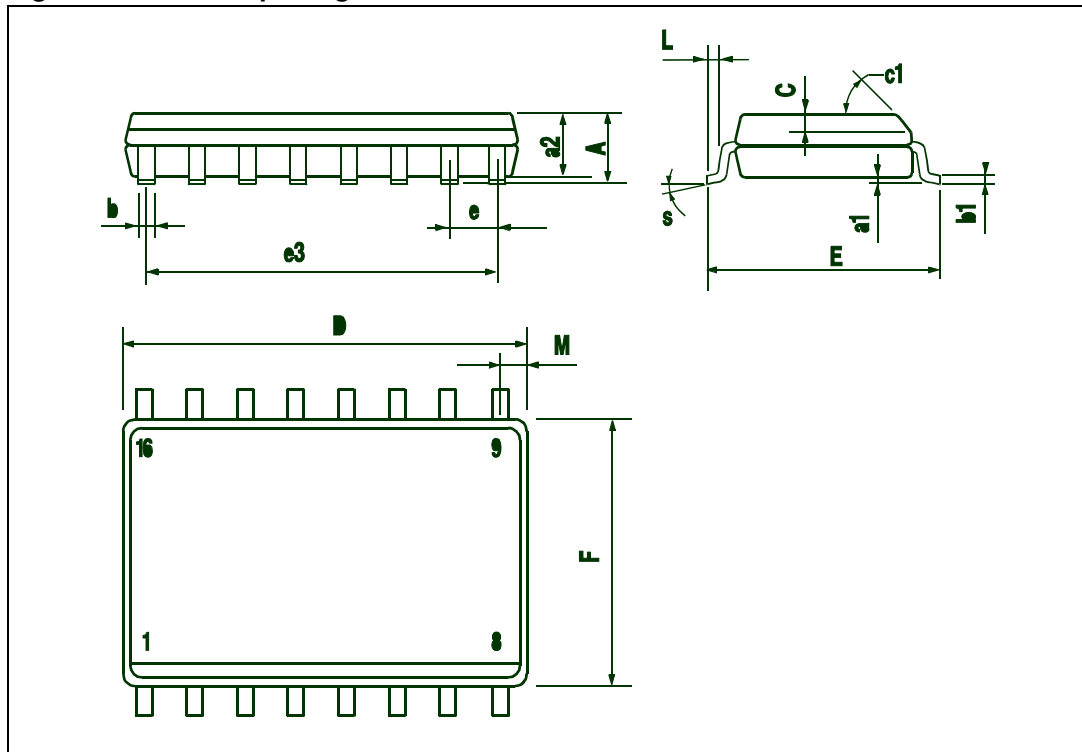


Table 15. SO-16L mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		

DIM.	mm.		
	Min.	Typ.	Max.
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

The technical drawing illustrates a 10-pin D-sub connector. The side view (top) shows the connector's profile with dimensions: A (total height), C (flange thickness), L (total length), L1 (body length), L2 (shell length), L3 (total length including pins), L5 (flange to body distance), D (shell thickness), D1 (internal diameter), E (pin thickness), M (total pin length), and M1 (pin length to shell end). The front view (bottom) shows the connector's face with dimensions: H3 (total height), Dia. (hole diameter), L7 (flange width), L6 (total width), F1 (pin spacing), H2 (pin height), F (pin thickness), G (pin length), and G1 (total pin length).

Table 16. PENTAWATT mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6
G1	6.6	6.8	7
H2			10.4
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

5.3 P²PAK mechanical data

Figure 32. P²PAK package dimensions

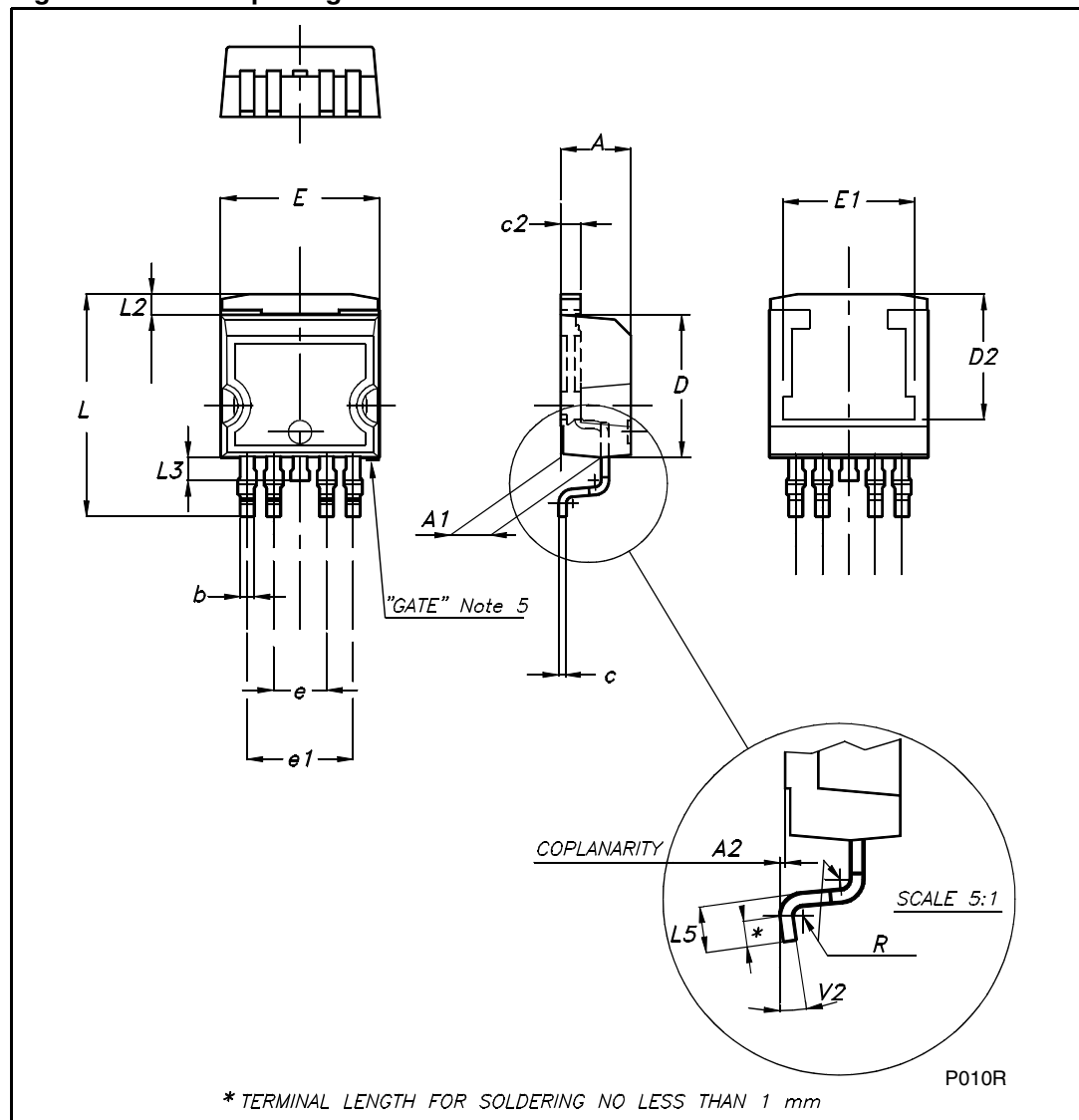


Table 17. P²PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package weight	1.40 Gr (typ)		

5.4 SO-16L packing information

Figure 33. SO-16L tube shipment (no suffix)

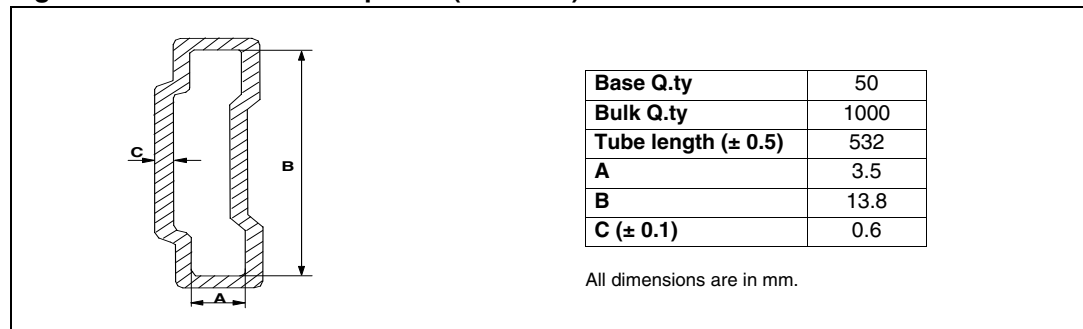
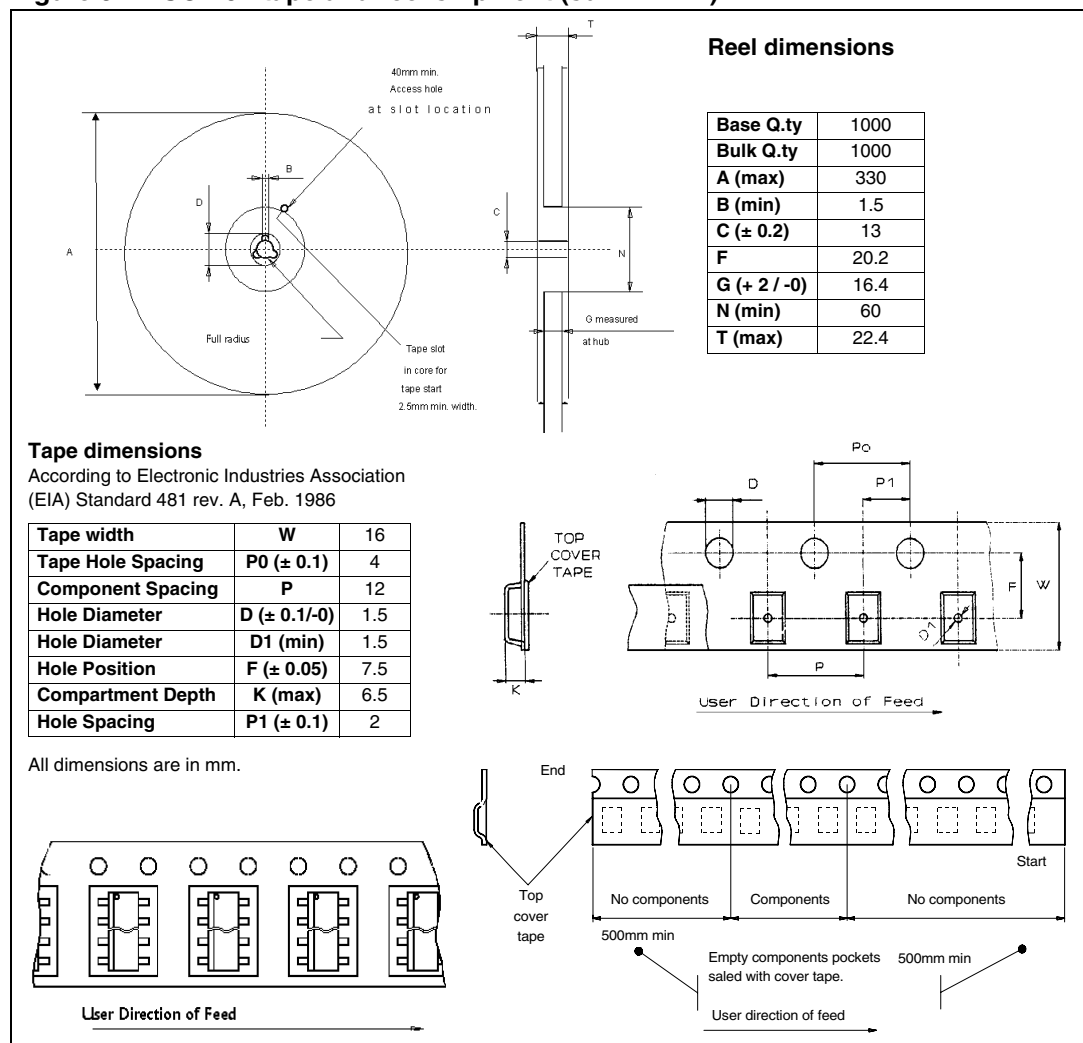
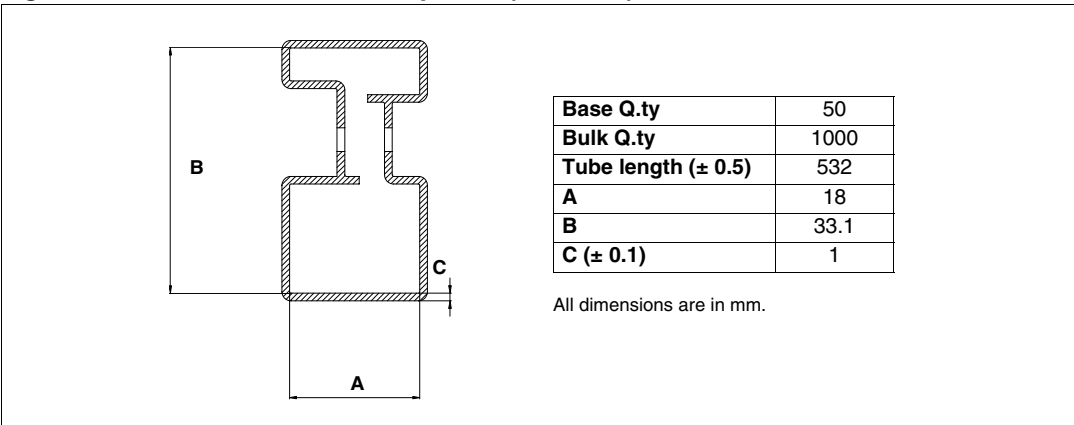


Figure 34. SO-16L tape and reel shipment (suffix "TR")



5.5 PENTAWATT packing information

Figure 35. PENTAWATT tube shipment (no suffix)



5.6 P²PAK packing information

Figure 36. P²PAK tube shipment (no suffix)

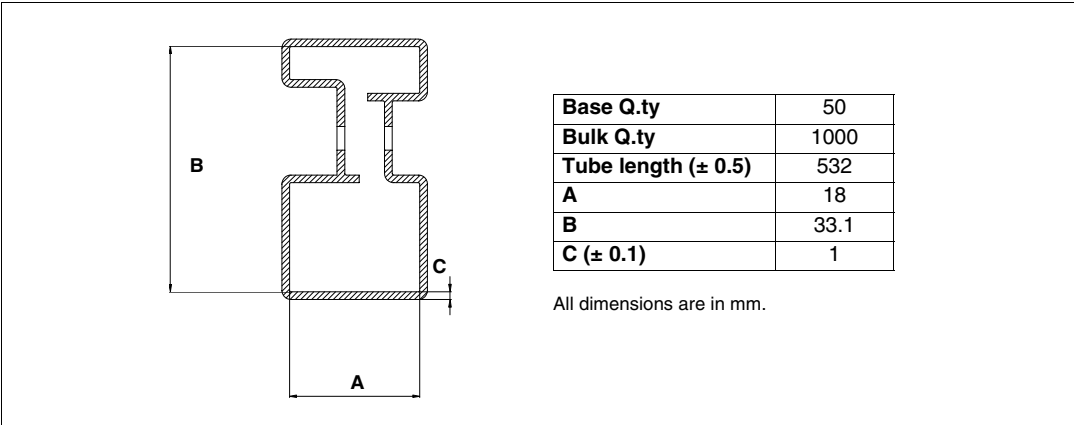
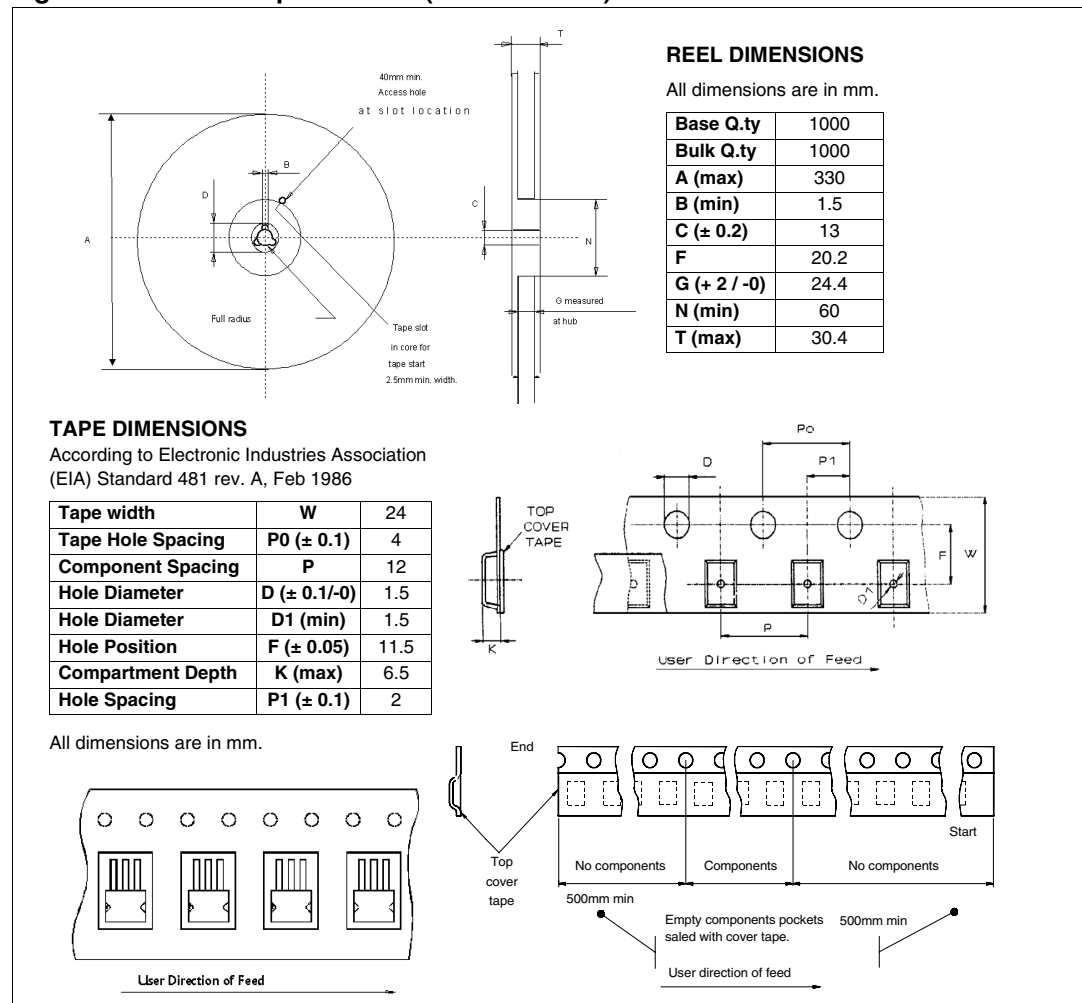


Figure 37. P²PAK tape and reel (suffix “13TR”)

6 Revision history

Table 18. Document revision history

Date	Revision	Changes
22-Jun-2004	1	Initial release.
07-Jul-2004	2	Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and n.c. pins insertion (page 2). 6cm2 Cu condition insertion in thermal data table (page 3).
09-Jul-2004	3	V _{CC} - output diode section update (page 5). Protections note insertion (page 5). Revision history table insertion (page 24). Disclaimers update (page 25).
03-May-2006	4	Suggested connections for unused and n.c.pins? correction (page 2).
17-Dec-2008	5	Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK® packages</i> information. Updated <i>Figure 37.: P²PAK tape and reel (suffix "13TR")</i> : changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.
24-Sep-2013	6	Updated Disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com