NEC

MOS INTEGRATED CIRCUIT

MC-222263-X

MCP (MULTI-CHIP PACKAGE) FLASH MEMORY AND SRAM
32M-BIT FLASH MEMORY AND 8M-BIT SRAM

Description

The MC-222263-X is a stacked type MCP (Multi-Chip Package) of 33,554,432 bits (BYTE mode : 4,194,304 words by 8 bits, WORD mode : 2,097,152 words by 16 bits) flash memory and 8,388,608 bits (BYTE mode : 1,048,576 words by 8 bits, WORD mode : 524,288 words by 16 bits) static RAM.

The MC-222263-X is packaged in a 77-pin TAPE FBGA.

Features

General Features

- Fast access time : t_{ACC} = 85 ns (MAX.) (Flash Memory), t_{AA} = 70 ns (MAX.) (SRAM)
- Supply voltage : $V_{CC}f$ / $V_{CC}s$ = 2.7 to 3.6 V
- Wide operating temperature : T_A = –25 to +85°C

Flash Memory Features

- Two bank organization enabling simultaneous execution of erase / program and read
- Bank organization : 2 banks (8M bits + 24M bits)
- Memory organization : 4,194,304 words × 8 bits (BYTE mode)
  2,097,152 words × 16 bits (WORD mode)
- Sector organization : 71 sectors (8K bytes / 4K words × 8 sectors, 64K bytes / 32K words × 63 sectors)
- Boot sector allocated to the highest address (sector)
- 3-state output
- Automatic program
  - Program suspend / resume
- Unlock bypass program
- Automatic erase
  - Chip erase
  - Sector erase (sectors can be combined freely)
  - Erase suspend / resume
- Program / Erase completion detection
  - Detection through data polling and toggle bits
  - Detection through RY (/BY) pin
- Sector group protection
  - Any sector can be protected
  - Any protected sector can be temporary unprotected
- Sectors can be used for boot application
- Hardware reset and standby using /RESET pin
- Automatic sleep mode
- Boot block sector protect by /WP (ACC) pin
- Conforms to common flash memory interface (CFI)
- Extra One Time Protect Sector provided

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The mark ★ shows major revised points.

SRAM Features

- Memory organization : 1,048,576 words × 8 bits (BYTE mode)
  524,288 words × 16 bits (WORD mode)
- Supply current : At operating : 50 mA (MAX.)
  At standby : 15 μA (MAX.)
- Two Chip Enable inputs : /CE1s, CE2s
- Byte data control : /LB, /UB
- Byte data select : CIOs
- Low V_{CC} data retention : 1.0 to 3.6 V

Ordering Information

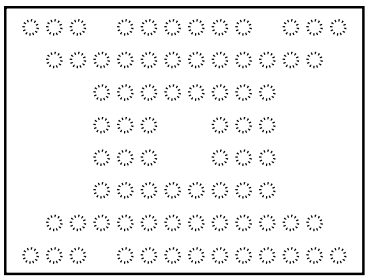
Part number	Flash Memory Boot sector	Flash Memory Access time ns (MAX.)	SRAM Access time ns (MAX.)	Package
MC-222263F9-B85X-BT3	Highest address (sector) (T type)	85	70	77-pin TAPE FBGA (12 × 7)

Pin Configuration

/xxx indicates active low signal.

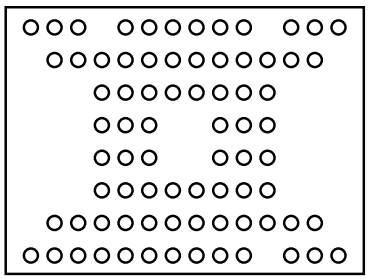
77-pin TAPE FBGA (12 × 7)

Top View



A B C D E F G H J K L M N P

Bottom View



P N M L K J H G F E D C B A

Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	NC	NC	NC		A15	NC	NC	A16	CIOf	V_{SS}		NC	NC	NC
7		NC	NC	A11	A12	A13	A14	SA	I/O15, A-1	I/O7	I/O14	NC	NC	
6				A8	A19	A9	A10	I/O6	I/O13	I/O12	I/O5			
5				/WE	CE2s	A20			I/O4	V_{CCS}	CIOs			
4				/WP(ACC)	/RESET	RY(/BY)			I/O3	V_{CCf}	I/O11			
3				/LB	/UB	A18	A17	I/O1	I/O9	I/O10	I/O2			
2		NC	NC	A7	A6	A5	A4	V_{SS}	/OE	I/O0	I/O8	NC	NC	
1	NC	NC	NC		A3	A2	A1	A0	/CEf	/CE1s	NC	NC	NC	NC

Common Pins

A0 - A18	:	Address inputs
I/O0 - I/O15	:	Data inputs / outputs
/OE	:	Output Enable
/WE	:	Write Enable
V_{SS}	:	Ground
NC [Note]	:	No Connection

Flash Memory Pins

A19, A20	:	Address inputs
I/O15, A–1	:	Data inputs / outputs 15 (WORD mode) LSB address input (BYTE mode)
/CEf	:	Chip Enable
RY (/BY)	:	Ready (Busy) output
/RESET	:	Hardware reset input
V_{CCf}	:	Supply Voltage
/WP(ACC)	:	Hardware Write Protect (Acceleration)
CIOf	:	Selects 8-bit or 16-bit mode

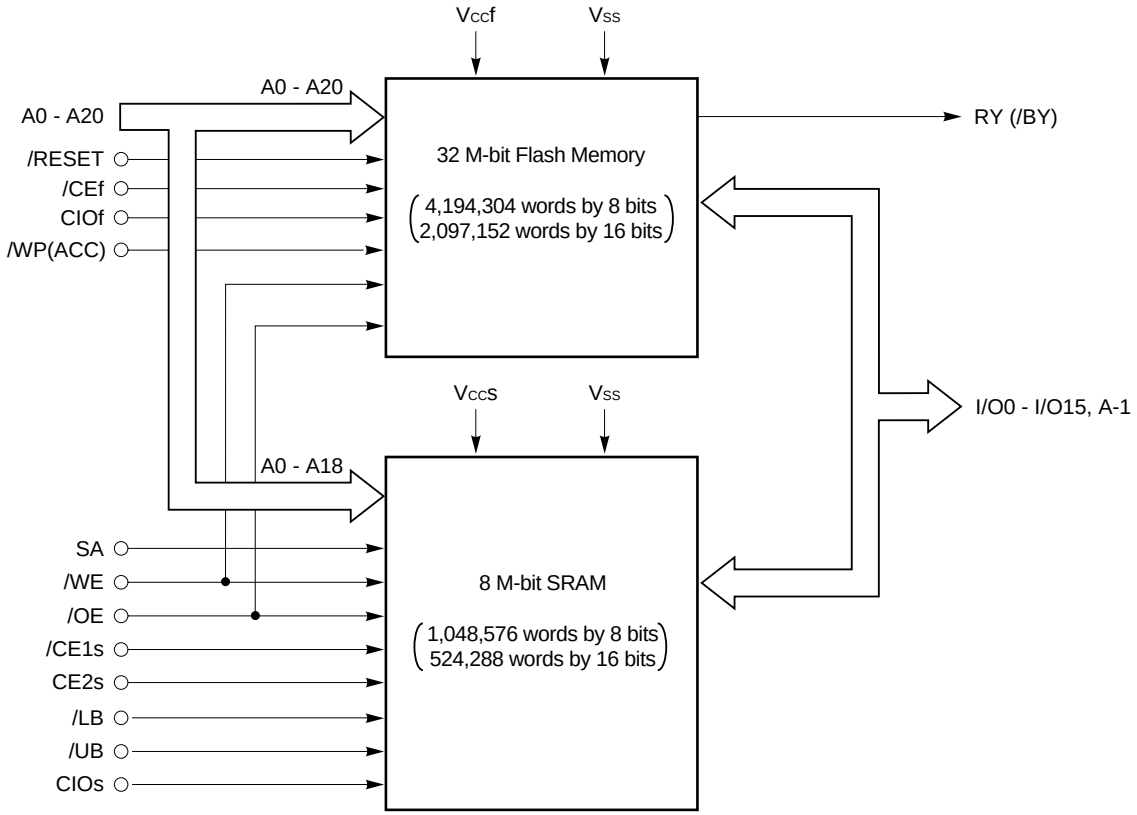
SRAM Pins

SA	:	Address input (A19 for SRAM)
/CE1s	:	Chip Enable 1
CE2s	:	Chip Enable 2
V_{CCS}	:	Supply Voltage
/LB, /UB	:	Byte data select
CIOs	:	Selects 8-bit or 16-bit mode

Note Some signals can be applied because this pin is not internally connected.

Remark Refer to **Package Drawing** for the index mark.

Block Diagram



Bus Operations Table

Operation		Flash Memory				SRAM					Common			
		/RESET	/CEf	ClOf	/WP(ACC)	/CE1s	CE2s	/LB	/UB	ClOs	/OE	/WE	I/O0 - I/O7	I/O8-I/O15
Full standby		H	H	×	×	H	×	×	×	×	×	×	Hi-Z	Hi-Z
						×	L							
						×	×	H	H					
Output disable		H	L	×	×	L	H	×	×	×	H	H	Hi-Z	Hi-Z
Read (Flash Memory [Note 1])	BYTE mode	H	L	L	×	**Note 2**					L	H	Data Out	Hi-Z
	WORD mode			H									Data Out	Data Out
Write (Flash Memory)	BYTE mode	H	L	L	×	**Note 2**					H	L	Data In	Hi-Z
	WORD mode			H									Data In	Data In
Temporary sector group unprotect		VID	×	×	×	**Note 2**					×	×	Hi-Z or Data In/Out	Hi-Z or Data In/Out
Boot block sector protect		×	×	×	L	×	×	×	×	×	×	×	Hi-Z or Data In/Out	Hi-Z or Data In/Out
Flash Memory hardware reset		L	×	×	×	×	×	×	×	×	×	×	Hi-Z	Hi-Z
Read (SRAM)	BYTE mode	**Note 3**				L	H	×	×	L	L	H	Data Out	Hi-Z
	WORD mode	**Note 3**				L	H	L	L	H	L	H	Data Out	Data Out
									H					Hi-Z
								H	L				Hi-Z	Data Out
Write (SRAM)	BYTE mode	**Note 3**				L	H	×	×	L	×	L	Data In	Hi-Z
	WORD mode	**Note 3**				L	H	L	L	H	×	L	Data In	Data In
									H					Hi-Z
								H	L				Hi-Z	Data In

Caution Other operations except for indicated in this table are inhibited.

Notes 1. When /OE = VIL, VIL can be applied to /WE. When /OE = VIH, a write operation is started.

2. SRAM should be Standby.

3. Flash Memory should be Standby or Hardware reset.

Remarks 1. H : VIH, L : VIL, × : VIH or VIL

2. Sector group protection and read the product ID are using a command.

★ **3.** Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)** for the flash memory bus operations.

Sector Organization / Sector Address Table (Flash Memory)

Flash Memory top boot **(1/2)**

Bank	Sector Organization	Address		Sectors Address	Sector Address Table								
					Bank Address Table								
	K bytes / K words	BYTE mode	WORD mode		A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 1	8/4	3FFFFFH 3FE000H	1FFFFFH 1FF000H	FSA70	1	1	1	1	1	1	1	1	1
	8/4	3FDFFFH 3FC000H	1FEFFFH 1FE000H	FSA69	1	1	1	1	1	1	1	1	0
	8/4	3FBFFFH 3FA000H	1FDFFFH 1FD000H	FSA68	1	1	1	1	1	1	1	0	1
	8/4	3F9FFFH 3F8000H	1FCFFFH 1FC000H	FSA67	1	1	1	1	1	1	1	0	0
	8/4	3F7FFFH 3F6000H	1FBFFFH 1FB000H	FSA66	1	1	1	1	1	1	0	1	1
	8/4	3F5FFFH 3F4000H	1FAFFFH 1FA000H	FSA65	1	1	1	1	1	1	0	1	0
	8/4	3F3FFFH 3F2000H	1F9FFFH 1F9000H	FSA64	1	1	1	1	1	1	0	0	1
	8/4	3F1FFFH 3F0000H	1F8FFFH 1F8000H	FSA63	1	1	1	1	1	1	0	0	0
	64/32	3EFFFFH 3E0000H	1F7FFFH 1F0000H	FSA62	1	1	1	1	1	0	x	x	x
	64/32	3DFFFFH 3D0000H	1EFFFFH 1E8000H	FSA61	1	1	1	1	0	1	x	x	x
	64/32	3CFFFFH 3C0000H	1E7FFFH 1E0000H	FSA60	1	1	1	1	0	0	x	x	x
	64/32	3BFFFFH 3B0000H	1DFFFFH 1D8000H	FSA59	1	1	1	0	1	1	x	x	x
	64/32	3AFFFFH 3A0000H	1D7FFFH 1D0000H	FSA58	1	1	1	0	1	0	x	x	x
	64/32	39FFFFH 390000H	1CFFFFH 1C8000H	FSA57	1	1	1	0	0	1	x	x	x
	64/32	38FFFFH 380000H	1C7FFFH 1C0000H	FSA56	1	1	1	0	0	0	x	x	x
	64/32	37FFFFH 370000H	1BFFFFH 1B8000H	FSA55	1	1	0	1	1	1	x	x	x
	64/32	36FFFFH 360000H	1B7FFFH 1B0000H	FSA54	1	1	0	1	1	0	x	x	x
	64/32	35FFFFH 350000H	1AFFFFH 1A8000H	FSA53	1	1	0	1	0	1	x	x	x
	64/32	34FFFFH 340000H	1A7FFFH 1A0000H	FSA52	1	1	0	1	0	0	x	x	x
	64/32	33FFFFH 330000H	19FFFFH 198000H	FSA51	1	1	0	0	1	1	x	x	x
	64/32	32FFFFH 320000H	197FFFH 190000H	FSA50	1	1	0	0	1	0	x	x	x
	64/32	31FFFFH 310000H	18FFFFH 188000H	FSA49	1	1	0	0	0	1	x	x	x
	64/32	30FFFFH 300000H	187FFFH 180000H	FSA48	1	1	0	0	0	0	x	x	x
Bank 2	64/32	2FFFFFH 2F0000H	17FFFFH 178000H	FSA47	1	0	1	1	1	1	x	x	x
	64/32	2EFFFFH 2E0000H	177FFFH 170000H	FSA46	1	0	1	1	1	0	x	x	x
	64/32	2DFFFFH 2D0000H	16FFFFH 168000H	FSA45	1	0	1	1	0	1	x	x	x
	64/32	2CFFFFH 2C0000H	167FFFH 160000H	FSA44	1	0	1	1	0	0	x	x	x
	64/32	2BFFFFH 2B0000H	15FFFFH 158000H	FSA43	1	0	1	0	1	1	x	x	x
	64/32	2AFFFFH 2A0000H	157FFFH 150000H	FSA42	1	0	1	0	1	0	x	x	x
	64/32	29FFFFH 290000H	14FFFFH 148000H	FSA41	1	0	1	0	0	1	x	x	x
	64/32	28FFFFH 280000H	147FFFH 140000H	FSA40	1	0	1	0	0	0	x	x	x
	64/32	27FFFFH 270000H	13FFFFH 138000H	FSA39	1	0	0	1	1	1	x	x	x
	64/32	26FFFFH 260000H	137FFFH 130000H	FSA38	1	0	0	1	1	0	x	x	x
	64/32	25FFFFH 250000H	12FFFFH 128000H	FSA37	1	0	0	1	0	1	x	x	x
	64/32	24FFFFH 240000H	127FFFH 120000H	FSA36	1	0	0	1	0	0	x	x	x
	64/32	23FFFFH 230000H	11FFFFH 118000H	FSA35	1	0	0	0	1	1	x	x	x

(2/2)

Bank	Sector Organization K bytes / K words	Address		Sectors Address	Sector Address Table								
					Bank Address Table								
		BYTE mode	WORD mode		A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 2	64/32	22FFFFH 220000H	117FFFH 110000H	FSA34	1	0	0	0	1	0	x	x	x
	64/32	21FFFFH 210000H	10FFFFH 108000H	FSA33	1	0	0	0	0	1	x	x	x
	64/32	20FFFFH 200000H	107FFFH 100000H	FSA32	1	0	0	0	0	0	x	x	x
	64/32	1FFFFFH 1F0000H	0FFFFFH 0F8000H	FSA31	0	1	1	1	1	1	x	x	x
	64/32	1EFFFFH 1E0000H	0F7FFFH 0F0000H	FSA30	0	1	1	1	1	0	x	x	x
	64/32	1DFFFFH 1D0000H	0EFFFFH 0E8000H	FSA29	0	1	1	1	0	1	x	x	x
	64/32	1CFFFFH 1C0000H	0E7FFFH 0E0000H	FSA28	0	1	1	1	0	0	x	x	x
	64/32	1BFFFFH 1B0000H	0DFFFFH 0D8000H	FSA27	0	1	1	0	1	1	x	x	x
	64/32	1AFFFFH 1A0000H	0D7FFFH 0D0000H	FSA26	0	1	1	0	1	0	x	x	x
	64/32	19FFFFH 190000H	0CFFFFH 0C8000H	FSA25	0	1	1	0	0	1	x	x	x
	64/32	18FFFFH 180000H	0C7FFFH 0C0000H	FSA24	0	1	1	0	0	0	x	x	x
	64/32	17FFFFH 170000H	0BFFFFH 0B8000H	FSA23	0	1	0	1	1	1	x	x	x
	64/32	16FFFFH 160000H	0B7FFFH 0B0000H	FSA22	0	1	0	1	1	0	x	x	x
	64/32	15FFFFH 150000H	0AFFFFH 0A8000H	FSA21	0	1	0	1	0	1	x	x	x
	64/32	14FFFFH 140000H	0A7FFFH 0A0000H	FSA20	0	1	0	1	0	0	x	x	x
	64/32	13FFFFH 130000H	09FFFFH 098000H	FSA19	0	1	0	0	1	1	x	x	x
	64/32	12FFFFH 120000H	097FFFH 090000H	FSA18	0	1	0	0	1	0	x	x	x
	64/32	11FFFFH 110000H	08FFFFH 088000H	FSA17	0	1	0	0	0	1	x	x	x
	64/32	10FFFFH 100000H	087FFFH 080000H	FSA16	0	1	0	0	0	0	x	x	x
	64/32	0FFFFFH 0F0000H	07FFFFH 078000H	FSA15	0	0	1	1	1	1	x	x	x
	64/32	0EFFFFH 0E0000H	077FFFH 070000H	FSA14	0	0	1	1	1	0	x	x	x
	64/32	0DFFFFH 0D0000H	06FFFFH 068000H	FSA13	0	0	1	1	0	1	x	x	x
	64/32	0CFFFFH 0C0000H	067FFFH 060000H	FSA12	0	0	1	1	0	0	x	x	x
	64/32	0BFFFFH 0B0000H	05FFFFH 058000H	FSA11	0	0	1	0	1	1	x	x	x
	64/32	0AFFFFH 0A0000H	057FFFH 050000H	FSA10	0	0	1	0	1	0	x	x	x
	64/32	09FFFFH 090000H	04FFFFH 048000H	FSA9	0	0	1	0	0	1	x	x	x
	64/32	08FFFFH 080000H	047FFFH 040000H	FSA8	0	0	1	0	0	0	x	x	x
	64/32	07FFFFH 070000H	03FFFFH 038000H	FSA7	0	0	0	1	1	1	x	x	x
	64/32	06FFFFH 060000H	037FFFH 030000H	FSA6	0	0	0	1	1	0	x	x	x
	64/32	05FFFFH 050000H	02FFFFH 028000H	FSA5	0	0	0	1	0	1	x	x	x
	64/32	04FFFFH 040000H	027FFFH 020000H	FSA4	0	0	0	1	0	0	x	x	x
	64/32	03FFFFH 030000H	01FFFFH 018000H	FSA3	0	0	0	0	1	1	x	x	x
	64/32	02FFFFH 020000H	017FFFH 010000H	FSA2	0	0	0	0	1	0	x	x	x
	64/32	01FFFFH 010000H	00FFFFH 008000H	FSA1	0	0	0	0	0	1	x	x	x
	64/32	00FFFFH 000000H	007FFFH 000000H	FSA0	0	0	0	0	0	0	x	x	x

★ **Sector Group Address Table (Flash Memory)**

Sector group	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA0	0	0	0	0	0	0	×	×	×	64 KB (1 Sector)	FSA0
SGA1	0	0	0	0	0	1	×	×	×	192 KB (3 Sectors)	FSA1–FSA3
					1	0					
					1	1					
SGA2	0	0	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA4–FSA7
SGA3	0	0	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA8–FSA11
SGA4	0	0	1	1	×	×	×	×	×	256 KB (4 Sectors)	FSA12–FSA15
SGA5	0	1	0	0	×	×	×	×	×	256 KB (4 Sectors)	FSA16–FSA19
SGA6	0	1	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA20–FSA23
SGA7	0	1	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA24–FSA27
SGA8	0	1	1	1	×	×	×	×	×	256 KB (4 Sectors)	FSA28–FSA31
SGA9	1	0	0	0	×	×	×	×	×	256 KB (4 Sectors)	FSA32–FSA35
SGA10	1	0	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA36–FSA39
SGA11	1	0	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA40–FSA43
SGA12	1	0	1	1	×	×	×	×	×	256 KB (4 Sectors)	FSA44–FSA47
SGA13	1	1	0	0	×	×	×	×	×	256 KB (4 Sectors)	FSA48–FSA51
SGA14	1	1	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA52–FSA55
SGA15	1	1	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA56–FSA59
SGA16	1	1	1	1	0	0	×	×	×	192 KB (3 Sectors)	FSA60–FSA62
					0	1					
					1	0					
SGA17	1	1	1	1	1	1	0	0	0	8 KB (1 Sector)	FSA63
SGA18	1	1	1	1	1	1	0	0	1	8 KB (1 Sector)	FSA64
SGA19	1	1	1	1	1	1	0	1	0	8 KB (1 Sector)	FSA65
SGA20	1	1	1	1	1	1	0	1	1	8 KB (1 Sector)	FSA66
SGA21	1	1	1	1	1	1	1	0	0	8 KB (1 Sector)	FSA67
SGA22	1	1	1	1	1	1	1	0	1	8 KB (1 Sector)	FSA68
SGA23	1	1	1	1	1	1	1	1	0	8 KB (1 Sector)	FSA69
SGA24	1	1	1	1	1	1	1	1	1	8 KB (1 Sector)	FSA70

Remark × : V_{IH} or V_{IL}

Command Sequence (Flash Memory)

Command sequence		Bus	1st bus Cycle		2nd bus Cycle		3rd bus Cycle		4th bus Cycle		5th bus Cycle		6th bus Cycle	
		Cycle	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset [Note1]		1	×××H	F0H	RA	RD	–	–	–	–	–	–	–	–
Read / Reset [Note1]	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	F0H	RA	RD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program Suspend [Note 2]		1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Program Resume [Note 3]		1	BA	30H	–	–	–	–	–	–	–	–	–	–
Chip Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
	WORD mode		555H		2AAH		555H		555H		2AAH		555H	
Sector Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	FSA	30H
	WORD mode		555H		2AAH		555H		555H		2AAH			
Sector Erase Suspend [Note 4]		1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Sector Erase Resume [Note 5]		1	BA	30H	–	–	–	–	–	–	–	–	–	–
Unlock Bypass Set	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	20H	–	–	–	–	–	–
	WORD mode		555H		2AAH		555H							
Unlock Bypass Program [Note 6]		2	×××H	A0H	PA	PD	–	–	–	–	–	–	–	–
Unlock Bypass Reset [Note 6]		2	BA	90H	×××H	00H[Note11]	–	–	–	–	–	–	–	–
Product ID	BYTE mode	3	AAAH	AAH	555H	55H	(BA) AAAH	90H	IA	ID	–	–	–	–
	WORD mode		555H		2AAH		(BA) 555H							
Sector Group Protection [Note 7]		4	×××H	60H	SPA	60H	SPA	40H	SPA	SD	–	–	–	–
Sector Group Unprotect [Note 8]		4	×××H	60H	SUA	60H	SUA	40H	SUA	SD	–	–	–	–
Query [Note 9]	BYTE mode	1	AAH	98H	–	–	–	–	–	–	–	–	–	–
	WORD mode		55H											
Extra One Time Protect	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	88H	–	–	–	–	–	–
Sector Entry	WORD mode		555H		2AAH		555H							
Extra One Time Protect	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
Sector Program [Note 10]	WORD mode		555H		2AAH		555H							
Extra One Time Protect	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	EOTPSA	30H
Sector Erase [Note 10]	WORD mode		555H		2AAH		555H		555H		2AAH			
Extra One Time Protect	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	90H	xxxH	00H	–	–	–	–
Sector Reset [Note 10]	WORD mode		555H		2AAH		555H							
Extra One Time Protect Sector Protection [Note 10]		4	×××H	60H	EOTPSA	60H	EOTPSA	40H	EOTPSA	SD	–	–	–	–

Notes 1. Both these read / reset commands reset the device to the read mode.

2. Programming is suspended if B0H is input to the bank address being programmed to in a program operation.

3. Programming is resumed if 30H is input to the bank address being suspended to in a program-suspend operation.

4. Erasure is suspended if B0H is input to the bank address being erased in a sector erase operation.

5. Erasure is resumed if 30H is input to the bank address being suspended in a sector-erase-suspend operation.

6. Valid only in the unlock bypass mode.

7. Valid only when /RESET = V_{ID} (except in the Extra One Time Protect Sector mode).

8. The command sequence that protects a sector group is excluded.

9. Only A0 to A6 are valid as an address.

10. Valid only in the Extra One Time Protect Sector mode.

11. This command can be used even if this data is F0H.

Remarks 1. Specify address 555H or 2AAH (A10 to A0) in the WORD mode, and AAAH or 555H (A10 to A0, A-1) in the BYTE mode.

2. RA : Read address

RD : Read data

IA : Address input

xx00H (to read the manufacturer code)

xx02H (to read the device code in the BYTE mode)

xx01H (to read the device code in the WORD mode)

ID : Code output. Refer to the **Product ID code (Manufacturer code / Device code) (Flash Memory)**.

PA : Program address

PD : Program data

FSA: Erase sector address. The sector to be erased is selected by the combination of this address. Refer to the **Sector Organization / Sector Address Table (Flash Memory)**.

BA : Bank address. Refer to the **Sector Organization / Sector Address Table (Flash Memory)**.

SPA : Sector group address to be protected. Set sector group address (SGA) and (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}). For the sector group address, refer to the **Sector Group Address Table (Flash Memory)**.

SUA : Unprotect sector group address. Set sector group address (SGA) and (A6, A1, A0) = (V_{IH}, V_{IH}, V_{IL}). For the sector group address, refer to the **Sector Group Address Table (Flash Memory)**.

SD : Data for verifying whether sector groups read from the address specified by SPA, SUA, and EOTPSA are protected.

EOTPSA : Extra One Time Protect Sector area addresses.

BYTE mode : 3F0000H to 3FFFFFH, WORD mode : 1F8000H to 1FFFFFH

3. The sector group address is don't care except when a program / erase address or read address are selected.

4. For the operation of the bus, refer to **Bus Operations Table**.

5. × of address bit indicates V_{IH} or V_{IL}.

★ **6.** Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)** for the flash memory commands.

Product ID Code (Manufacturer Code / Device Code) (Flash Memory)

Product ID Code	Address inputs			Output
	A6	A1	A0	Hex
Manufacturer Code	L	L	L	10H
Device code	L	L	H	50H (BYTE mode), 2250H (WORD mode)

Product ID Code		Code outputs																
		I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	Hex
Manufacturer Code		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	10H
Device code	BYTE mode	A-1	x	x	x	x	x	x	x	0	1	0	1	0	0	0	0	50H
	WORD mode	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0	2250H

Remark H : V_{IH}, L : V_{IL}, x : Hi-Z

★ **Hardware Sequence Flags, Hardware Data Protection (Flash Memory)**

Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

Electrical Specifications

Before turning on power, input $V_{SS} \pm 0.2$ V to the /RESET pin until $V_{CCf} \geq V_{CCf}$ (MIN.).

Absolute Maximum Ratings

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{CCf}, V_{CCS}	with respect to V_{SS}		–0.5 to +4.0	V
Input / Output voltage	V_T	with respect to V_{SS}	/WP(ACC), /RESET	–0.5 Note 1 to +13.0	V
			except /WP(ACC), /RESET	–0.5 Note 1 to V_{CCf}, V_{CCS} + 0.4 (4.0 V MAX.) Note 2	
Ambient operation temperature	T_A			–25 to +85	°C
Storage temperature	T_{stg}			–55 to +125	°C

Notes 1. –2.0 V (MIN.) (pulse width ≤ 20 ns)

2. V_{CCf}, V_{CCS} + 0.5 V (MAX.) (pulse width ≤ 20 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CCf}, V_{CCS}		2.7		3.6	V
Ambient operation temperature	T_A		–25		+85	°C

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Common

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.4		$V_{CC}f$, $V_{CC}s$ + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.5	V
High level output voltage	V_{OH}	I_{OH} = –500 μA, $V_{CC}f$ = $V_{CC}f$ (MIN.), $V_{CC}s$ = $V_{CC}s$ (MIN.)	2.4			V
Low level output voltage	V_{OL}	I_{OL} = +1.0 mA, $V_{CC}f$ = $V_{CC}f$ (MIN.), $V_{CC}s$ = $V_{CC}s$ (MIN.)			0.4	V
Input leakage current	I_{LI}		–1.0		+1.0	μA
Output leakage current	I_{LO}		–1.0		+1.0	μA

Flash Memory

Parameter			Symbol	Test condition		MIN.	TYP.	MAX.	Unit
Power supply current	Read	BYTE mode	$I_{CC1}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /CEf = V_{IL}, /OE = V_{IH}	t_{CYCLE} = 5 MHz		10	16	mA
					t_{CYCLE} = 1 MHz		2	4	
		WORD mode			t_{CYCLE} = 5 MHz		10	16	
					t_{CYCLE} = 1 MHz		2	4	
	Program, Erase		$I_{CC2}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /CEf = V_{IL}, /OE = V_{IH}			15	30	mA
	Standby		$I_{CC3}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /CEf = /RESET = /WP(ACC) = $V_{CC}f$ ± 0.3 V, /OE = V_{IL}			0.2	5	μA
	Standby / Reset		$I_{CC4}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /RESET = V_{SS} ± 0.2 V			0.2	5	μA
	Automatic sleep mode		$I_{CC5}f$	V_{IH} = $V_{CC}f$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			0.2	5	μA
	Read during programming		$I_{CC6}f$	V_{IH} = $V_{CC}f$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			21	45	mA
	Read during erasing		$I_{CC7}f$	V_{IH} = $V_{CC}f$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			21	45	mA
	Programming during suspend		$I_{CC8}f$	/CEf = V_{IL}, /OE = V_{IH}, Automatic programming during suspend			17	35	mA
	Accelerated programming		I_{ACC}	/WP (ACC) pin			5	10	mA
				$V_{CC}f$			15	30	
/RESET high level input voltage			V_{ID}	High Voltage is applied		11.5		12.5	V
Accelerated programming voltage			V_{ACC}	High Voltage is applied		8.5		9.5	V
Low $V_{CC}f$ lock-out voltage[Note]			V_{LKO}					1.7	V

★ **Note** When $V_{CC}f$ is equal to or lower than V_{LKO}, the device ignores all write cycles. Refer to Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

SRAM

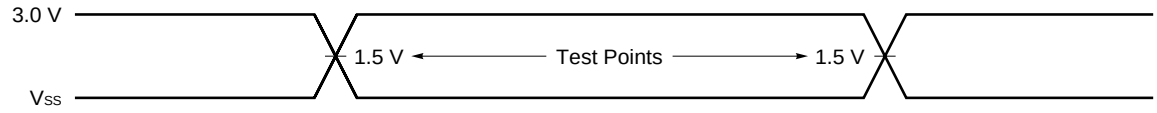
Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Power supply current	I_{CC1S}	/CE1s = V_{IL}, CE2s = V_{IH}, Minimum cycle time, $I_{I/O}$ = 0 mA		–	50	mA
		/CE1s = V_{IL}, CE2s = V_{IH}, $I_{I/O}$ = 0 mA, Cycle time = ∞		–	12	
	I_{CC2S}	/CE1s ≤ 0.2 V, CE2s ≥ $V_{CC}s$ – 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ $V_{CC}s$ – 0.2 V		–	10	
Standby supply current	I_{SB1S}	/CE1s = V_{IH} or CE2s = V_{IL} or /LB = /UB = V_{IH}		–	0.6	mA
	I_{SB2S}	/CE1s ≥ $V_{CC}s$ – 0.2 V, CE2s ≥ $V_{CC}s$ – 0.2 V		1	15	μA
		CE2s ≤ 0.2 V		1	15	
		/LB = /UB ≥ $V_{CC}s$ – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ $V_{CC}s$ – 0.2 V		1	15	

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

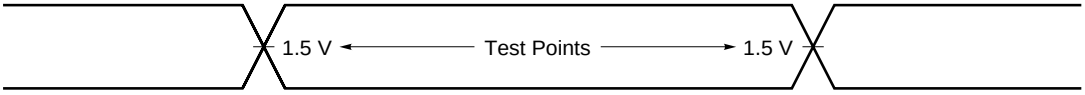
★ **AC Test Conditions**

Flash Memory

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

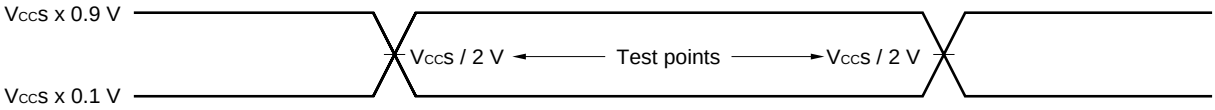


Output Load

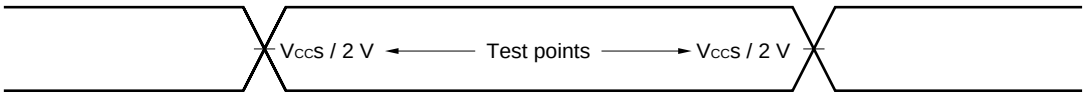
1 TTL + 30 pF

SRAM

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1 TTL + 30 pF

/CEf, /CE1s, CE2s Timing

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
/CEf, /CE1s, CE2s recover time	t_{CCR}		0			ns	

Read Cycle (Flash Memory)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Read cycle time	t_{RC}		85			ns	
Address access time	t_{ACC}	/CEf = /OE = V_{IL}			85	ns	
/CEf access time	t_{CEf}	/OE = V_{IL}			85	ns	
/OE access time	t_{OE}	/CEf = V_{IL}			40	ns	
Output disable time	t_{DF}	/OE = V_{IL} or /CEf = V_{IL}			30	ns	
Output hold time	t_{OH}		0			ns	
/RESET pulse width	t_{RP}		500			ns	
/RESET hold time before read	t_{RH}		50			ns	
/RESET low to read mode	t_{READY}				20	μs	
/CEf low to CIOf low, high	t_{ELFL}/t_{ELFH}				5	ns	
CIOf low output disable time	t_{FLQZ}				30	ns	
CIOf high access time	t_{FHQV}		85			ns	

Remark t_{DF} is the time from inactivation of /CEf or /OE to Hi-Z state output.

Write Cycle (Erase / Program) (Flash Memory)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Notes
Write cycle time		t_{WC}	85			ns	
Address setup time (/WE to address)		t_{AS}	0			ns	
Address setup time (/CEf to address)		t_{AS}	0			ns	
Address hold time (/WE to address)		t_{AH}	45			ns	
Address hold time (/CEf to address)		t_{AH}	45			ns	
Input data setup time		t_{DS}	35			ns	
Input data hold time		t_{DH}	0			ns	
/OE hold time	Read	t_{OEH}	0			ns	
	Toggle bit, Data polling		10				
Read recovery time before write (/OE to /CEf)		t_{GHEL}	0			ns	
Read recovery time before write (/OE to /WE)		t_{GHWL}	0			ns	
/WE setup time (/CEf to /WE)		t_{WS}	0			ns	
/CEf setup time (/WE to /CEf)		t_{CS}	0			ns	
/WE hold time (/CEf to /WE)		t_{WH}	0			ns	
/CEf hold time (/WE to /CEf)		t_{CH}	0			ns	
Write pulse width		t_{WP}	35			ns	
/CEf pulse width		t_{CP}	35			ns	
Write pulse width high		t_{WPH}	30			ns	
/CEf pulse width high		t_{CPH}	30			ns	
Byte programming operation time		t_{BPG}		9	200	μs	
Word programming operation time		t_{WPG}		11	200	μs	
Sector erase operation time		t_{SER}		0.7	5	s	1
V_{CC}f setup time		t_{VCS}	50			μs	
RY (/BY) recovery time		t_{RB}	0			ns	
/RESET pulse width		t_{RP}	500			ns	
/RESET high-voltage (V_{ID}) hold time from high of RY(/BY) when sector group is temporarily unprotect		t_{RRB}	20			μs	
/RESET hold time		t_{RH}	50			ns	
From completion of automatic program / erase to data output time		t_{EOE}			85	ns	
RY (/BY) delay time from valid program or erase operation		t_{BUSY}			90	ns	
Address setup time to /OE low in toggle bit		t_{ASO}	15			ns	
Address hold time to /CEf or /OE high in toggle bit		t_{AHT}	0			ns	
/CEf pulse width high for toggle bit		t_{CEPH}	20			ns	
/OE pulse width high for toggle bit		t_{OEPH}	20			ns	
Voltage transition time		t_{VLHT}	4			μs	2
Rise time to V_{ID} (/RESET)		t_{VIDR}	500			ns	3
Rise time to V_{ACC} (/WP(ACC))		t_{VACCR}	500			ns	2
Erase timeout time		t_{TOW}	50			μs	4
Erase suspend transition time		t_{SPD}			20	μs	4

Notes 1. The preprogramming time prior to the erase operation is not included.

2. Sector group protection and accelerated mode only

3. Sector group protection only.

4. Table only.

Write operation (Erase / Program) Performance (Flash Memory)

Parameter	Description		MIN.	TYP.	MAX.	Unit
Sector erase time	Excludes programming time prior to erasure			0.7	5	s
Chip erase time	Excludes programming time prior to erasure			50		s
Byte programming time	Excludes system-level overhead			9	200	μs
Word programming time	Excludes system-level overhead			11	200	μs
Chip programming time	Excludes system-level overhead	BYTE mode		40		s
		WORD mode		25		
Accelerated programming time	Excludes system-level overhead			7	150	μs
Erase / Program cycle			100,000			cycles

Read Cycle (SRAM)

Parameter	Symbol	MIN.	MAX.	Unit	Notes
Read cycle time	t_{RC}	70		ns	
Address access time	t_{AA}		70	ns	
/CE1s access time	t_{CO1}		70	ns	
CE2s access time	t_{CO2}		70	ns	
/OE to output valid	t_{OE}		35	ns	
/LB, /UB to output valid	t_{BA}		70	ns	
Output hold from address change	t_{OH}	10		ns	
/CE1s to output in Low-Z	t_{LZ1}	10		ns	
CE2s to output in Low-Z	t_{LZ2}	10		ns	
/OE to output in Low-Z	t_{OLZ}	0		ns	
/LB, /UB to output in Low-Z	t_{BLZ}	10		ns	
/CE1s to output in Hi-Z	t_{HZ1}		25	ns	
CE2s to output in Hi-Z	t_{HZ2}		25	ns	
/OE to output in Hi-Z	t_{OHZ}		25	ns	
/LB, /UB to output in Hi-Z	t_{BHZ}		25	ns	

Write Cycle (SRAM)

Parameter	Symbol	MIN.	MAX.	Unit	Notes
Write cycle time	t_{WC}	70		ns	
/CE1s to end of write	t_{CW1}	55		ns	
CE2s to end of write	t_{CW2}	55		ns	
/LB, /UB to end of write	t_{BW}	55		ns	
Address valid to end of write	t_{AW}	55		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	50		ns	
Write recovery time	t_{WR}	0		ns	
Data valid to end of write	t_{DW}	30		ns	
Data hold time	t_{DH}	0		ns	
/WE to output in Hi-Z	t_{WHZ}		25	ns	
Output active from end of write	t_{OW}	5		ns	

Low V_{CC} Data Retention Characteristics (SRAM)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	/CE1s ≥ V_{CC}s – 0.2 V, CE2s ≥ V_{CC}s – 0.2 V	1.0		3.6	V
	V_{CCDR2}	CE2s ≤ 0.2 V	1.0		3.6	
	V_{CCDR3}	/LB = /UB ≥ V_{CC}s – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V	1.0		3.6	
Data retention supply current	I_{CCDR1}	V_{CC}s = 1.5 V, /CE1s ≥ V_{CC}s – 0.2 V, CE2s ≥ V_{CC}s – 0.2 V		0.5	6	μA
	I_{CCDR2}	V_{CC}s = 1.5 V, CE2s ≤ 0.2 V		0.5	6	
	I_{CCDR3}	V_{CC}s = 1.5 V, /LB = /UB ≥ V_{CC}s – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V		0.5	6	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		t_{RC} Note			ns

Note t_{RC} : Read cycle time

Figure 1. Alternating SRAM to Flash Memory Timing Chart

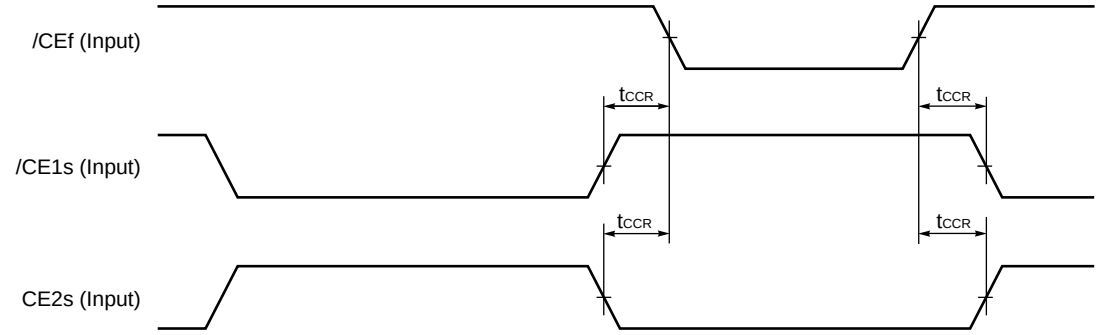


Figure 2. Read Cycle Timing Chart 1 (Flash Memory)

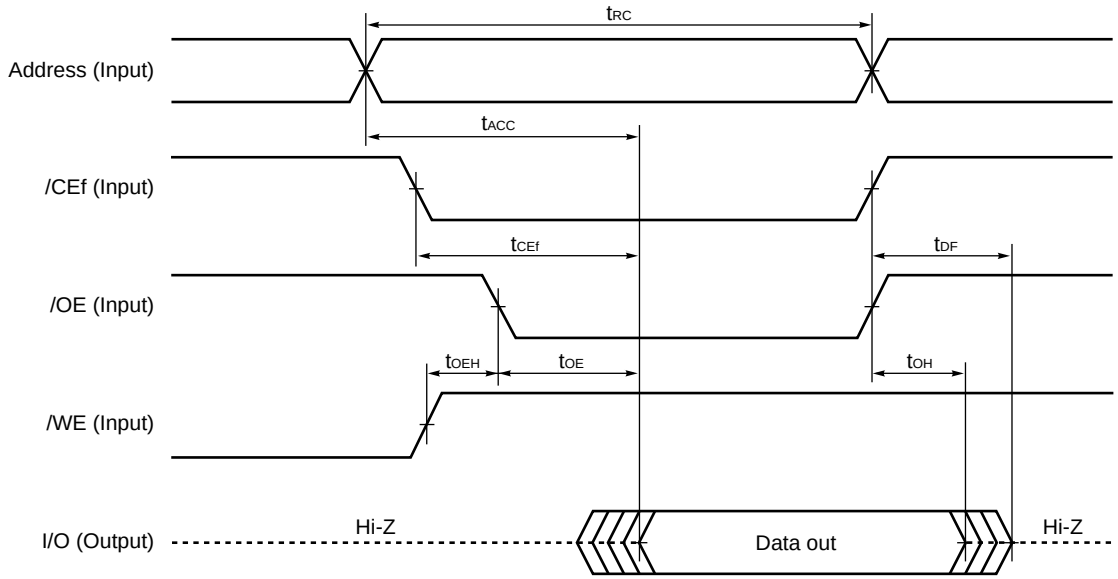


Figure 3. Read Cycle Timing Chart 2 (Flash Memory)

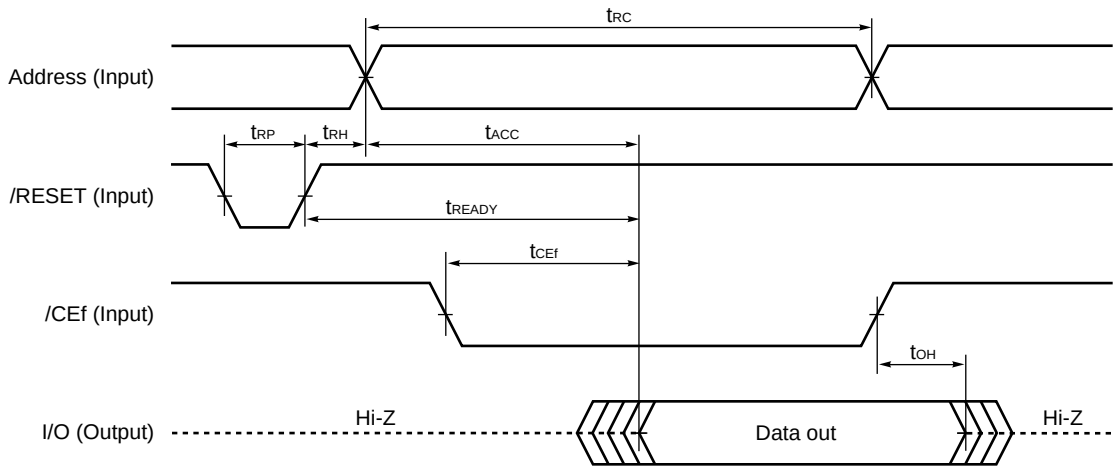
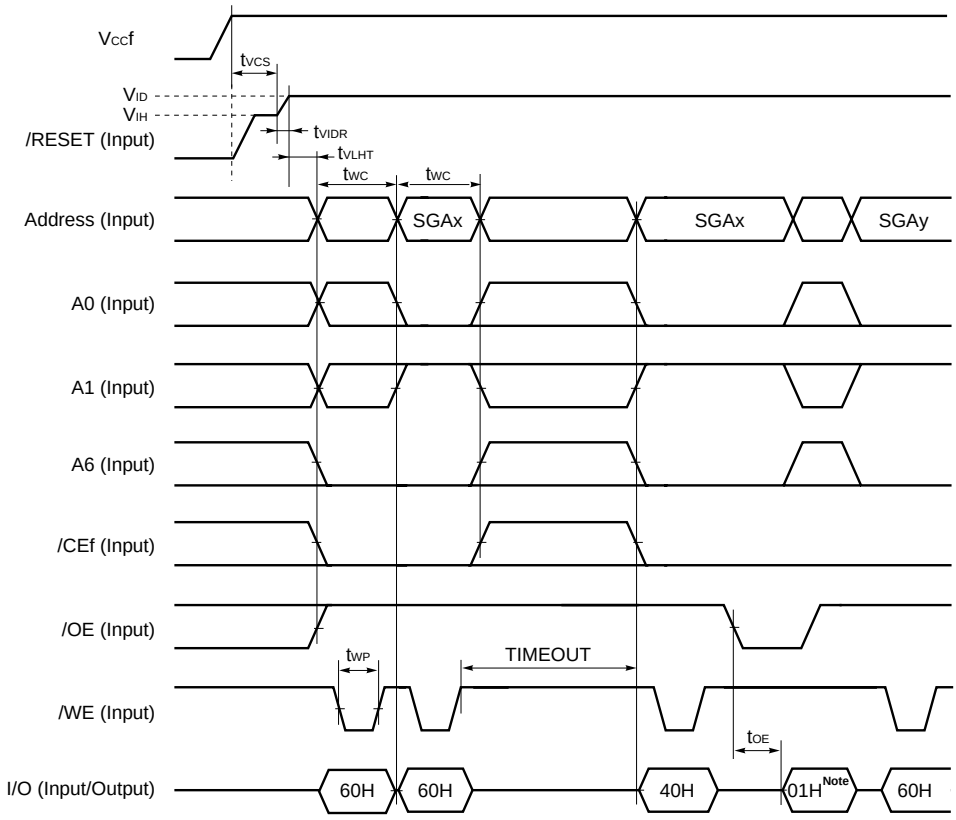


Figure 4. Sector Group Protection Timing Chart (Flash Memory)



Note The sector group protection verification result is output.

01H : The sector group is protected.

00H : The sector group is not protected.

Figure 5. Temporary Sector Group Unprotect Timing Chart (Flash Memory)

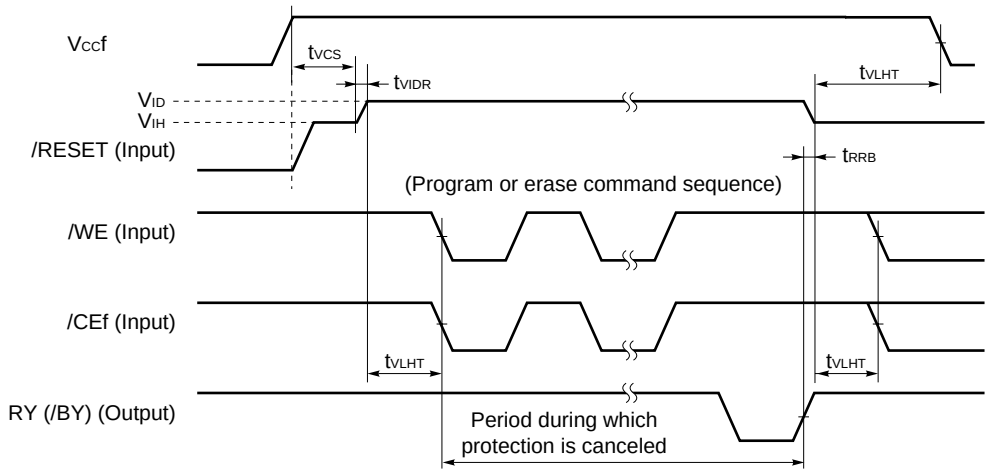


Figure 6. Accelerated Mode Timing Chart (Flash Memory)

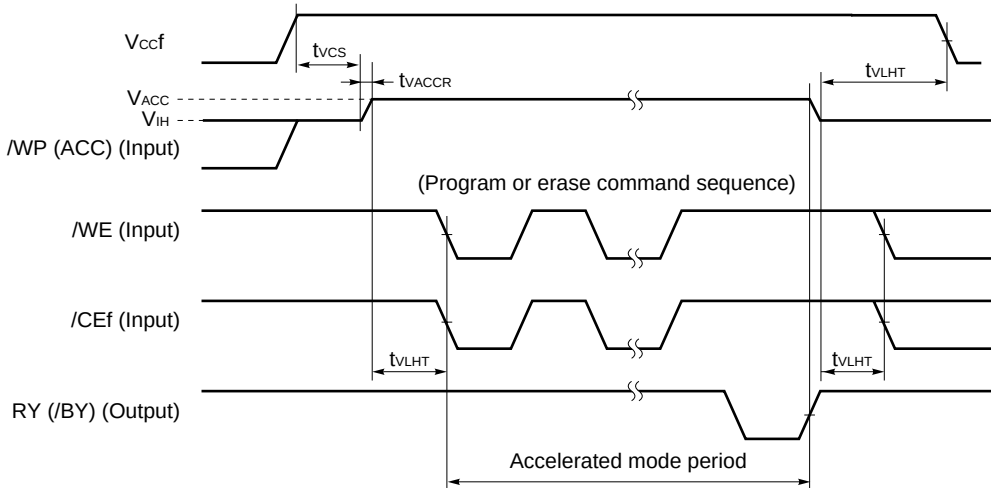


Figure 7. Dual Operation Timing Chart (Flash Memory)

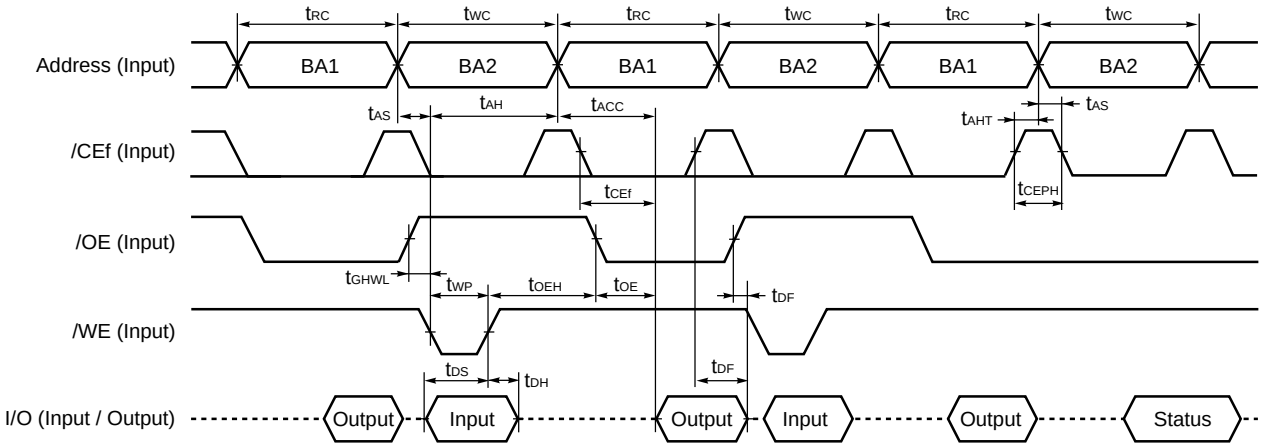
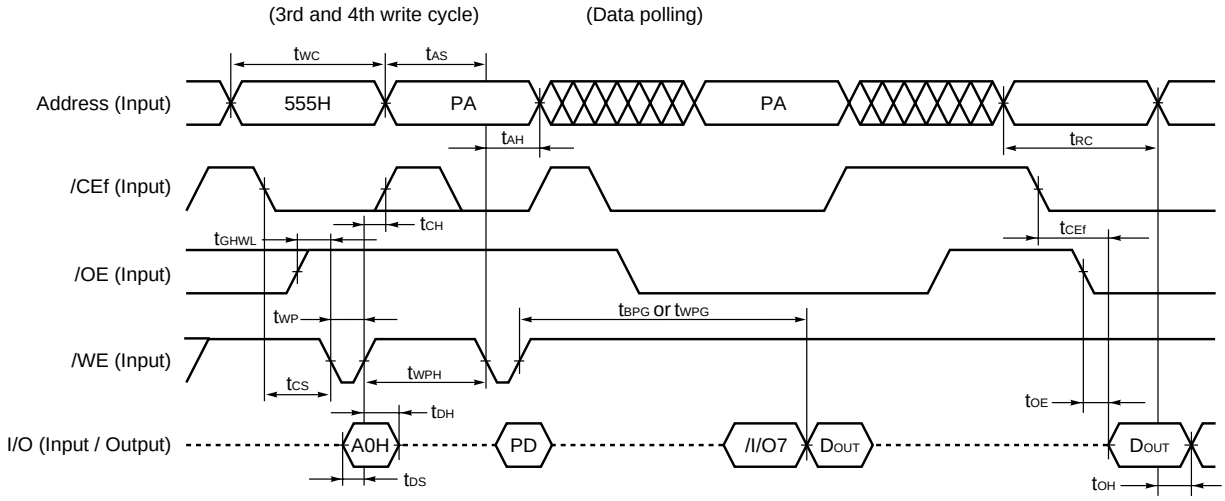


Figure 8. Write Cycle Timing Chart (/WE Controlled) (Flash Memory)

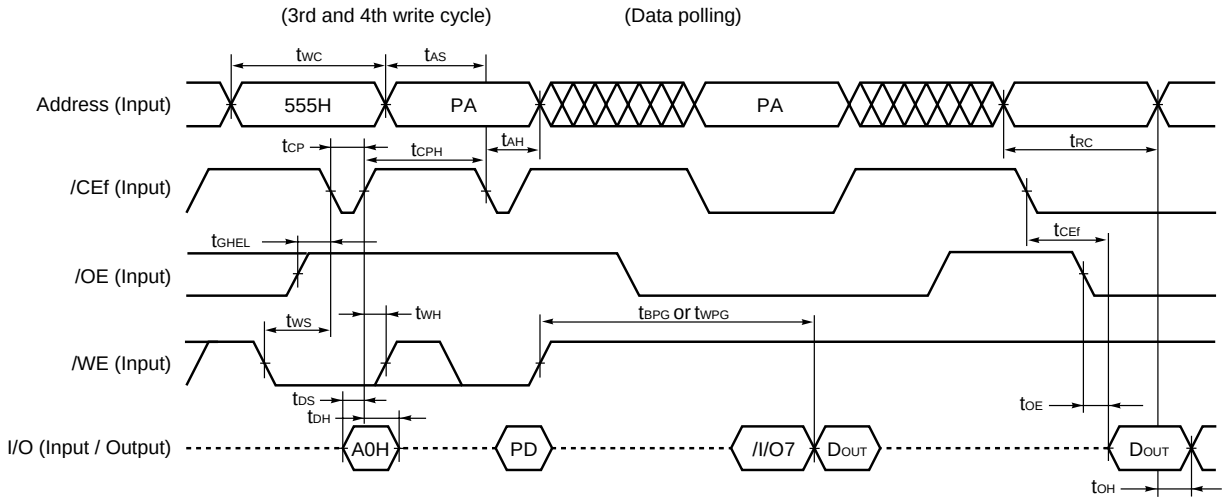


Remarks 1. This timing chart shows the last two write cycles among the program command sequence's four write cycles, and data polling.

2. This timing chart shows the WORD mode's case. In the BYTE mode, address to be input are different from the WORD mode. See **Command Sequence (Flash Memory)**.

3. PA : Program address
PD : Program data
/I/O7 : The output of the complement of the data written to the device.
DOUT : The output of the data written to the device.

Figure 9. Write Cycle Timing Chart (/CEf Controlled) (Flash Memory)

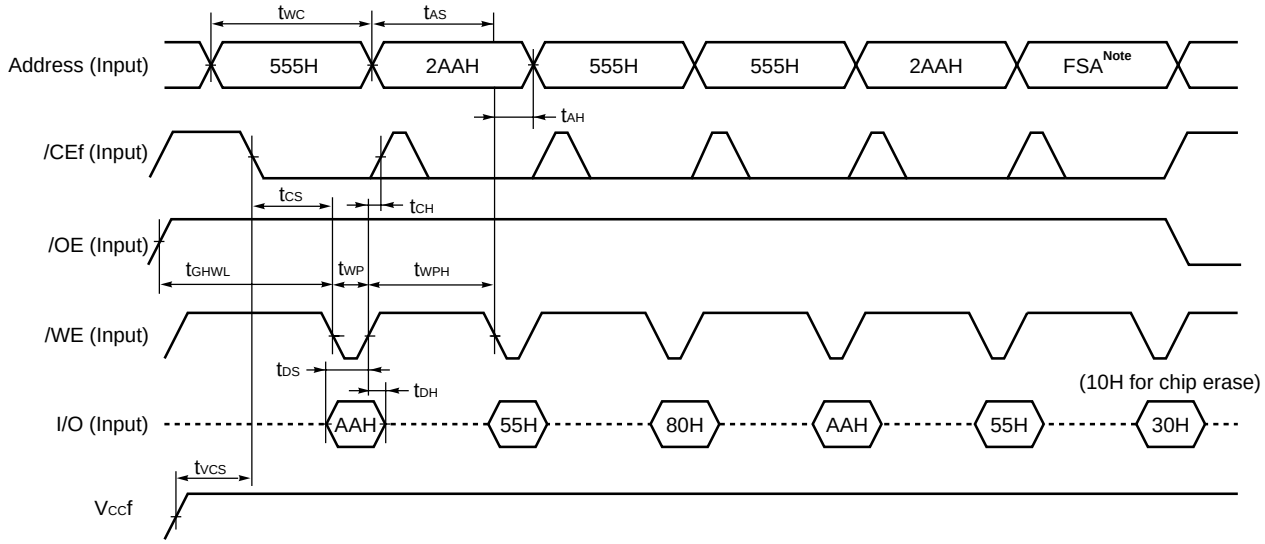


Remarks 1. This timing chart shows the last two write cycles among the program command sequence's four write cycles, and data polling.

2. This timing chart shows the WORD mode's case. In the BYTE mode, address to be input are different from the WORD mode. See **Command Sequence (Flash Memory)**.

3. PA : Program address
PD : Program data
/I/O7 : The output of the complement of the data written to the device.
DOUT : The output of the data written to the device.

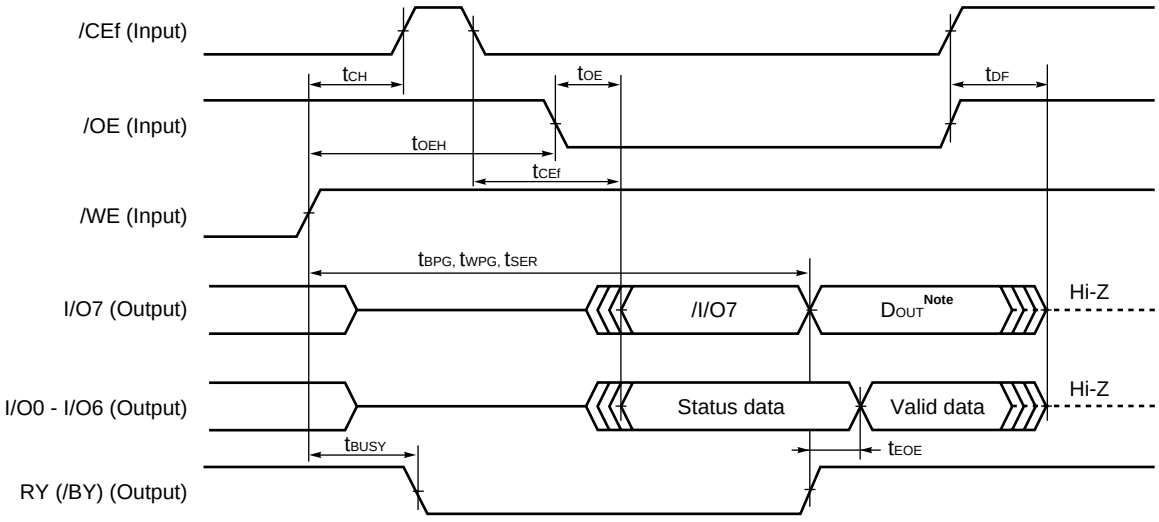
Figure 10. Sector / Chip Erase Timing Chart (Flash Memory)



Note FSA is the sector address to be erased. In the case of chip erase, input 555H (WORD mode), AAAH (BYTE mode).

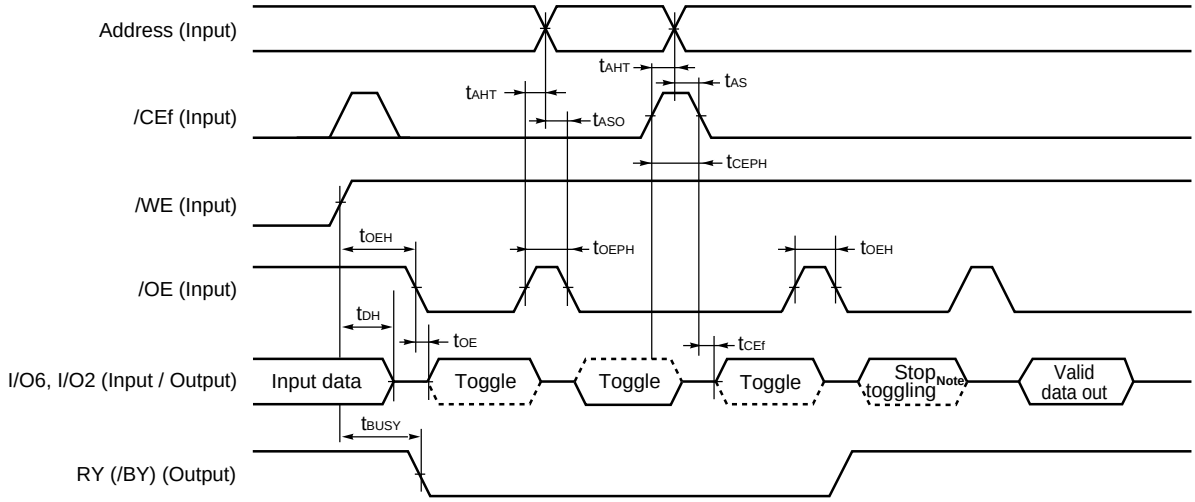
Remark This timing chart shows the WORD mode's case. In the BYTE mode, address to be input are different from the WORD mode. See **Command Sequence (Flash Memory)**..

Figure 11. Data Polling Timing Chart (Flash Memory)



Note I/O7 = D_{OUT} : True value of program data (indicates completion of automatic program / erase)

Figure 12. Toggle Bit Timing Chart (Flash Memory)



Note I/O6 stops the toggle (indicates automatic program / erase completion).

Figure 13. I/O2 vs. I/O6 Timing Chart (Flash Memory)

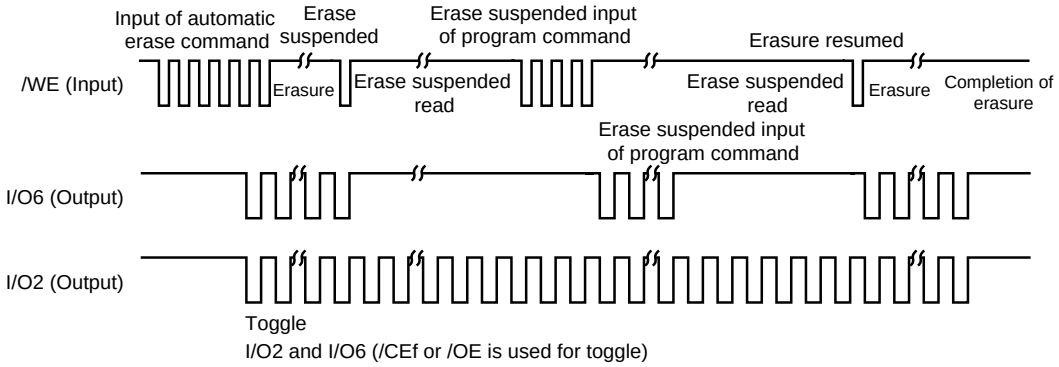


Figure 14. RY (/BY) (Ready / Busy) Timing Chart (Flash Memory)

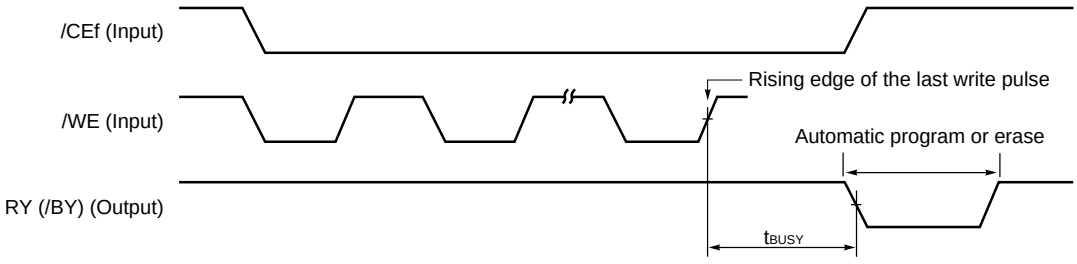


Figure 15. /RESET and RY (/BY) Timing Chart (Flash Memory)

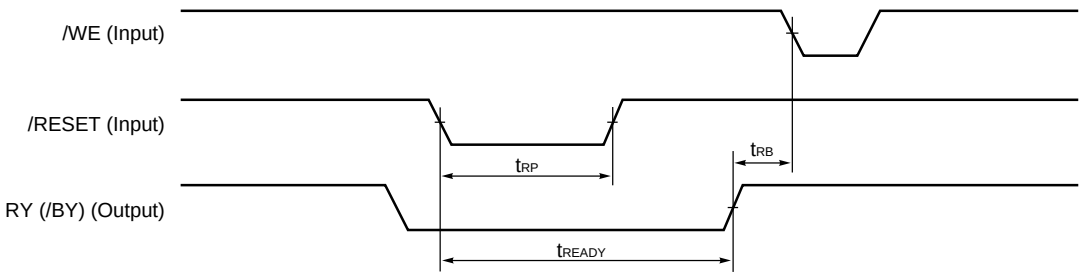
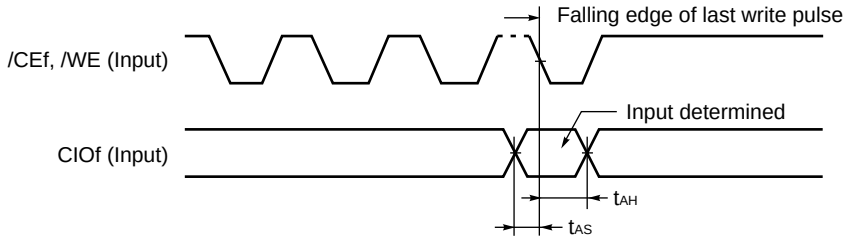
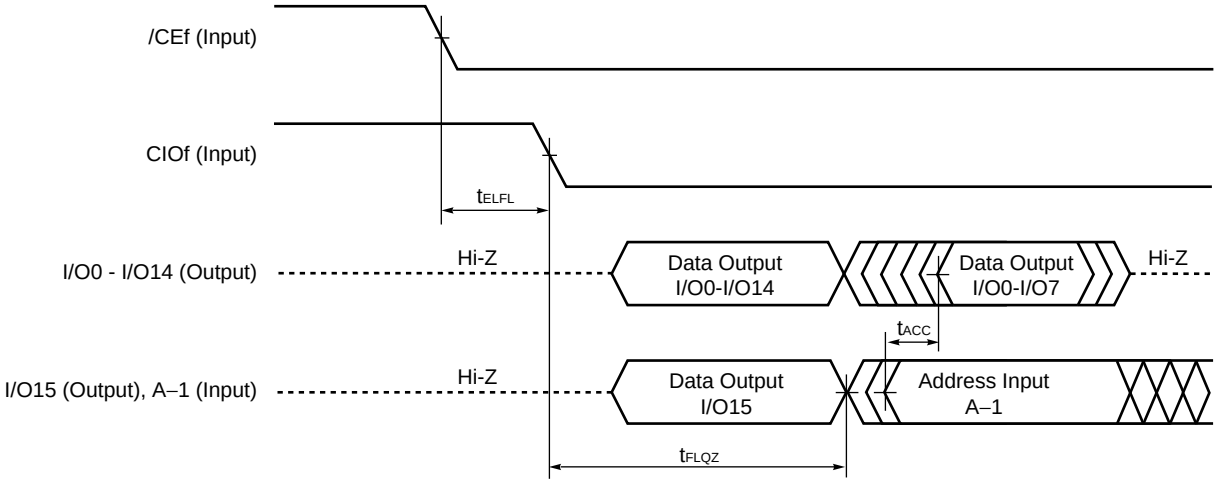


Figure 16. Write CIOf Timing Chart (Flash Memory)



★ **Figure 17. BYTE mode Switching Timing Chart (Flash Memory)**



★ **Figure 18. WORD mode Switching Timing Chart (Flash Memory)**

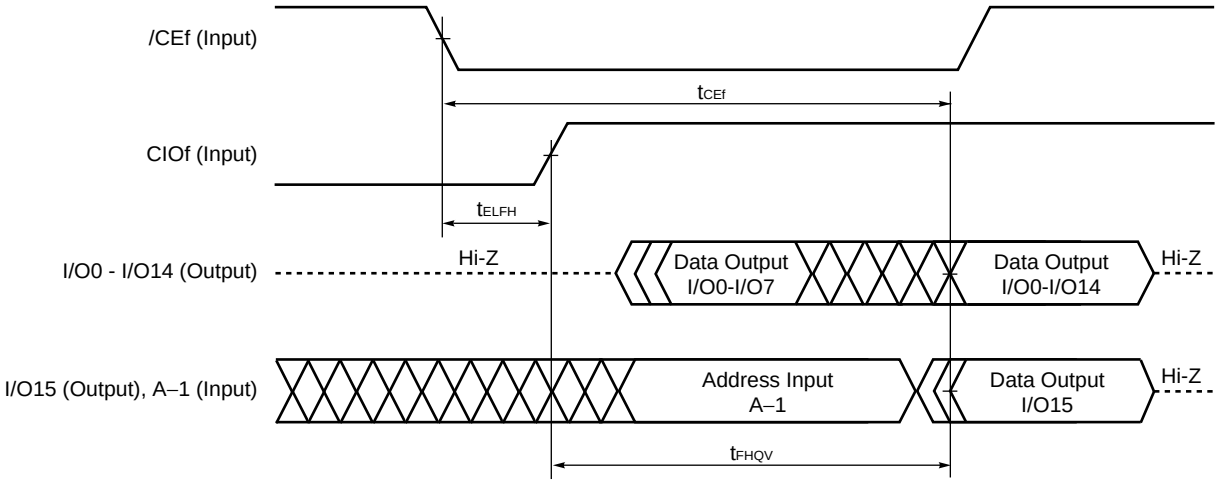
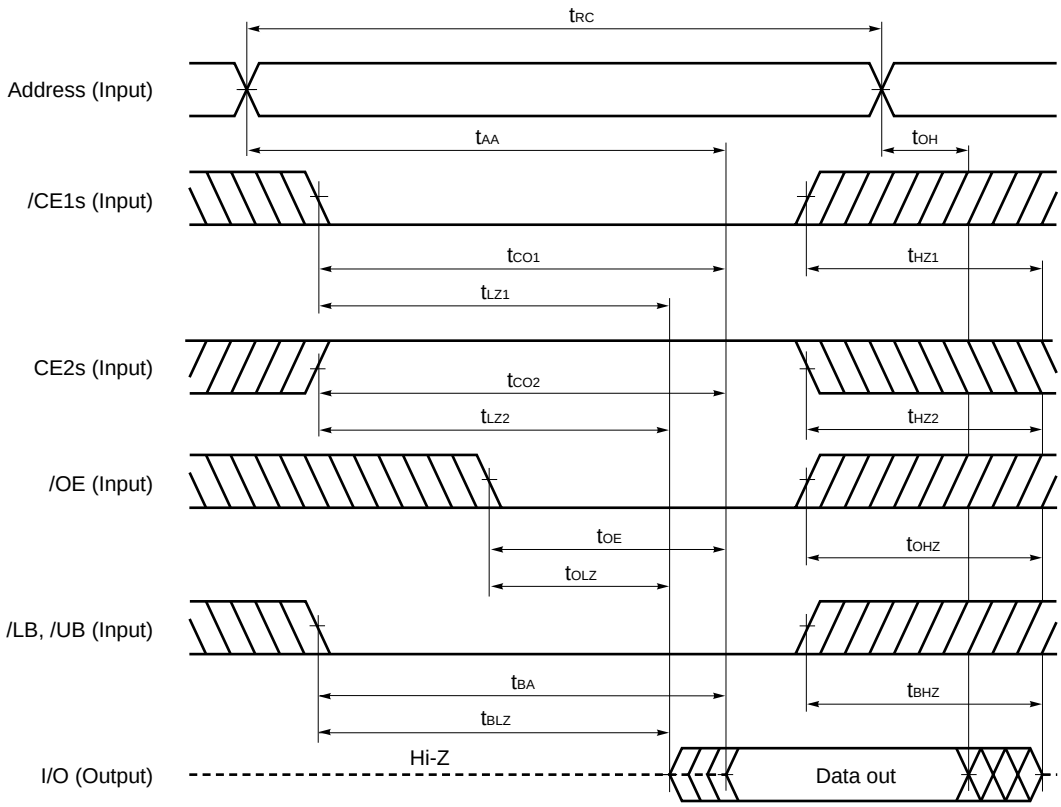
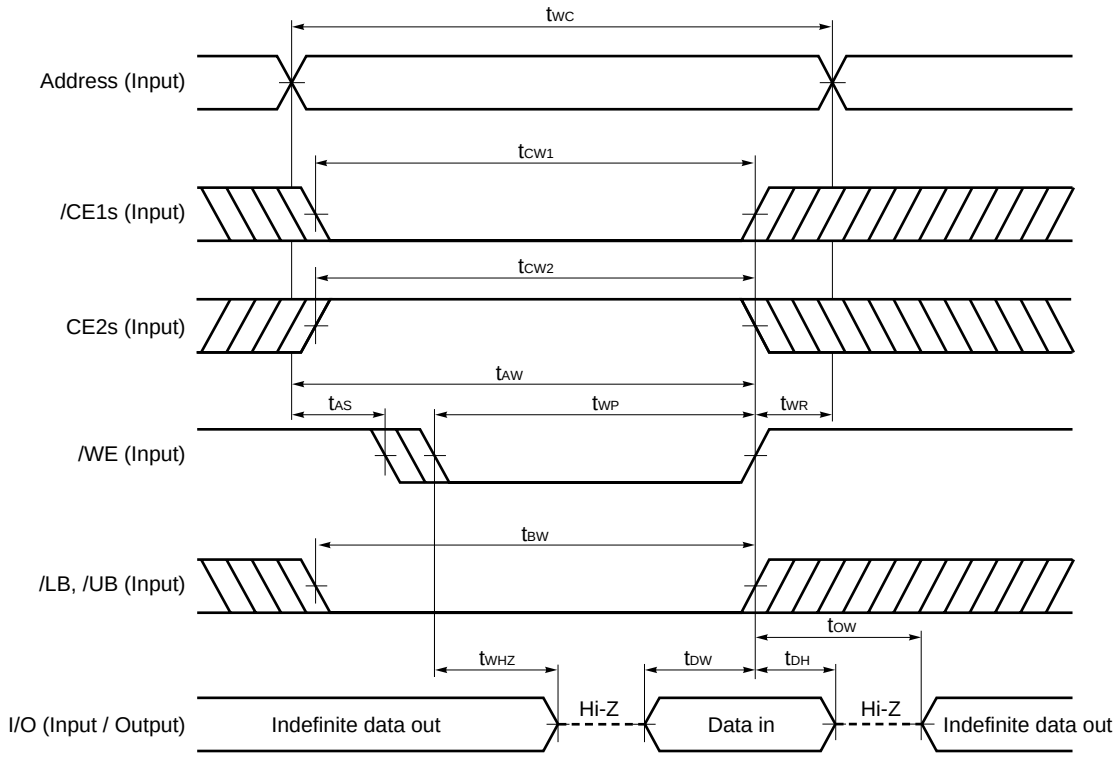


Figure 19. Read Cycle Timing Chart (SRAM)



Remark In read cycle, /WE should be fixed to high level.

Figure 20. Write Cycle Timing Chart 1 (/WE Controlled) (SRAM)



Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

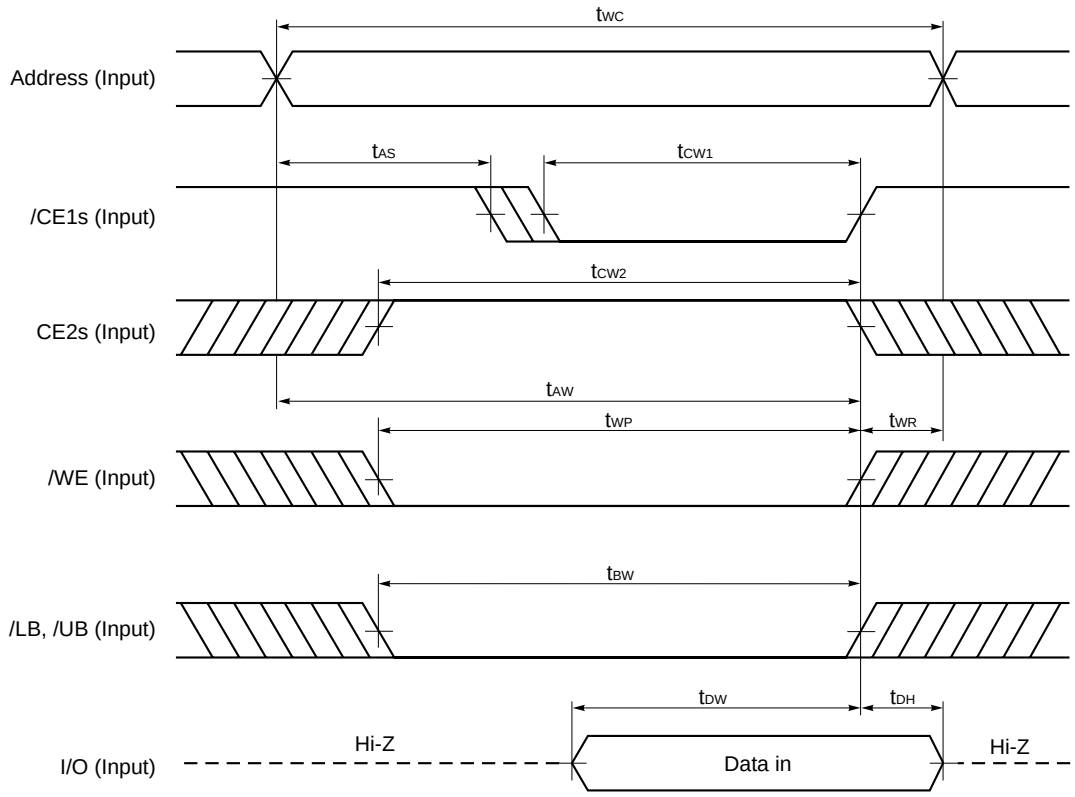
2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

2. If /CE1s changes to low level at the same time or after the change of /WE to low level, or if CE2s changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain Hi-Z state.

3. When /WE is at low level, the I/O pins are always Hi-Z. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins Hi-Z.

Figure 21. Write Cycle Timing Chart 2 (/CE1s Controlled) (SRAM)

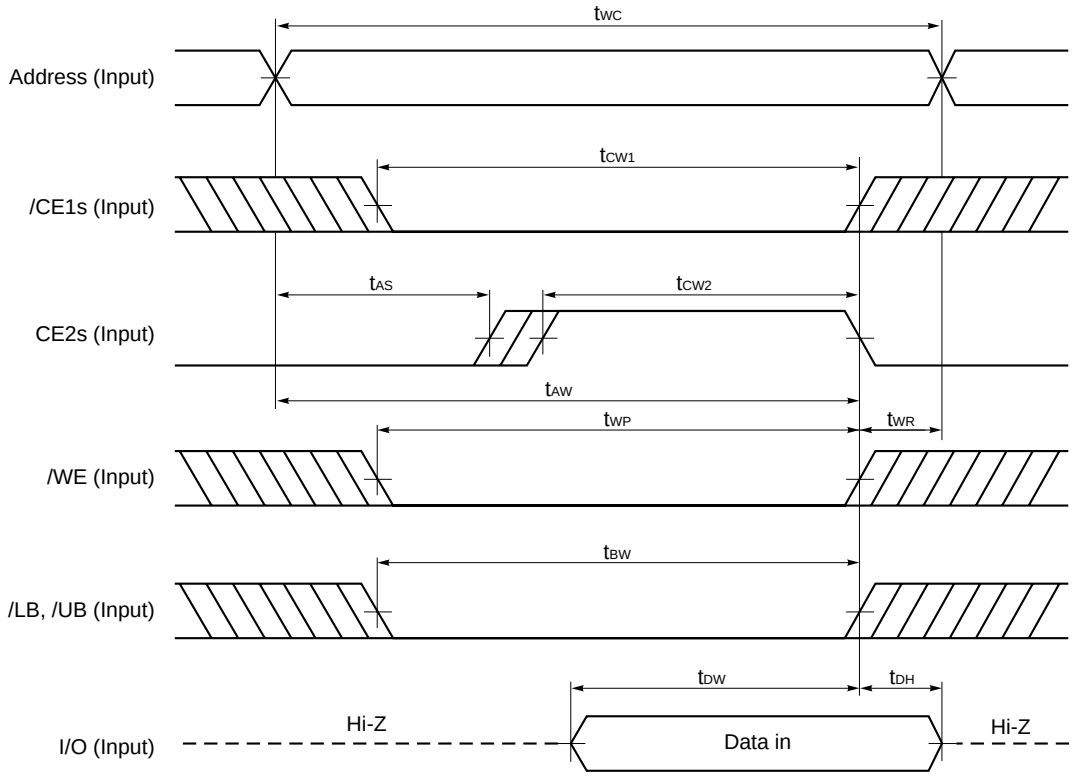


Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

Figure 22. Write Cycle Timing Chart 3 (CE2s Controlled) (SRAM)

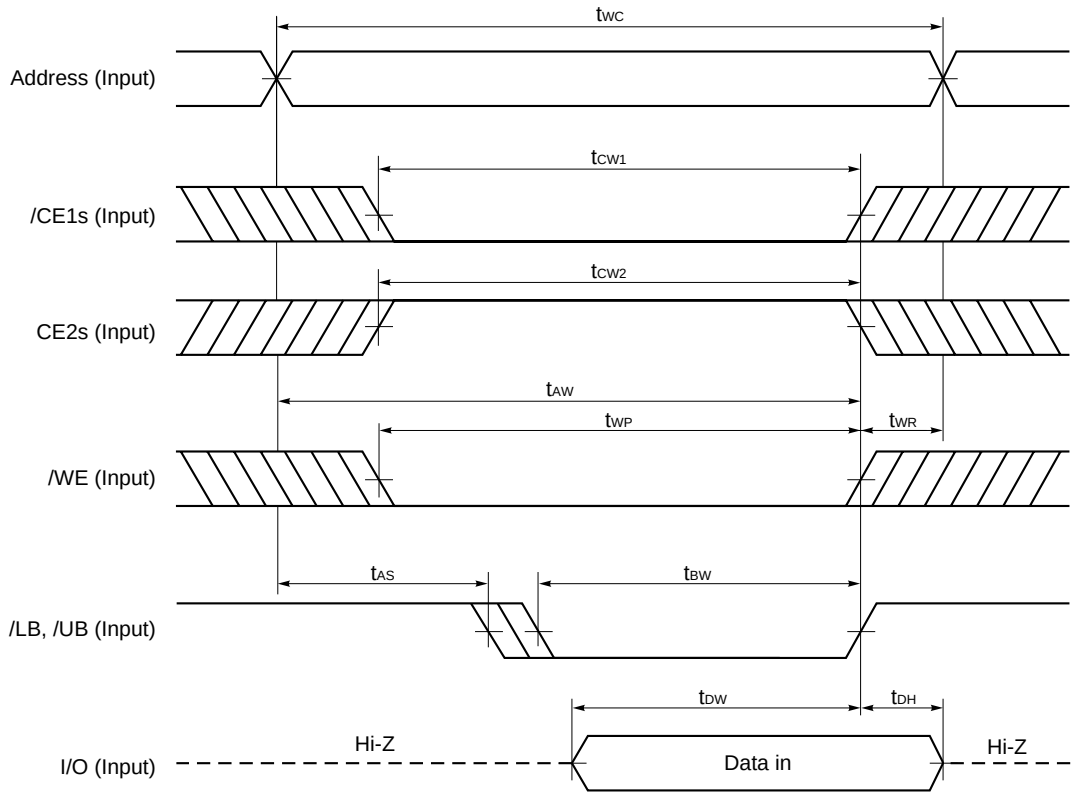


Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

Figure 23. Write Cycle Timing Chart 4 (/LB, /UB Controlled) (SRAM)

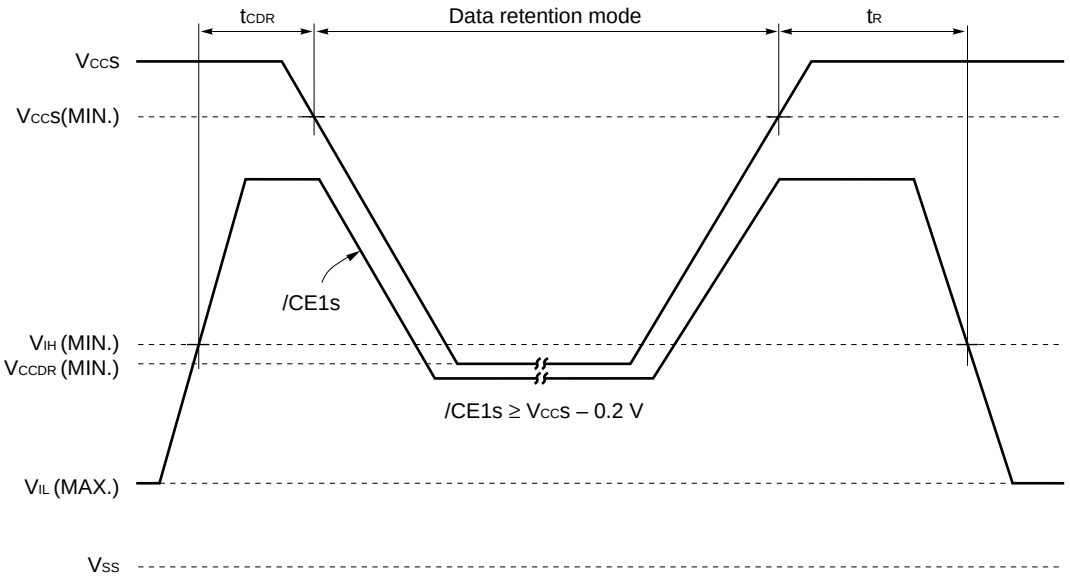


Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

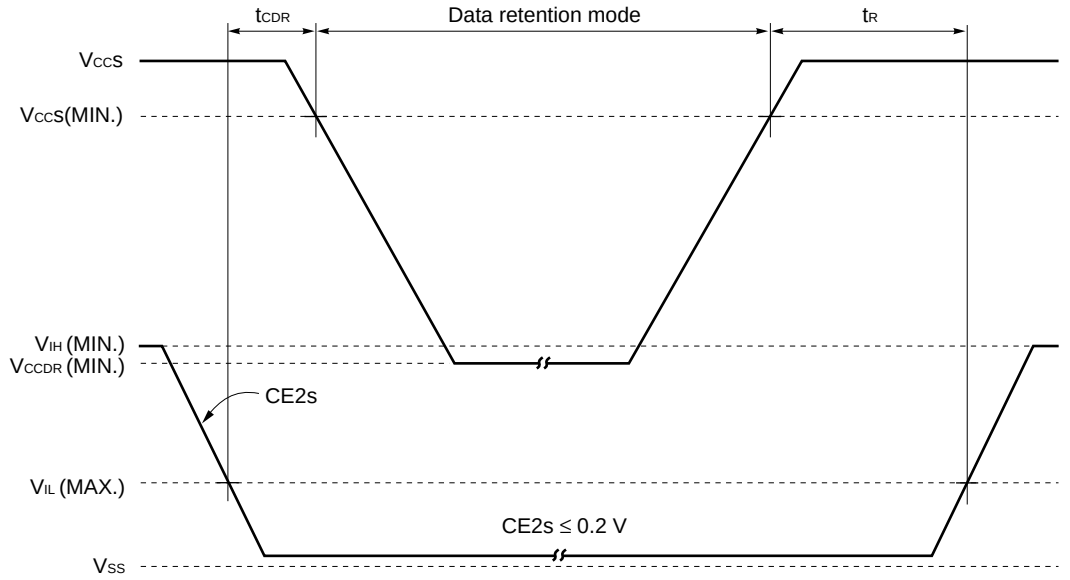
Remark Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

Figure 24. Data Retention Timing Chart 1 (/CE1s Controlled) (SRAM)



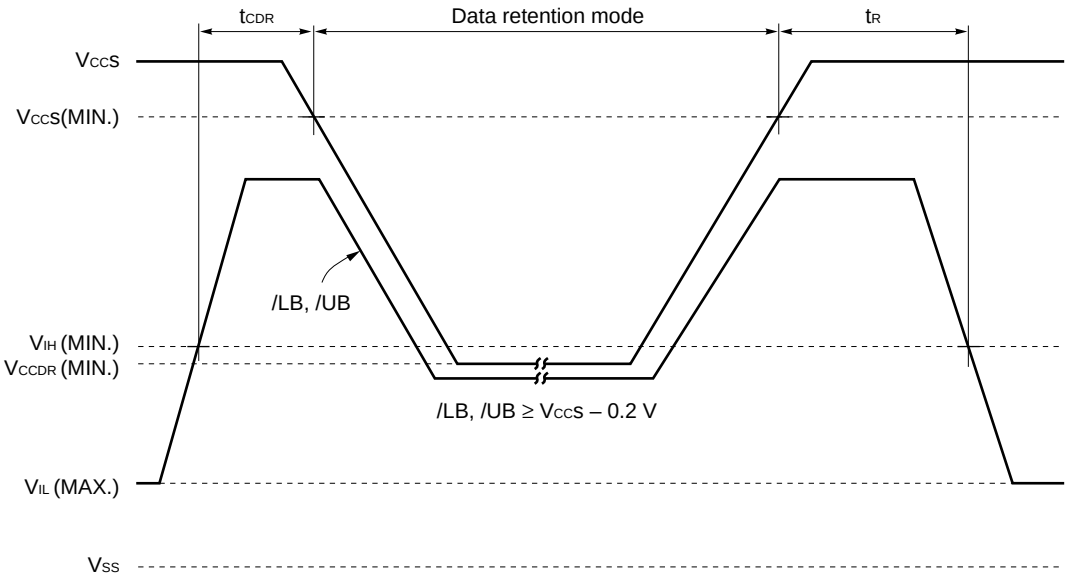
Remark On the data retention mode by controlling /CE1s, the input level of CE2s must be ≥ V_{CCS} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE, /LB, /UB) can be in Hi-Z state.

Figure 25. Data Retention Timing Chart 2 (CE2s Controlled) (SRAM)



Remark On the data retention mode controlling CE2s, the other pins (/CE1s, Address, I/O, /WE, /OE, /LB, /UB) can be in Hi-Z state.

Figure 26. Data Retention Timing Chart 3 (/LB, /UB Controlled) (SRAM)



Remark On the data retention mode by controlling /LB and /UB, the input level of /CE1s and CE2s must be ≥ V_{CCS} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in Hi-Z state.

★ **Flow Charts (Flash Memory)**

Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

CFI Code List

(1/2)

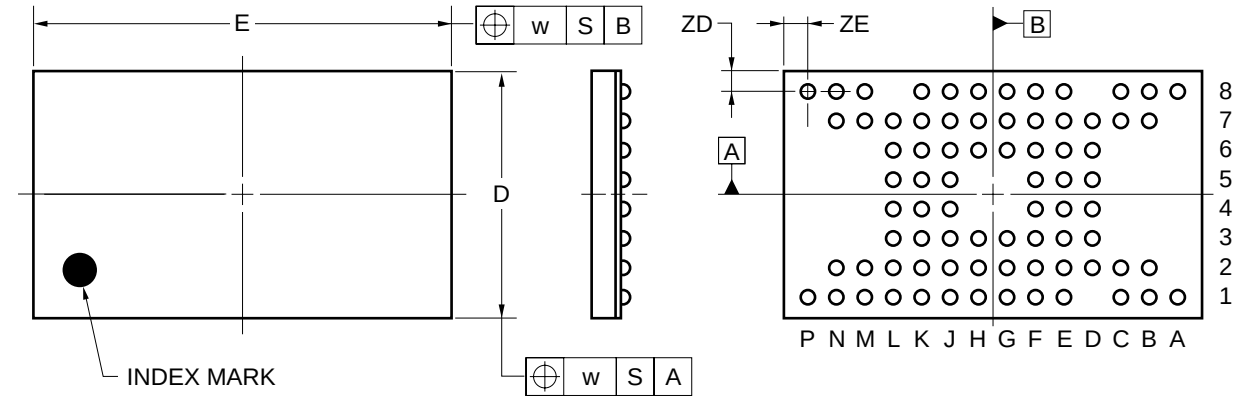
Address A6 to A0	Data I/O15 to I/O0	Description
10H	0051H	"QRY" (ASCII code)
11H	0052H	
12H	0059H	
13H	0002H	Main command set
14H	0000H	2 : AMD/FJ standard type
15H	0040H	Start address of PRIMARY table
16H	0000H	
17H	0000H	Auxiliary command set
18H	0000H	00H : Not supported
19H	0000H	Start address of auxiliary algorithm table
1AH	0000H	
1BH	0027H	Minimum V_{CC}f voltage (program / erase)
		I/O7 to I/O4 : 1 V/bit
		I/O3 to I/O0 : 100 mV/bit
1CH	0036H	Maximum V_{CC}f voltage (program / erase)
		I/O7 to I/O4 : 1 V/bit
		I/O3 to I/O0 : 100 mV/bit
1DH	0000H	Minimum V_{PP} voltage
1EH	0000H	Maximum V_{PP} voltage
1FH	0004H	Typical word program time (2^N μs)
20H	0000H	Typical buffer program time (2^N μs)
21H	000AH	Typical sector erase time (2^N ms)
22H	0000H	Typical chip erase time (2^N ms)
23H	0005H	Maximum word program time (typical time $\times$ 2^N)
24H	0000H	Maximum buffer program time (typical time $\times$ 2^N)
25H	0004H	Maximum sector erasing time (typical time $\times$ 2^N)
26H	0000H	Maximum chip erasing time (typical time $\times$ 2^N)
27H	0016H	Capacity (2^N Bytes)
28H	0002H	I/O information
29H	0000H	2 : $\times$8/$\times$16-bit organization
2AH	0000H	Maximum number of bytes when two banks are programmed (2^N)
2BH	0000H	
2CH	0002H	Type of erase block
2DH	0007H	Information about erase block 1
2EH	0000H	Bit0 to 15 : y = number of sectors
2FH	0020H	Bit16 to 31 : z = size
30H	0000H	(Z $\times$ 256 Bytes)

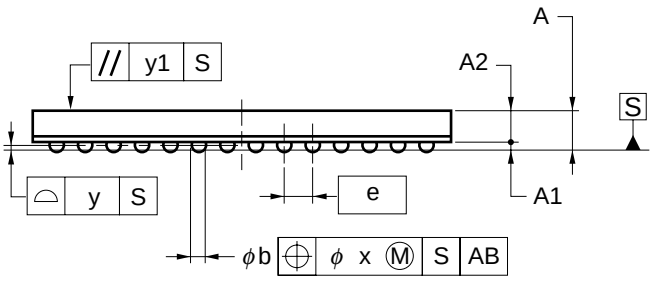
(2/2)

Address A6 to A0	Data I/O15 to I/O0	Description
31H	003EH	Information about erase block 2
32H	0000H	bit0 to 15 : y = number of sectors
33H	0000H	bit16 to 31 : z = size
34H	0001H	(z × 256 Bytes)
40H	0050H	"PRI" (ASCII code)
41H	0052H	
42H	0049H	
43H	0031H	Main version (ASCII code)
44H	0032H	Minor version (ASCII code)
45H	0000H	Address during command input 00H : Necessary 01H : Unnecessary
46H	0002H	Temporary erase suspend function 00H : Not supported 01H : Read only 02H : Read / Program
47H	0001H	Sector group protection 00H : Not supported 01H : Supported
48H	0001H	Temporary sector group protection 00H : Not supported 01H : Supported
49H	0004H	Sector group protection algorithm
4AH	00xxH	Number of sectors of bank 2 00H : Not supported 30H : MC-222263-X
4BH	0000H	Burst mode 00H : Not supported
4CH	0000H	Page mode 00H : Not supported
4DH	0085H	Minimum V_{ACC} voltage I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
4EH	0095H	Maximum V_{ACC} voltage I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
4FH	00xxH	Boot organization 03H : Top boot
50H	0001H	Temporary program suspend function 00H : Not supported 01H : Supported

Package Drawing

77-PIN TAPE FBGA (12x7)





ITEM	MILLIMETERS
D	7.0±0.1
E	12.0±0.1
w	0.2
A	1.1±0.1
A1	0.26±0.05
A2	0.84
e	0.8
b	0.45±0.05
x	0.08
y	0.1
y1	0.1
ZD	0.7
ZE	0.8

P77F9-80-BT3

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the MC-222263-X.

Type of Surface Mount Device

MC-222263F9-B85X-BT3 : 77-pin TAPE FBGA (12 × 7)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related Documents

Document Name	Document Number
DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information	M14914E

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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