Ultrasensitive Hall Effect Latch with Internally or Externally Controlled Sample and Sleep Periods for Track Ball and Scroll Wheel Applications

Last Time Buy

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: December 3, 2013

Deadline for receipt of LAST TIME BUY orders: May 30, 2014

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

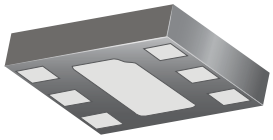
Ultrasensitive Hall Effect Latch with Internally or Externally Controlled Sample and Sleep Periods for Track Ball and Scroll Wheel Applications

Features and Benefits

- Micro-power latch operation
- 1.65 to 3.5 V battery operation
- Push-pull output eliminates the need for an external pull-up resistor
- User configured, internally or externally controlled sample and sleep periods
  - Floating the two clock pins results in the use of a fixed sampling clock internal to the device
  - Toggling the clock pins allows the user to control the sampling and sleep times of the device for extreme low power operation
- External control of the clock pins allows the user to implement synchronous sampling of multiple sensors in direction detection systems
- Chopper stabilization
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- Solid state reliability
- Small size

Package: 6-contact MLP/DFN (suffix EW)

1.5 mm × 2 mm × 0.40 mm



Not to scale

Description

The A1174 is a micro-power, Hall-effect latch for use in portable devices that employ rotational detection systems, and have a power supply voltage between 1.65 and 3.5 V. The device has a single push-pull output structure and requires no external pull-up resistor for reliable operation.

When a sufficient positive magnetic field is present on the device, the device output transitions to the low state and is latched in this state until a negative field of sufficient strength latches the device output into the high state. The latched output is ideal when using multiple sensors in rotational speed and direction sensing systems (for example, track ball and scroll bar systems in portable devices).

The device includes an innovative clocking scheme that satisfies the micro-power needs of almost any application, including track balls for PDAs and cell phones. Using the EXTERNAL_CLK and DUAL_CLK pins as described in this datasheet, the device can be set into various working modes.

In Dual Clock mode, the device switches between predefined slow and fast sampling rates. The average current consumption of the device is extremely low when rotation is not detected. In External Clock mode, the user sets the clock rate for the device to achieve the required on and off times for controlling average power. This user-determined clocking also helps to

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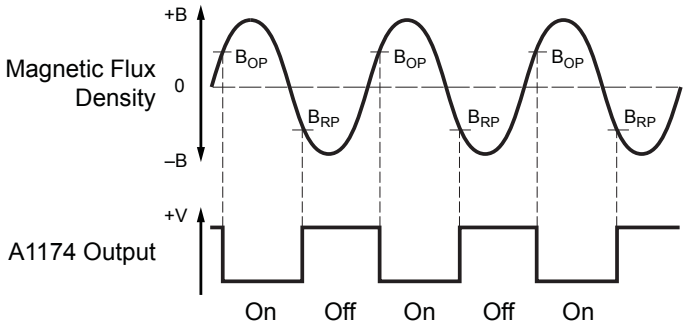


Figure 1. Timing diagram for output switching

Description (continued)

achieve synchronous clocking of multiple devices. This allows a defined phase relationship between the output transitions of each device in direction detection systems.

Improved stability is made possible through dynamic offset cancellation using chopper stabilization, which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress. Solid state reliability is provided by integrating, on a single silicon chip, a Hall-voltage generator, a small-signal amplifier, chopper stabilization, a latch, and a MOSFET output.

The device package is a 6-contact, 1.5 mm × 2 mm, 0.40 mm nominal overall height MLP/DFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with NiPdAu leadframe plating.

Selection Guide

Part Number	Package	Packing[1]
A1174EEWLT-P[2]	DFN/MLP 1.5×2 mm; 0.40 mm maximum height	3000 pieces per 7-inch reel

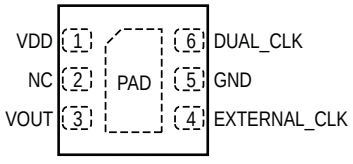
[1]Contact Allegro™ for additional packing options.
2Allegro products sold in DFN package types are not intended for automotive applications.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{DD}		5.0	V
Reverse Supply Voltage	V_{RDD}		–0.3	V
Output Voltage	V_{OUT}		5.0	V
Reverse Output Voltage	V_{ROUT}		–0.3	V
EXTERNAL_CLK and DUAL_CLK Pins Input Voltage	V_{IN}		5.0	V
EXTERNAL_CLK and DUAL_CLK Pins Reverse Input Voltage	V_{RIN}		–0.3	V
Continuous Output Current	$I_{OUT(sink)}$		–1	mA
	$I_{OUT(source)}$		1	mA
Magnetic Flux Density*	B		Unlimited	G
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	T_J(MAX)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

*1G = 0.1 mT (millitesla)

Pin-out Diagram

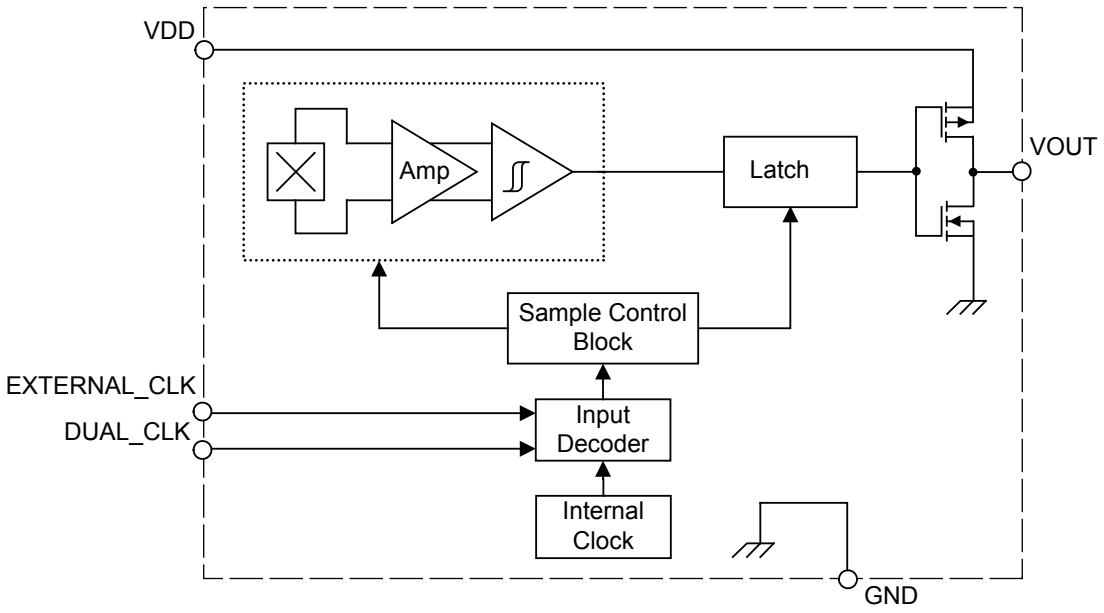


(Top View)

Terminal List

Number	Name	Function
1	VDD	Supply Voltage
2	NC	No connect
3	VOUT	Output
4	EXTERNAL_CLK	In combination with DUAL_CLK, allows external control of the device sampling period and duty cycle
5	GND	Ground
6	DUAL_CLK	In combination with EXTERNAL_CLK, drives the part in Dual Clock mode

Functional Block Diagram



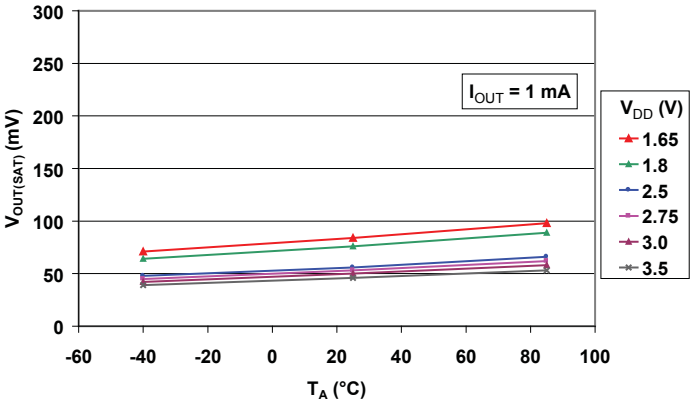
Operating Characteristics Valid over full operating voltage and ambient temperature ranges (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
Electrical Characteristics						
Supply Voltage[2]	V_{DD}	T_A = 25°C	1.65	–	3.5	V
		–40°C ≥ T_A ≥ 85°C	1.8	–	3.5	V
Output On Voltage	$V_{OUT(SAT)}$	NMOS on, I_{OUT} = 1 mA	–	100	300	mV
	$V_{OUT(HIGH)}$	PMOS on, I_{OUT} = 1 mA	V_{DD} – 300	V_{DD} – 100	–	mV
Supply Current	$I_{DD(EN)}$	Chip in awake state (enabled)	–	–	2.0	mA
	$I_{DD(DIS)}$	Chip in sleep state (disabled)	–	–	8.0	µA
	$I_{DD(AV)}$	Normal Clock mode, V_{DD} = 2.5 V	–	–	71	µA
		Normal Clock mode, V_{DD} = 3.0 V	–	–	82	µA
Internal Chopper Stabilization Clock Frequency	f_C		–	200	–	kHz
EXTERNAL_CLK and DUAL_CLK Pins Input Current	I_{IN}	$V_{EXTERNAL\_CLK} = V_{DD}$, $V_{DUAL\_CLK} = V_{DD}$	–	0.5	–	µA
EXTERNAL_CLK and DUAL_CLK Pins Leakage Current	I_{OFF}	$V_{EXTERNAL\_CLK} = 0$ V, $V_{DUAL\_CLK} = 0$ V	–	0.02	–	µA
Supply Slew Rate[3]	SR	t_{OFF} = 100 ms	0.1	–	–	V/ms
Normal Clock Mode Characteristics[4]						
Normal Mode Awake Duration	t_{awake_norm}		–	25	46	µs
Normal Mode Period	t_{period_norm}		–	0.7	1.05	ms
External Clock Mode Characteristics[4]						
EXTERNAL_CLK and DUAL_CLK Pins Threshold	$V_{th(HIGH)}$		–	–	$0.75 \times V_{DD}$	V
	$V_{th(LOW)}$		$0.25 \times V_{DD}$	–	–	V
External Clock Mode Awake Duration	t_{awake_ext}	$V_{EXTERNAL\_CLK} > V_{th(HIGH)}$	46	–	–	µs
External Clock Mode Period	t_{period_ext}	$V_{EXTERNAL\_CLK} > V_{th(HIGH)}$	80	–	–	µs
State Transition Delay[5]	t_{delay_ext}		–	25	46	µs
Dual Clock Mode Characteristics[4]						
Dual Clock Mode Awake Duration	t_{awake_dual}		–	25	46	µs
Dual Clock Mode Fast Sampling Period	t_{period_fast}		–	$8 \times t_{awake\_dual}$	–	µs
Dual Clock Mode Slow Sampling Period	t_{period_slow}		–	28	–	ms
Dual Clock Mode Timeout[6]	$t_{timeout}$		–	$100 \times t_{period\_slow}$	–	ms
Magnetic Characteristics[2]						
Operate Point	B_{OP}	South pole to device branded side	5	36	55	G
Release Point	B_{RP}	North pole to device branded side	–55	–36	–5	G
Hysteresis	B_{HYS}	$B_{OP} - B_{RP}$	–	72	110	G

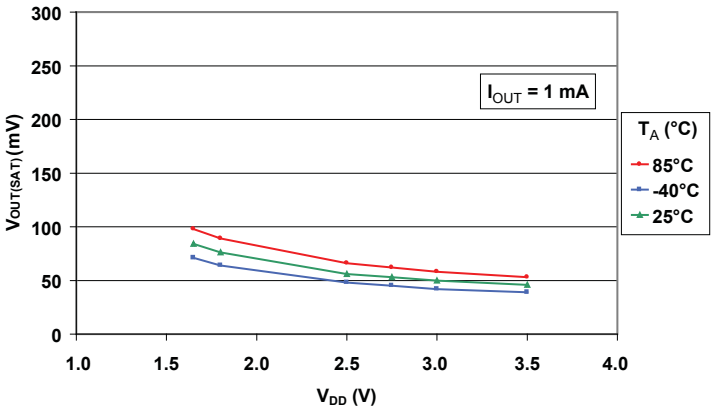
[1]Typical values are at T_A = 25°C and V_{DD} = 2.75 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]Magnetic operate and release points vary with supply voltage.
[3]If the device power supply is chopped, power-up slew rate dV_{DD} / dt has to be adjusted to ensure correct functioning of the device. t_{OFF} is the time of the power cycle when $V_{DD} < V_{DD}$(min).
[4]Defined in the Functional Description section of this datasheet.
[5]Time between external clock transition and resulting transition of the device between the awake and sleep states. See Functional Description section.
[6]If no output transition is detected during the timeout interval, the device goes back into slow sampling. See Functional Description section.

Characteristic Performance

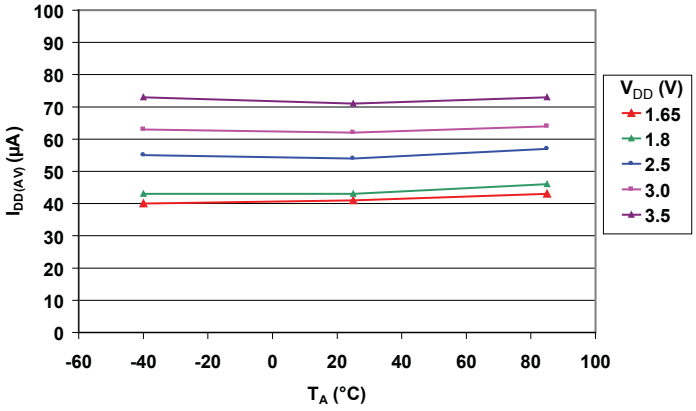
Saturation Voltage versus Temperature



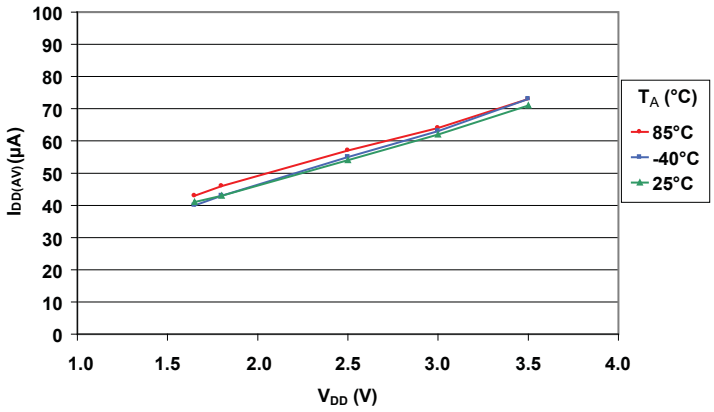
Saturation Voltage versus Supply Voltage



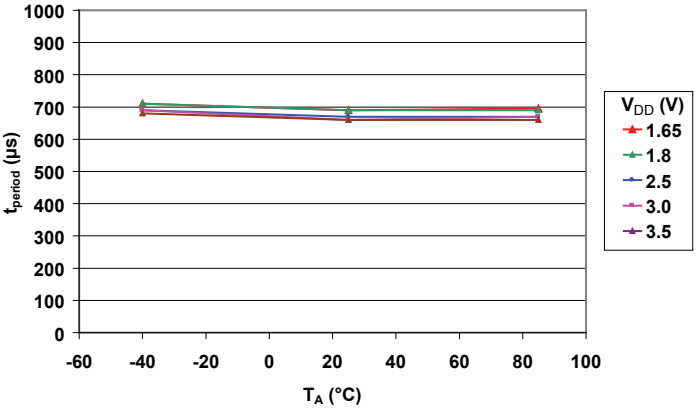
Average Supply Current versus Temperature



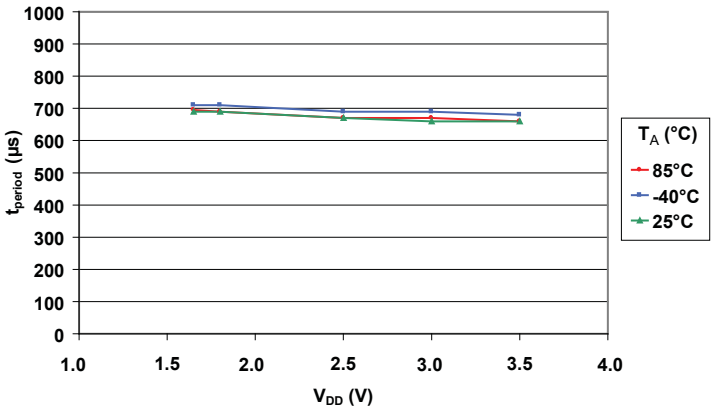
Average Supply Current versus Supply Voltage



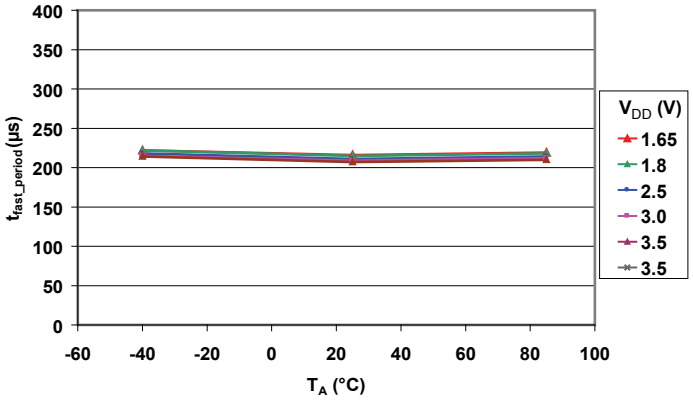
Normal Mode Period versus Temperature



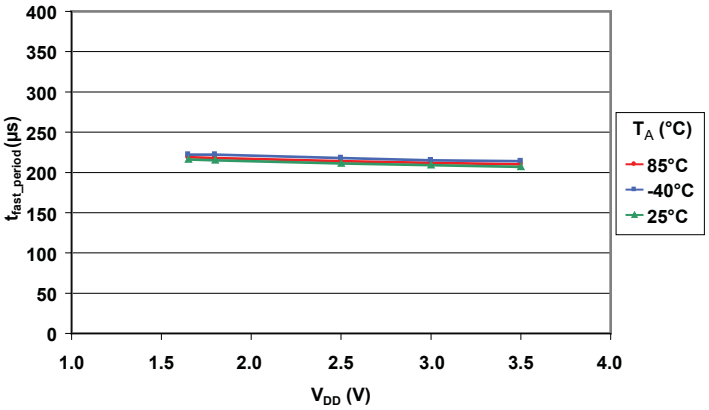
Normal Mode Period versus Supply Voltage



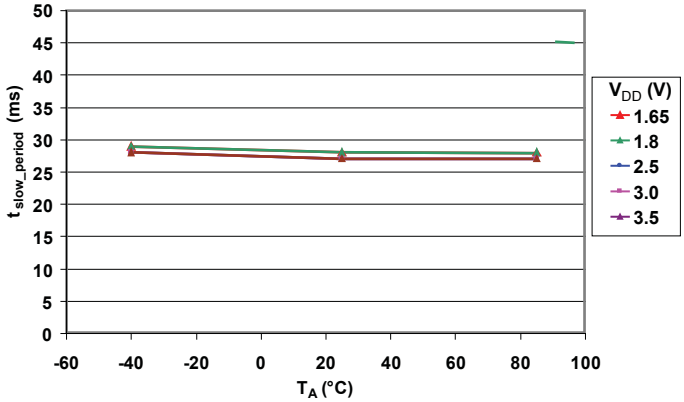
Dual Mode Fast Period versus Temperature



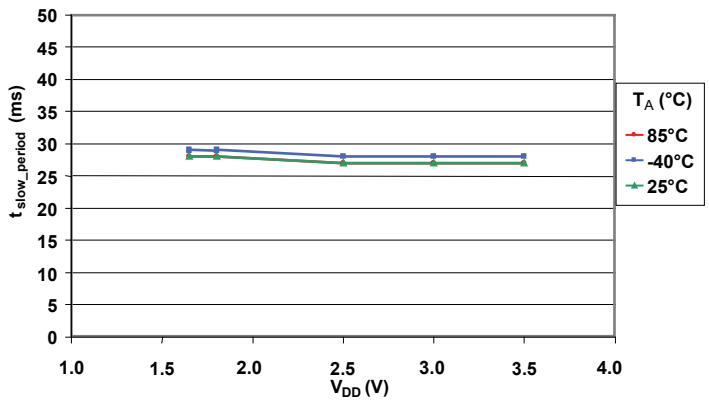
Dual Mode Fast Period versus Supply Voltage



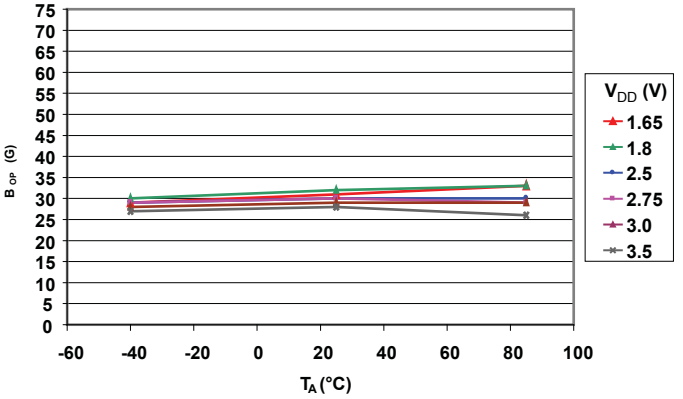
Dual Mode Slow Period versus Temperature



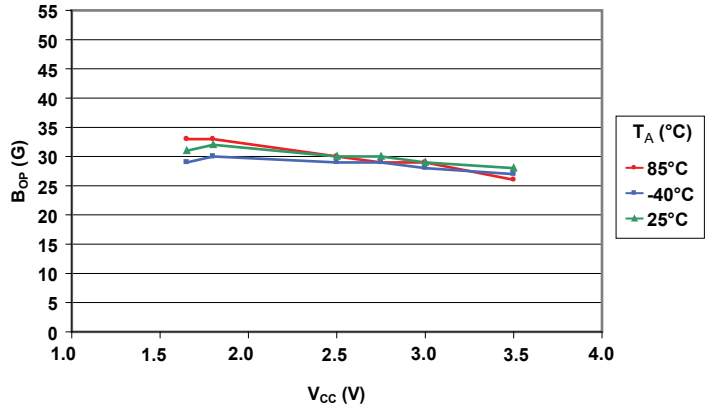
Dual Mode Slow Period versus Supply Voltage



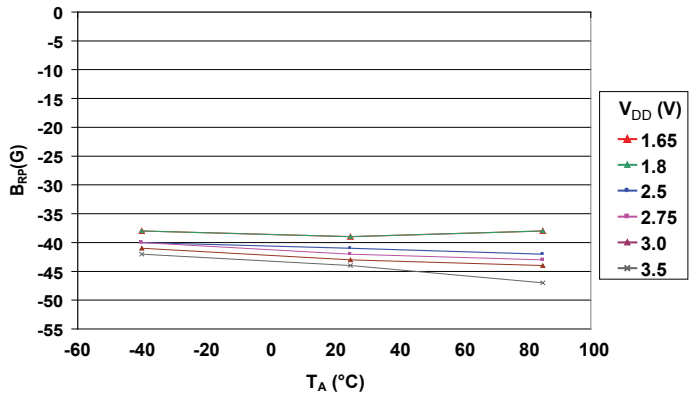
Operate Point versus Temperature



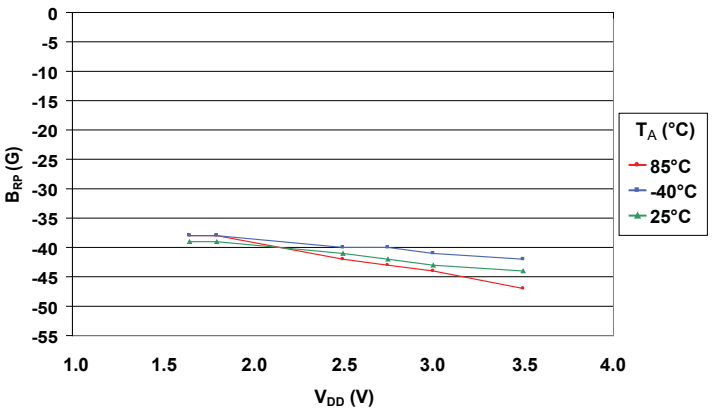
Operate Point versus Supply Voltage



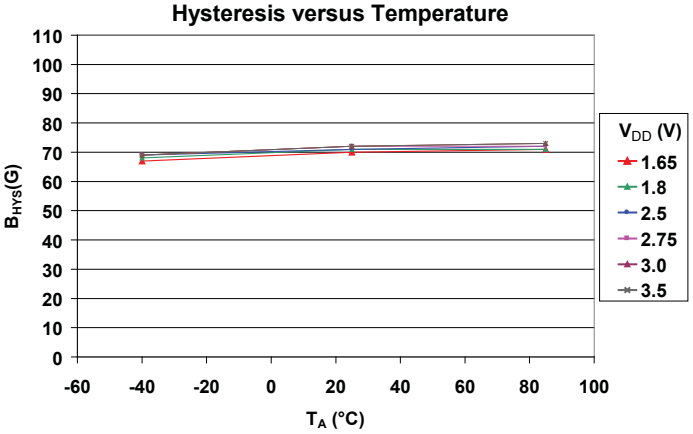
Release Point versus Temperature



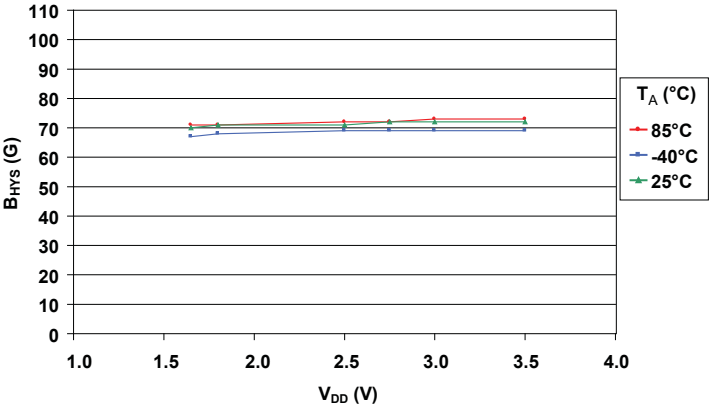
Release Point versus Supply Voltage



Hysteresis versus Temperature



Hysteresis versus Supply Voltage



Functional Description

Output State Operation

The output state (VOUT pin) of this device switches to low (on) when an incident magnetic field, perpendicular to the Hall element, exceeds the operate point threshold, B_{OP}. After turn-on, the output voltage is $V_{OUT(SAT)}$ (see figure 2). When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (off), $V_{OUT(HIGH)}$. The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Removal of the magnetic field leaves the device output latched low (on) if the last crossed switchpoint is B_{OP}, or latched high (off) if the last crossed switchpoint is B_{RP}.

Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) gives an indeterminate output state. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

Micro-power Operation

Micro-power operation of the device involves duty cycle control achieved by:

- powering all circuits in the chip and latching the device output state at the end of awake state periods, and
- turning off the bias current to most circuits in the chip and maintaining the device output state through sleep state periods.

This is illustrated in figure 3. The awake state duration, t_{awake_x}, is common in all defined modes of operation. The sleep state duration is set at a longer duration than the awake period in order to conserve power. During the sleep state, current consumption is insignificant (equal to $I_{DD(DIS)}$), but the device output does not switch in response to changing incident magnetic fields.

The device shows maximum current consumption, $I_{DD(EN)}$, during the awake state and minimal current consumption, $I_{DD(DIS)}$, during the sleep state. Average current, $I_{DD(AV)}$, for micro-power operation is derived from following formula:

$$I_{DD(AV)} = \frac{I_{DD(EN)} \times t_{awake\_x} + I_{DD(DIS)} \times t_{sleep\_x}}{t_{period\_x}} \quad .$$

Three micro-power control modes are available:

- Normal Clock mode
- External Clock mode
- Dual Clock mode

Selection of clock mode is determined by the configuration of the EXTERNAL_CLK pin and the DUAL_CLK pin, and applied voltages as illustrated in figure 4 and table 1.

Normal Clock Mode When both device clock pins are left floating or are grounded, the internal timing circuitry activates the device for t_{awake_norm} and deactivates it for the remainder, t_{sleep}, of the duty cycle period, t_{period_norm}. The short awake time

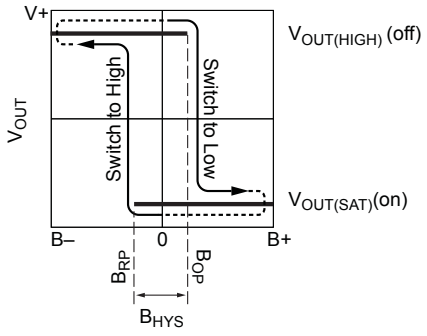


Figure 2. Device output switching logic

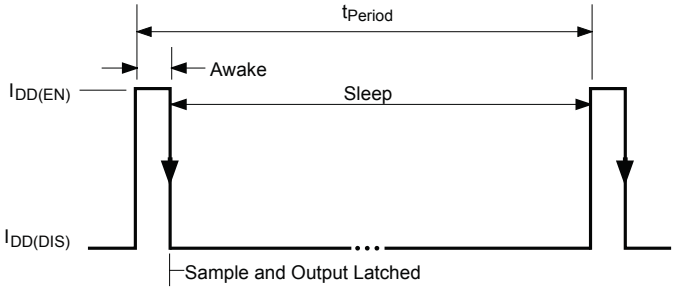


Figure 3. Micro-power behavior of the device

allows stabilization prior to the IC sampling and data latching on the falling edge of the timing pulse. The output during the sleep time, t_{sleep}, is latched in the last sampled state.

External Clock Mode Applying a voltage greater than $V_{th(HIGH)}$ to both clock pins puts the device into the awake state (without automatic cycling through the sleep state). The device uses the maximum defined supply current, reaching maximum power consumption.

Applying a voltage greater than $V_{th(HIGH)}$ to the EXTERNAL_CLK pin and a voltage lower than $V_{th(LOW)}$ to the DUAL_CLK pin puts the device into the sleep state (without automatic cycling through the awake state), and latches the device output in the output state determined during the prior awake state.

The duration of the awake and sleep periods can be controlled externally by applying a voltage greater than $V_{th(HIGH)}$ to the EXTERNAL_CLK pin and applying an external clock to the DUAL_CLK pin. The user can define the input sampling time and frequency to reach a target consumption current level, but the minimum sample time must remain longer than t_{awake_ext}. Note that the device should be periodically put into the awake state in order to update the device output state.

State Transition Delay, t_{ext_delay}, appears as the time between an external clock transition and the resulting transition of the device between the awake and the sleep state. This is illustrated in figure 5.

Dual Clock Mode When the EXTERNAL_CLK pin is left floating, or is grounded, and the DUAL_CLK pin is pulled to a voltage greater than $V_{th(HIGH)}$, the device enters Dual Clock mode. Figure 6 gives an overview of the device operation algorithm in Dual Clock mode.

Table 1. Clock Mode Selection Options

Connection		Mode	Description
EXTERNAL_CLK Pin	DUAL_CLK Pin		
Low / NC	Low / NC	Normal Clock	Awake and sleep state durations defined by device internal clock
High	High	External Clock, Awake State	Awake and sleep state durations defined by external clock
	Low	External Clock, Sleep State	
Low / NC	High	Dual Clock	Awake and sleep state durations defined by internal fast or slow clock

High = $V \geq V_{th(HIGH)}$, Low = $V \leq V_{th(LOW)}$, NC = no connect (float or connect to ground)

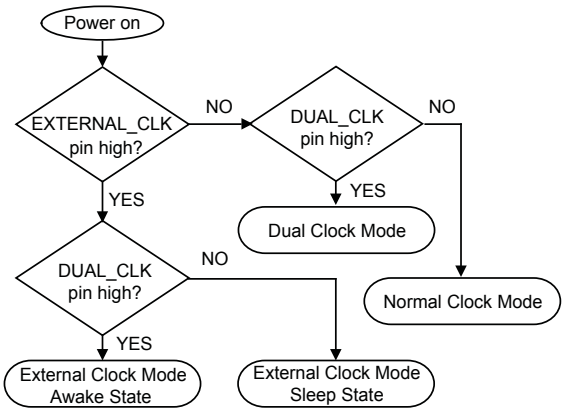


Figure 4. Clock mode selection algorithm; determined by clock pins connections in the application

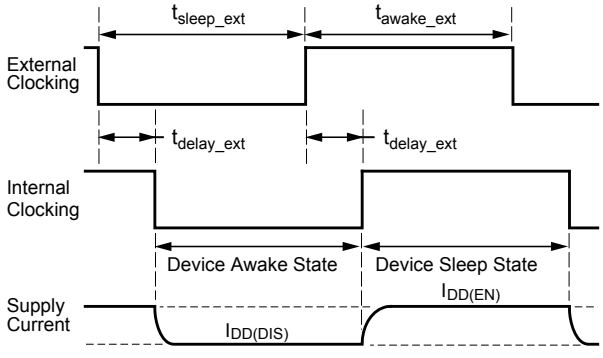


Figure 5. External Clock mode clocking; t_{delay_ext} corresponding to the device transition delay into the awake or sleep states after an external clock transition

Initially, the device operates in the slow sampling state with a typical sleep time duration, t_{sleep_slow}. The awake time duration, t_{awake}, is common in all defined modes of operation. After the first output state transition, the device switches into the fast sampling state, with a sleep time duration, t_{sleep_fast}, of $8 \times t_{awake\_dual}$.

Fast input sampling ensures that the device does not miss any subsequent transitions of the incident magnetic field. This is advantageous in applications such as track ball monitoring, when the track ball can be rotated at very high speeds. If there is no output switching for the duration of the specified timeout, $t_{timeout}$, then the device switches back into the slow sampling state to conserve battery life in handheld devices.

Figure 7 shows the case in which the field does not change within the $t_{timeout}$ period. The behavior of the device in the presence of a rapidly changing magnetic field is shown in figure 8.

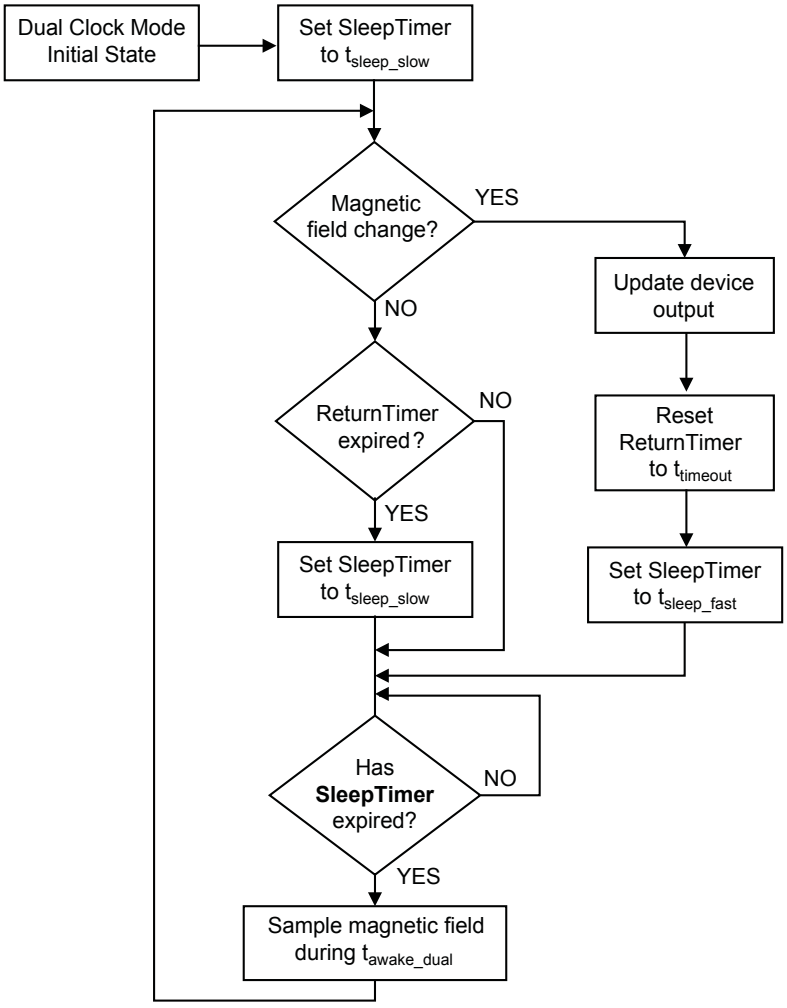


Figure 6. Dual Clock mode operation algorithm

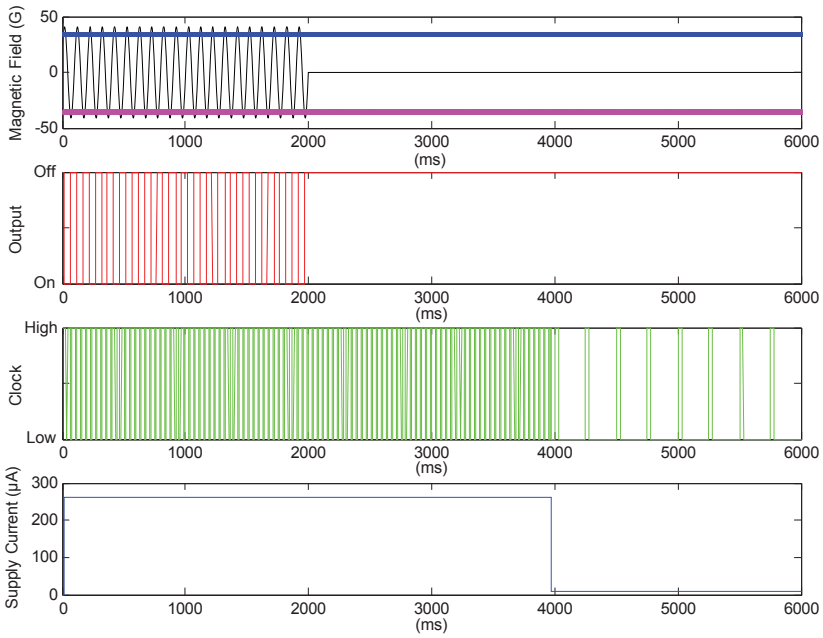


Figure 7. Device output response in Dual Clock mode with no change of the magnetic field for the duration of $t_{timeout}$

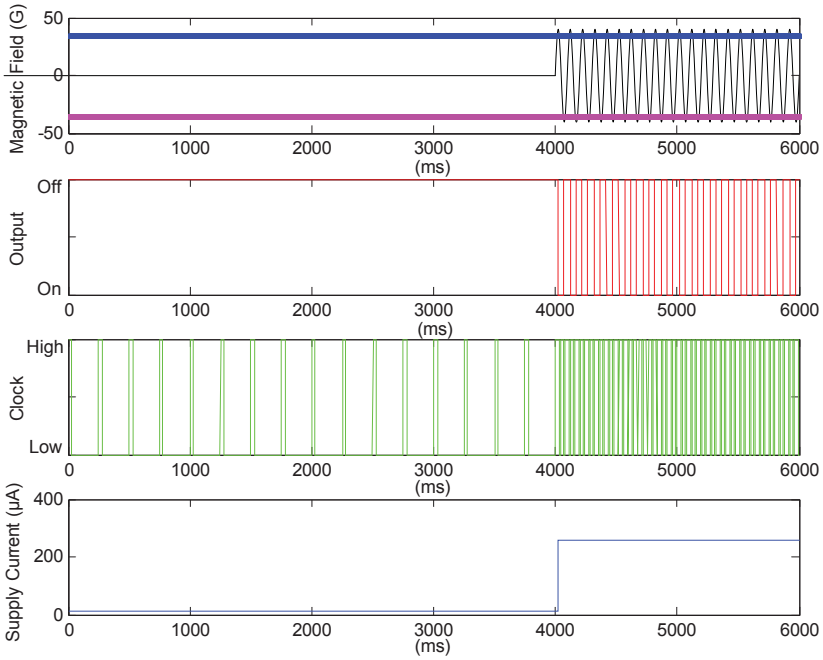


Figure 8. Device output response in Dual Clock mode with a rapid change of the magnetic field

Application Information

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique (0.1 µF is a typical value). Additionally, it is recommended that, when possible, pins be tied to either the VDD pin or ground potential in order to improve the EMC performance of the device. However, it is feasible to float the EXTERNAL_CLK and DUAL_CLK pins in the application. In the case where these pins are floating, care should be taken to locate the device as far as possible from system antennas and transceivers.

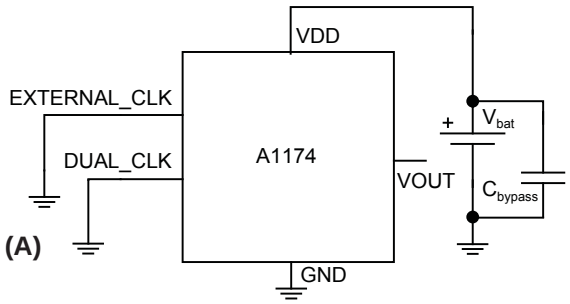
The schematics on this page represent typical application circuits.

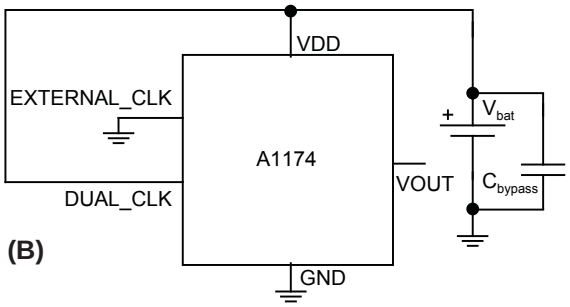
(A) Device is working in Normal Clock mode. Power consumption is determined by device internal clock.

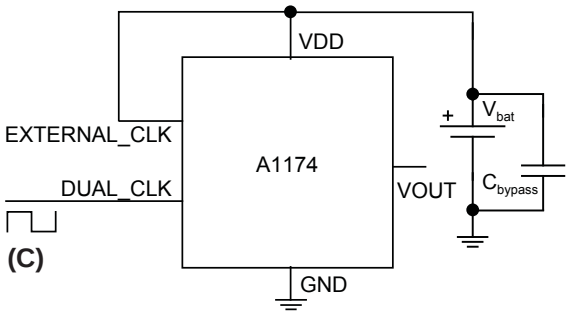
(B) Device is working in Dual Clock mode. Power consumption is determined by device internal clock; frequent usage of device in fast sampling state.

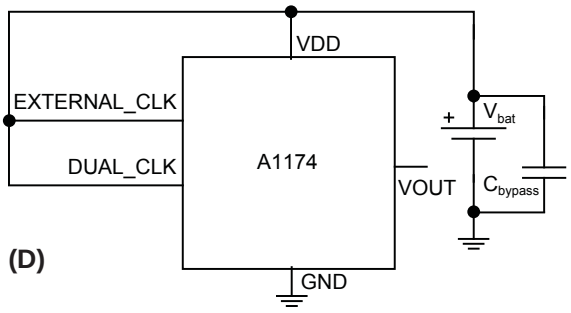
(C) Device is working in External Clock mode; externally-controlled power consumption.

(D) Device is working in External Clock mode; high power consumption.

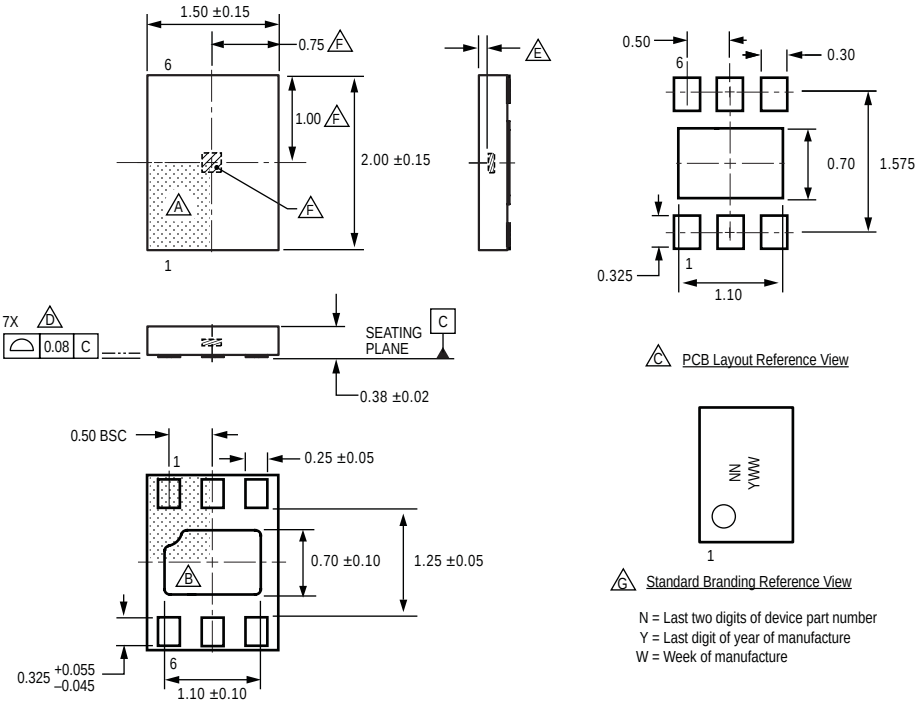








Package EW 6-Contact MLP/DFN



For Reference Only, not for tooling use (refernce DWG-2856; similar to JEDEC Type 1, MO-229X2BCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Active Area Depth 0.15 mm REF

F Hall Element (not to scale)

G Branding scale and appearance at supplier discretion

Revision History

Revision	Revision Date	Description of Revision
Rev. 7	October 26, 2011	Update Selection Guide

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