19-2640; Rev 1; 7/04

EVALUATION KIT AVAILABLE

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

General Description

The MAX1945R/MAX1945S high-efficiency pulse-width modulation (PWM) switching regulators deliver up to 6A of output current. The devices operate from an input supply range of 2.6V to 5.5V and provide selectable output voltages of 1.8V, 2.5V, and adjustable output voltages from 0.8V to 85% of the supply voltage. With V_{CC} at 3.3V/5V, the input voltage can be as low as 2.25V. The MAX1945R/MAX1945S are ideal for on-board post-regulation applications. Total output voltage error is less than ±1% over load, line, and temperature.

The MAX1945R/MAX1945S operate at a selectable fixed frequency (500kHz or 1MHz) or can be synchronized to an external clock (400kHz to 1.2MHz). The high operating frequency minimizes the size of external components. The high bandwidth of the internal error amplifier provides excellent transient response. The MAX1945R/MAX1945S have internal dual N-channel MOSFETs to lower heat dissipation at heavy loads. Two MAX1945R/MAX1945Ss can operate 180 degrees out-of-phase of each other to minimize input capacitance. The devices provide output voltage margining for board-level testing. The MAX1945R provides a ±4% voltage margining. The MAX1945S provides a ±9% voltage margining.

The MAX1945R/MAX1945S are available in 28-pin TSSOP-EP packages and are specified over the -40°C to +85°C industrial temperature range. An evaluation kit is available to speed designs.

Applications

Low-Voltage, High-Density Distributed Power Supplies

ASIC, CPU, and DSP Core Voltages

RAM Power Supply

Base Station, Telecom, and Networking Equipment Power Supplies

Server and Notebook Power Supplies

Pin Configuration appears at end of data sheet.

Features

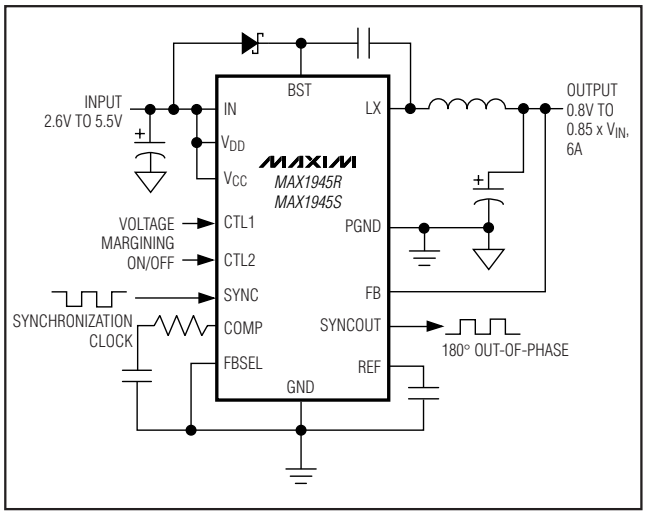
- **6A PWM Step-Down Regulator with 95% Efficiency**
- **1MHz/500kHz Switching for Small External Components**
- **0.76in² Complete 6A Regulator Footprint**
- **External Components' Height <3mm**
- **±1% Output Accuracy over Load, Line, and Temperature**
- **Operate from 2.6V to 5.5V Supply**
- **Operate from 2.5V Input with V_{CC} at 3.3V/5V**
- **Preset Output Voltage of 1.8V or 2.5V**
- **Adjustable Output from 0.8V to 85% of Input**
- **Voltage Margining: ±4% (MAX1945R) or ±9% (MAX1945S)**
- **Synchronize to External Clock**
- **SYNCOUT Provides 180-Degree Out-of-Phase Clock Output**
- **All-Ceramic or Electrolytic Capacitor Designs**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1945REUI	-40°C to +85°C	28 TSSOP-EP*
MAX1945SEUI	-40°C to +85°C	28 TSSOP-EP*

**EP = Exposed pad.*

Typical Operating Circuit



1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

ABSOLUTE MAXIMUM RATINGS

CTL1, CTL2, IN, SYNC, V_{CC}, V_{DD} to GND .....-0.3V to +6V
SYNCOUT, COMP, FB, FBSEL,
REF to GND .....-0.3V to (V_{CC} + 0.3V)
LX Current (Note 1) .....-9A to +9A
BST to LX .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V

Continuous Power Dissipation (T_A = +85°C)
(derate 23.8mW/°C above +70°C) 1191mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = V_{CTL1} = V_{CTL2} = V_{DD} = 3.3V, SYNC = GND, FBSEL = High-Z, V_{FB} = 0.7V, C_{REF} = 0.22µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN/V_{CC}							
Input Voltage	V_{IN}			2.6		5.5	V
IN Supply Current	I_{IN}	SYNC = V_{CC} (1MHz), no load	V_{IN} = 3.3V		12	20	mA
			V_{IN} = 5.5V		48		
V_{CC} Supply Current	I_{CC}	SYNC = V_{CC} (1MHz)	V_{CC} = 3.3V		2	3	mA
			V_{CC} = 5.5V		3		
V_{DD} Supply Current	I_{DD}	SYNC = V_{CC} (1MHz)	V_{DD} = 3.3V		5	8	mA
			V_{DD} = 5.5V		10		
Total Shutdown Current from IN, V_{CC}, and V_{DD}	I_{TOTAL}	V_{IN} = V_{CC} = V_{DD} = V_{BST} - V_{LX} = 5.5V, CTL1 = CTL2 = GND				500	µA
V_{CC} Undervoltage Lockout Threshold	V_{UVLO}	When LX starts/stops switching	V_{CC} rising		2.40	2.55	V
			V_{CC} falling	2.20	2.35		
V_{DD}							
V_{DD} Shutdown Supply Current		V_{IN} = V_{DD} = V_{BST} = 5.5V, V_{LX} = 5.5V or 0, CTL1 = CTL2 = GND				10	µA
BST							
BST Shutdown Supply Current	I_{BST}	V_{IN} = V_{DD} = V_{BST} = 5.5V, V_{LX} = 5.5V or 0, CTL1 = CTL2 = GND				10	µA
REF							
REF Voltage	V_{REF}	I_{REF} = 0, V_{IN} = 2.6V to 5.5V		1.97	2.00	2.04	V
REF Shutdown Resistance		From REF to GND, CTL1 = CTL2 = GND			10	100	Ω
COMP							
COMP Transconductance		From FB to COMP, V_{COMP} = 1.25V	FBSEL = High-Z	30	55	85	µS
			FBSEL = GND	13.3	24.4	37.8	
			FBSEL = V_{CC}	9.6	17.6	27.2	
COMP Clamp Voltage Low	V_{LOW_CLAMP}	V_{IN} = 2.6V to 5.5V, V_{FB} = 0.9V		0.5	0.8	1.1	V
COMP Clamp Voltage High	V_{HIGH_CLAMP}	V_{IN} = 2.6V to 5.5V, V_{FB} = 0.7V		1.90	2.15	2.40	V
COMP Shutdown Resistance		From COMP to GND, CTL1 = CTL2 = GND			10	100	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = V_{CTL1} = V_{CTL2} = V_{DD} = 3.3V, SYNC = GND, FBSEL = High-Z, V_{FB} = 0.7V, C_{REF} = 0.22µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FB							
FB Regulation Voltage (Error Amp Only)	V_{FB}	V_{COMP} = 1V to 2V, V_{IN} = 2.6V to 5.5V	FBSEL = GND	1.782	1.800	1.818	V
			FBSEL = V_{CC}	2.475	2.500	2.525	
			FBSEL = High-Z	0.792	0.800	0.808	
Maximum Output Current	I_{FB_OUT}	V_{IN} = 3.3V, V_{OUT} = 1.8V, L = 1µH		6			A
FB Voltage Margining Output (Error Amp Only)	$V_{MARGIN\_}$	MAX1945R, V_{COMP} = 1V to 2V, V_{IN} = 2.6V to 5.5V	CTL1 = V_{CC}, CTL2 = V_{CC}	-1		+1	%
			CTL1 = GND, CTL2 = V_{CC}	3		5	
			CTL1 = V_{CC}, CTL2 = GND	-5		-3	
		MAX1945S, V_{COMP} = 1V to 2V, V_{IN} = 2.6V to 5.5V	CTL1 = V_{CC}, CTL2 = V_{CC}	-1		+1	
			CTL1 = GND, CTL2 = V_{CC}	8		10	
			CTL1 = V_{CC}, CTL2 = GND	-10		-8	
FB Input Resistance		FB to GND, FBSEL = GND, or V_{FB} = 1.8V, or FBSEL = V_{CC}, or V_{FB} = 2.5V		25	50	100	kΩ
FB Input Bias Current		FBSEL = High-Z, V_{FB} = 0.7V			0.01	0.10	µA
LX							
LX On-Resistance High	$R_{ON\_HIGH\_LX}$	V_{IN} = V_{BST} - V_{LX} = 3.3V			26	43	mΩ
		V_{IN} = V_{BST} - V_{LX} = 2.6V			30	50	
LX On-Resistance Low	$R_{ON\_LOW\_LX}$	V_{IN} = 3.3V			26	43	mΩ
		V_{IN} = 2.6V			30	50	
LX Current-Sense Transresistance		From LX to COMP		43	54	65	mΩ
LX Current-Limit Threshold		Duty cycle =100%, V_{IN} = 2.6V/3.3V/5.5V	High side	8.0	10.4	12.8	A
			Low side	-6	-4	-2	
LX Leakage Current	I_{LEAK_LX}	V_{IN} = 5.5V, CTL1 = CTL2 = GND	V_{LX} = 5.5V			100	µA
			LX = GND	-100			
LX Switching Frequency	f_{SW}	V_{IN} = 2.6V/3.3V	SYNC = V_{CC}	0.8	1.0	1.2	MHz
			SYNC = GND	400	500	600	kHz
LX Minimum Off-Time	t_{OFF}	V_{IN} = 2.6V/3.3V			155	180	ns
LX Maximum Duty Cycle		V_{IN} = 2.6V/3.3V	SYNC = GND	90			%
			SYNC = V_{CC}	80			

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = V_{CTL1} = V_{CTL2} = V_{DD} = 3.3V, SYNC = GND, FBSEL = High-Z, V_{FB} = 0.7V, C_{REF} = 0.22µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Minimum Duty Cycle		V_{IN} = 2.6V/3.3V	SYNC = GND		8.8	10.5	%
			SYNC = V_{CC}		17.6		
RMS LX Output Current						6	A
FBSEL							
FBSEL Input Threshold 1.8V		Where 1.8V feedback switches in and out, V_{CC} = 2.6V/3.3V/5.5V	FBSEL rising		0.16	0.22	V
			FBSEL falling	0.08	0.14		
FBSEL Input Threshold 2.5V		Where 2.5V feedback switches in and out, V_{CC} = 2.6V/3.3V/5.5V	FBSEL rising		V_{CC} - 0.14	V_{CC} - 0.08	V
			FBSEL falling	V_{CC} - 0.22	V_{CC} - 0.16		
FBSEL Input Current Low	I_{LOW_FBSEL}	FBSEL = GND		-50	-20		µA
FBSEL Input Current High	I_{HIGH_FBSEL}	FBSEL = V_{CC}			20	50	µA
CTL1 /CTL2							
CTL1/CTL2 Input Threshold	$V_{IL\_CTL\_}$	V_{IN} = 2.6V to 5.5V		0.4	0.95		V
	$V_{IH\_CTL\_}$				1.0	1.6	
CTL1/CTL2 Input Current	$I_{IL\_CTL\_}$	V_{CTL1} or V_{CTL2} = 0 or 5.5V, V_{IN} = 5.5V		-1		+1	µA
	$I_{IH\_CTL\_}$			-1		+1	
Soft-Start Period		Time required for output to ramp up		2.9	3.7	4.5	ms
Time from Nominal to Margin High	$t_{HIGH\_4\%}$	+4%			160		µs
	$t_{HIGH\_9\%}$	+9%			360		
Time from Nominal to Margin Low	$t_{LOW\_4\%}$	-4%			450		µs
	$t_{LOW\_9\%}$	-9%			1000		
SYNC							
SYNC Capture Range		V_{IN} = 2.6V to 5.5V		0.4		1.2	MHz
SYNC Pulse Width	t_{LO}, t_{HI}	V_{IN} = 2.6V to 5.5V		250			ns
SYNC Input Threshold	V_{IL_SYNC}	V_{IN} = 2.6V to 5.5V		0.40	0.95		V
	V_{IH_SYNC}				1.0	1.6	
SYNC Input Current	I_{IL}, I_{IH}	V_{SYNC} = 0 or 5.5V, V_{IN} = 5.5V		-1		+1	µA
SYNCOUT							
SYNCOUT Frequency Range	$f_{SYNCOUT}$	V_{CC} = 2.6V to 5.5V		0.4		1.2	MHz
SYNCOUT Output Voltage	$V_{OH\_SYNCOUT}$	$I_{SYNCOUT}$ = ±1mA, V_{CC} = 2.6V to 5.5V		V_{CC} - 0.4	V_{CC} - 0.05		V
	$V_{OL\_SYNCOUT}$				0.05	0.40	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = V_{CTL1} = V_{CTL2} = V_{DD} = 3.3V, SYNC = GND, FBSEL = High-Z, V_{FB} = 0.7V, C_{REF} = 0.22µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN						
Thermal-Shutdown Hysteresis				20		°C
Thermal-Shutdown Threshold		When LX stops switching		165		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = V_{CTL1} = V_{CTL2} = V_{DD} = 3.3V, SYNC = GND, FBSEL = High-Z, V_{FB} = 0.7V, C_{REF} = 0.22µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN/V_{CC}							
Input Voltage	V_{IN}			2.6		5.5	V
IN Supply Current	I_{IN}	SYNC = V_{CC} (1MHz), no load	V_{IN} = 3.3V			20	mA
V_{CC} Supply Current	I_{CC}	SYNC = V_{CC} (1MHz)	V_{CC} = 3.3V			4	mA
V_{DD} Supply Current	I_{DD}	SYNC = V_{CC} (1MHz)	V_{DD} = 3.3V			8	mA
Total Shutdown Current from IN, V_{CC}, and V_{DD}	I_{TOTAL}	V_{IN} = V_{CC} = V_{DD} = V_{BST} - V_{LX} = 5.5V, CTL1 = CTL2 = GND				500	µA
V_{CC} Undervoltage Lockout Threshold	V_{UVLO}	When LX starts/stops switching	V_{CC} rising			2.55	V
			V_{CC} falling	2.20			
V_{DD}							
V_{DD} Shutdown Supply Current	I_{VDD}	V_{IN} = V_{DD} = V_{BST} = 5.5V, V_{LX} = 5.5V or 0, CTL1 = CTL2 = GND				10	µA
BST							
BST Shutdown Supply Current	I_{BST}	V_{IN} = V_{DD} = V_{BST} = 5.5V, V_{LX} = 5.5V or 0, CTL1 = CTL2 = GND				10	µA
REF							
REF Voltage	V_{REF}	I_{REF} = 0, V_{IN} = 2.6V to 5.5V		1.96		2.04	V
REF Shutdown Resistance		From REF to GND, CTL1 = CTL2 = GND				100	Ω
COMP							
COMP Transconductance		From FB to COMP, V_{COMP} = 1.25V	FBSEL = High-Z	30		85	µS
			FBSEL = GND	13.3		37.8	
			FBSEL = V_{CC}	9.6		27.2	
COMP Clamp Voltage Low	V_{LOW_CLAMP}	V_{IN} = 2.6V to 5.5V, V_{FB} = 0.9V		0.5		1.1	V
COMP Clamp Voltage High	V_{HIGH_CLAMP}	V_{IN} = 2.6V to 5.5V, V_{FB} = 0.7V		1.90		2.40	V
COMP Shutdown Resistance		From COMP to GND, CTL1 = CTL2 = GND				100	Ω

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = V_{CTL1} = V_{CTL2} = V_{DD} = 3.3V, SYNC = GND, FBSEL = High-Z, V_{FB} = 0.7V, C_{REF} = 0.22µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FB							
FB Regulation Voltage (Error Amp Only)	V_{FB}	V_{COMP} = 1V to 2V, V_{IN} = 2.6V to 5.5V	FBSEL = GND	1.773		1.827	V
			FBSEL = V_{CC}	2.462		2.538	
			FBSEL = High-Z	0.788		0.812	
Maximum Output Current	I_{FB_OUT}	V_{IN} = 3.3V, V_{OUT} = 1.8V, L = 1µH		6			A
FB Voltage Margining Output (Error Amp Only)	$V_{MARGIN\_}$	MAX1945R, V_{COMP} = 1V to 2V, V_{IN} = 2.6V to 5.5V	CTL1 = V_{CC}, CTL2 = V_{CC}	-1.5		+1.5	%
			CTL1 = GND, CTL2 = V_{CC}	2.5		5.5	
			CTL1 = V_{CC}, CTL2 = GND	-5.5		-2.5	
		MAX1945S, V_{COMP} = 1V to 2V, V_{IN} = 2.6V to 5.5V	CTL1 = V_{CC}, CTL2 = V_{CC}	-1.5		+1.5	
			CTL1 = GND, CTL2 = V_{CC}	7.5		10.5	
			CTL1 = V_{CC}, CTL2 = GND	-10.5		-7.5	
FB Input Resistance		FB to GND, FBSEL = GND, or V_{FB} = 1.8V, or FBSEL = V_{CC}, or V_{FB} = 2.5V		25		100	kΩ
FB Input Bias Current		FBSEL = High-Z, V_{FB} = 0.7V				0.1	µA
LX							
LX On-Resistance High	$R_{ON\_HIGH\_LX}$	V_{IN} = V_{BST} - V_{LX} = 3.3V				43	mΩ
		V_{IN} = V_{BST} - V_{LX} = 2.6V				50	
LX On-Resistance Low	$R_{ON\_LOW\_LX}$	V_{IN} = 3.3V				43	mΩ
		V_{IN} = 2.6V				50	
LX Current-Sense Transresistance		From LX to COMP		43		65	mΩ
LX Current-Limit Threshold		Duty cycle =100%, V_{IN} = 2.6V/3.3V/5.5V	High side	8.0		12.8	A
			Low side	-6		-2	
LX Leakage Current	I_{LEAK_LX}	V_{IN} = 5.5V, CTL1 = CTL2 = GND	V_{LX} = 5.5V			100	µA
			LX = GND	-100			
LX Switching Frequency	f_{SW}	V_{IN} = 2.6V/3.3V	SYNC = V_{CC}	0.8		1.2	MHz
			SYNC = GND	400		600	kHz
LX Minimum Off-Time	t_{OFF}	V_{IN} = 2.6V/3.3V				180	ns
LX Maximum Duty Cycle		V_{IN} = 2.6V/3.3V	SYNC = GND	90			%
			SYNC = V_{CC}	80			

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = V_{CTL1} = V_{CTL2} = V_{DD} = 3.3V, SYNC = GND, FBSEL = High-Z, V_{FB} = 0.7V, C_{REF} = 0.22µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Minimum Duty Cycle		SYNC = GND, V_{IN} = 2.6V/3.3V				10.5	%
FBSEL							
FBSEL Input Threshold 1.8V		Where 1.8V feedback switches in and out, V_{CC} = 2.6V/3.3V/5.5V	FBSEL rising			0.22	V
			FBSEL falling	0.08			
FBSEL Input Threshold 2.5V		Where 2.5V feedback switches in and out, V_{CC} = 2.6V/3.3V/5.5V	FBSEL rising			V_{CC} - 0.08	V
			FBSEL falling	V_{CC} - 0.22			
FBSEL Input Current Low	I_{LOW_FBSEL}	FBSEL = GND		-50			µA
FBSEL Input Current High	I_{HIGH_FBSEL}	FBSEL = V_{CC}				50	µA
CTL1/CTL2							
CTL1/CTL2 Input Threshold	$V_{IL\_CTL\_}$	V_{IN} = 2.6V to 5.5V		0.4			V
	$V_{IH\_CTL\_}$					1.6	
CTL1/CTL2 Input Current	$I_{IL\_CTL\_}$	V_{CTL1} or V_{CTL2} = 0 or 5.5V, V_{IN} = 5.5V		-1		+1	µA
	$I_{IH\_CTL\_}$			-1		+1	
Soft-Start Period		Time required for output to ramp up		2.9		4.5	ms
SYNC							
SYNC Capture Range		V_{IN} = 2.6V to 5.5V		0.4		1.2	MHz
SYNC Pulse Width		V_{IN} = 2.6V to 5.5V		250			ns
SYNC Input Threshold	V_{IL_SYNC}	V_{IN} = 2.6V to 5.5V		0.4			V
	V_{IH_SYNC}					1.6	
SYNC Input Current	I_{IL}, I_{IH}	V_{SYNC} = 0 or 5.5V, V_{IN} = 5.5V		-1		+1	µA
SYNCOUT							
SYNCOUT Frequency Range	$f_{SYNCOUT}$	V_{CC} = 2.6V to 5.5V		0.4		1.2	MHz
SYNCOUT Output Voltage	$V_{OH\_SYNCOUT}$	$I_{SYNCOUT}$ = ±1mA, V_{CC} = 2.6V to 5.5V		V_{CC} - 0.4			V
	$V_{OL\_SYNCOUT}$					0.4	

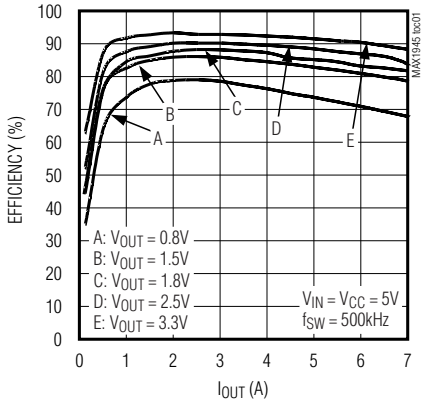
Note 2: Specifications to -40°C are guaranteed by design, not production tested.
Note 3: When connected together, the LX output is designed to provide 6A RMS current.

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

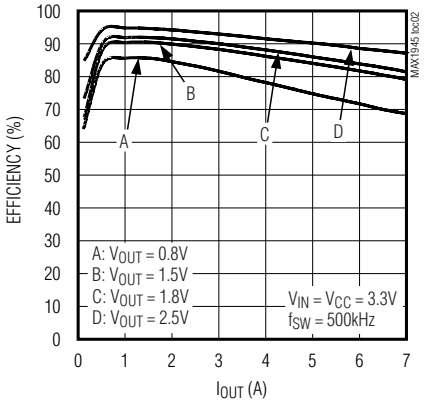
Typical Operating Characteristics

(V_{IN} = V_{CC} = 5V, V_{OUT} = 1.8V, I_{OUT} = 6A, f_{SW} = 500kHz, V_{DD} = V_{CC}, and T_A = +25°C, unless otherwise noted.)

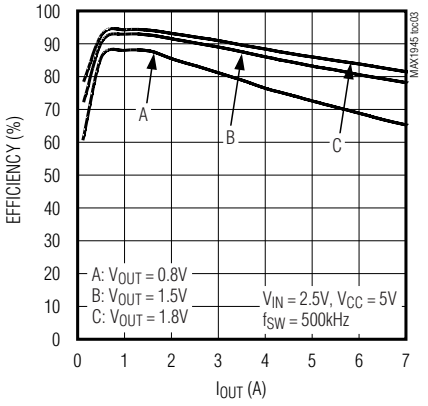
EFFICIENCY vs. OUTPUT CURRENT
V_{IN} = V_{CC} = 5V



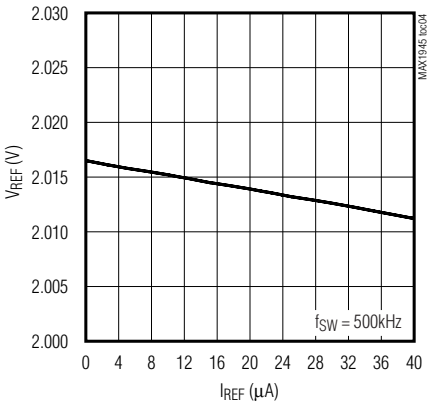
EFFICIENCY vs. OUTPUT CURRENT
V_{IN} = V_{CC} = 3.3V



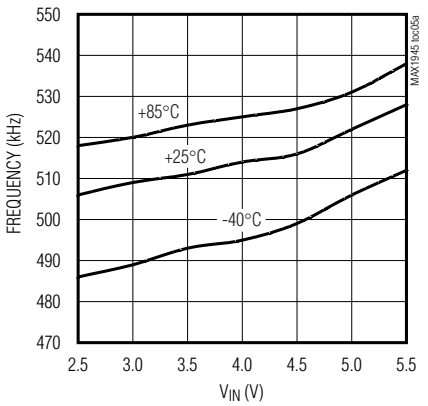
EFFICIENCY vs. OUTPUT CURRENT
V_{IN} = 2.5V, V_{CC} = 5V



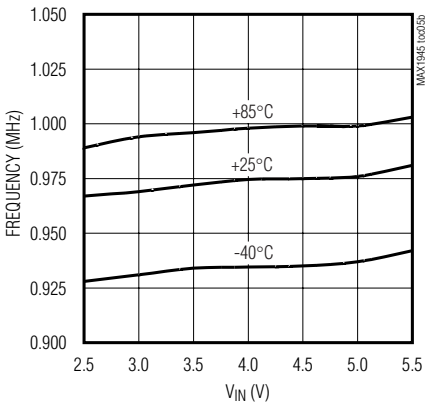
REFERENCE VOLTAGE
vs. REFERENCE SOURCE CURRENT



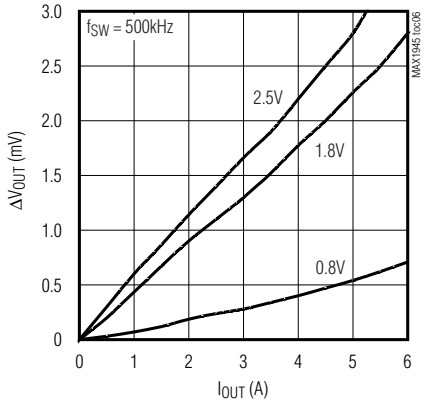
FREQUENCY vs. INPUT VOLTAGE (500kHz)



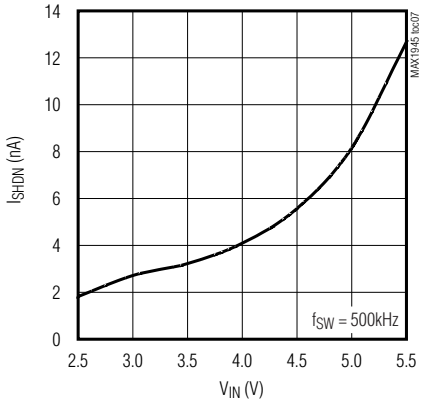
FREQUENCY vs. INPUT VOLTAGE (1MHz)



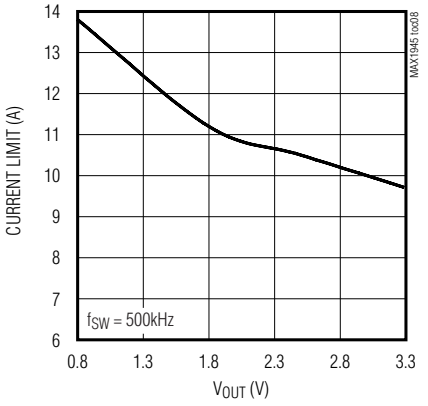
OUTPUT LOAD REGULATION



SHUTDOWN SUPPLY CURRENT
vs. INPUT VOLTAGE



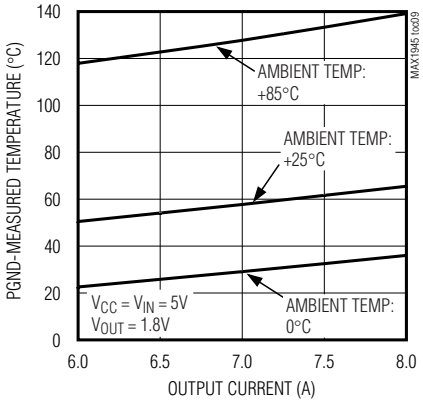
CURRENT LIMIT
vs. OUTPUT VOLTAGE



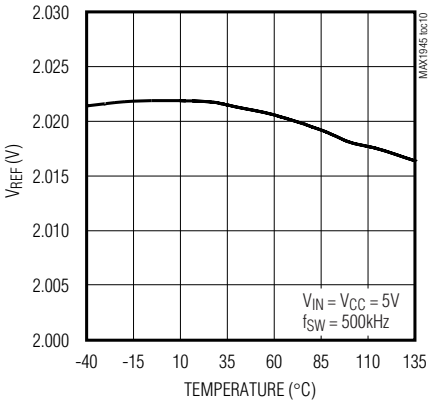
Typical Operating Characteristics (continued)

(V_{IN} = V_{CC} = 5V, V_{OUT} = 1.8V, I_{OUT} = 6A, f_{SW} = 500kHz, V_{DD} = V_{CC}, and T_A = +25°C, unless otherwise noted.)

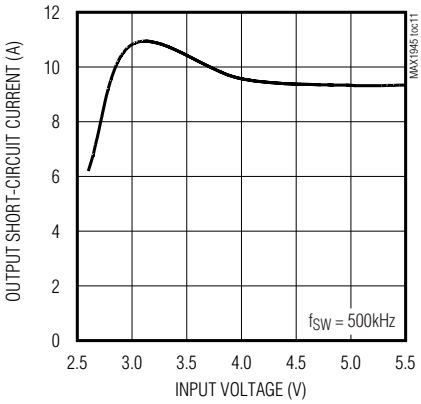
PGND-MEASURED TEMPERATURE vs. OUTPUT CURRENT



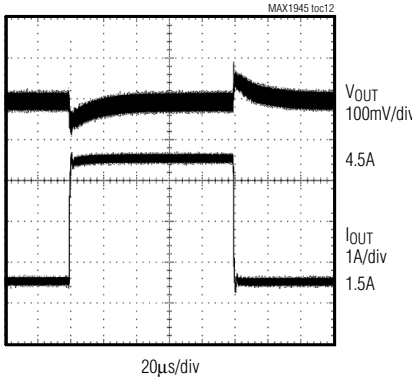
REFERENCE VOLTAGE vs. TEMPERATURE



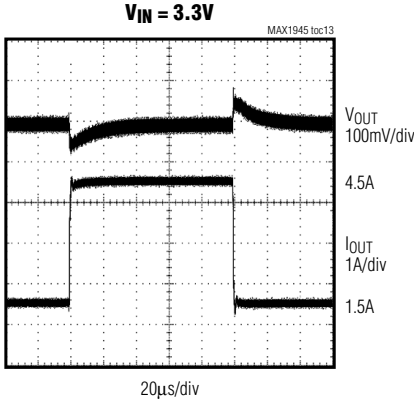
OUTPUT SHORT-CIRCUIT CURRENT vs. INPUT VOLTAGE



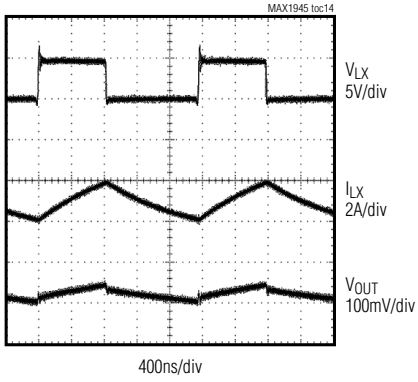
TRANSIENT RESPONSE VIN = 5V



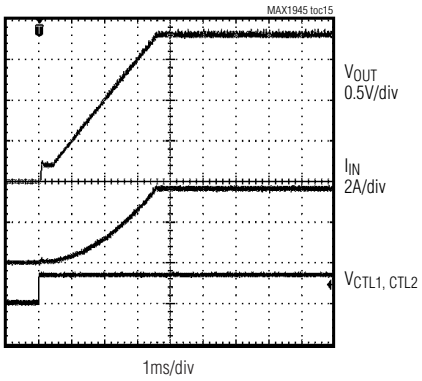
TRANSIENT RESPONSE VIN = 3.3V



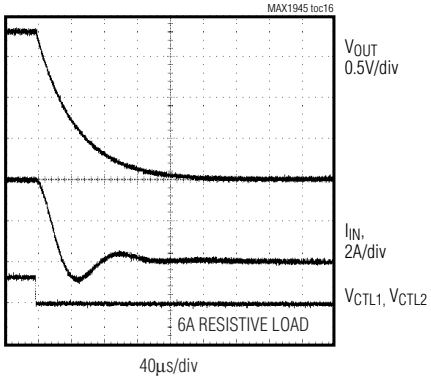
SWITCHING WAVEFORM VIN = 5V



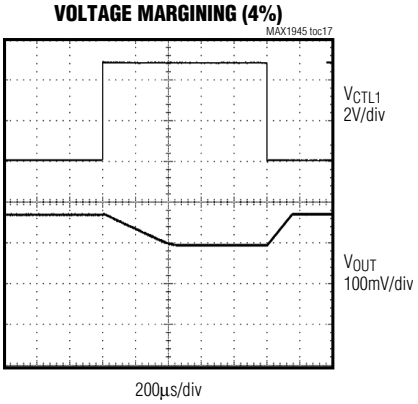
STARTUP WAVEFORMS



SHUTDOWN WAVEFORMS



VOLTAGE MARGINING (4%)

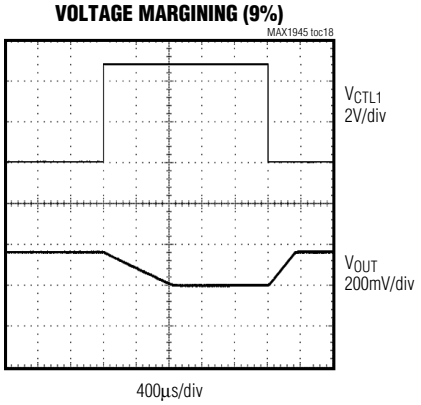


1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

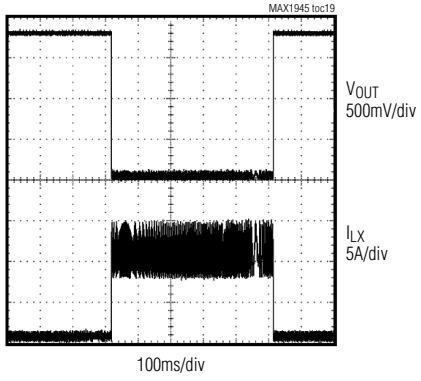
Typical Operating Characteristics (continued)

(V_{IN} = V_{CC} = 5V, V_{OUT} = 1.8V, I_{OUT} = 6A, f_{SW} = 500kHz, V_{DD} = V_{CC}, and T_A = +25°C, unless otherwise noted.)

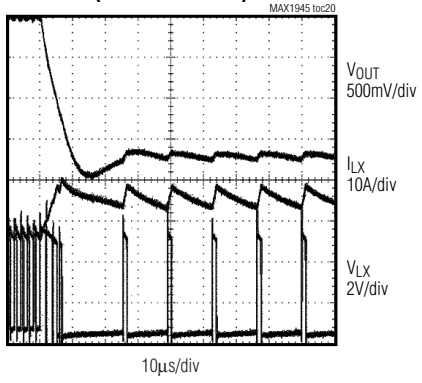
VOLTAGE MARGINING (9%)



SHORT-CIRCUIT INDUCTOR CURRENT



SHORT-CIRCUIT INDUCTOR CURRENT (EXPANDED TIME)



Pin Description

PIN	NAME	FUNCTION
1	BST	Bootstrap Voltage. High-side driver supply input. Connect a 0.1µF capacitor from BST to LX. Connect a Schottky diode from IN to BST. A 1N4148 diode can be used for 5V input to reduce cost.
2	V_{DD}	Low-Side Driver Supply Voltage
3, 5, 7, 9, 20, 22, 24, 26	LX	Inductor Connection. Connect an inductor between LX and the regulator output. Connect all LX pins together close to the device.
4, 6, 8, 10	IN	Power-Supply Voltage. Input voltage ranges from 2.6V to 5.5V. Bypass with 3 x 22µF ceramic capacitors in parallel to PGND (see the *Input Capacitor Selection* section).
11	V_{CC}	Supply-Voltage Input. V_{CC} powers the device. Connect a 10Ω resistor from IN to V_{CC}. Bypass V_{CC} to GND with 0.1µF.
12	GND	Analog Ground
13	REF	Reference. Bypass REF with 0.22µF capacitor to GND. REF tracks the soft-start ramp voltage margining and is pulled to GND when the output shuts down.
14	COMP	Regulator Compensation. Connect a series RC network from COMP to GND. COMP is pulled to GND when the output shuts down (see the *Compensation Design* section).
15	FB	Feedback Input. When FBSEL = High-Z, use an external resistor divider from the output to set the voltage from 0.8V to 85% of V_{IN}. Connect FB to the output for regulation to 1.8V when FBSEL = 0, or for regulation to 2.5V when FBSEL = V_{CC}.
16	FBSEL	Feedback Select Input. The device regulates to an output of 0.8V when FBSEL is left unconnected. The device regulates to an output of 1.8V when FBSEL = GND and regulates to an output of 2.5V when FBSEL = V_{CC}.
17	SYNC	Synchronization/Frequency Select. Connect SYNC to GND for 500kHz operation, to V_{CC} for 1MHz operation, or connect to an external clock at 400kHz to 1.2MHz.
18	SYNCOUT	Synchronization Output. SYNCOUT provides a frequency output synchronized 180 degrees out-of-phase to the operating frequency of the device.

Pin Description (continued)

PIN	NAME	FUNCTION
19, 21, 23, 25	PGND	Power Ground. Connect all PGND together close to the device. Star connect GND to PGND (see the *PC Board Layout Considerations* section).
27	CTL1	Output Margining Control Inputs. When CTL1 = CTL2 = GND, the regulator is off. When CTL1 = CTL2 = V_{CC}, the regulator runs at nominal output voltage. When CTL1 = V_{CC} and CTL2 = GND, the output is set to the margin-low output (-4% or -9%). When CTL1 = GND and CTL2 = V_{CC}, the output is set to the margin-high output (+4% or +9%).
28	CTL2	
	EP	Exposed Pad. Connect to PGND to improve power dissipation.

Detailed Description

The MAX1945R/MAX1945S high-efficiency PWM switching regulators deliver up to 6A of output current. The devices operate at a selectable fixed frequency (500kHz or 1MHz) or can be synchronized to an external frequency (400kHz to 1.2MHz). The devices operate from a 2.6V to 5.5V input supply voltage and have a selectable output voltage of 1.8V or 2.5V, or an adjustable output voltage from 0.8V to 85% of the input voltage, making the MAX1945R/MAX1945S ideal for on-board post-regulation applications. The high switching frequency allows the use of small external components. Internal synchronous rectifiers improve efficiency and eliminate the typical Schottky freewheeling diode. Total output error over load, line, and temperature is less than ±1%.

Controller Function

The MAX1945R/MAX1945S step-down converters use a PWM current-mode control scheme. A PWM comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope-compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Because the average inductor current is nearly the same as the peak inductor current (<30% ripple current), the circuit acts as a switch-mode transconductance amplifier.

To preserve inner-loop stability and eliminate inductor staircasing, a slope-compensation ramp is summed into the main PWM comparator. During the off-cycle, the internal high-side N-channel MOSFET turns off, and the internal low-side N-channel turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current and discharges when the inductor current is lower, smoothing the voltage across the load. During an overload condition, when the inductor current exceeds the current limit (see the *Current Limit* section), the high-side MOSFET does not turn on at the rising edge of the clock, and the low-side MOSFET remains on to let the inductor current ramp down.

Current Sense

An internal current-sense amplifier produces a current signal proportional to the voltage generated by the high-side MOSFET on-resistance and the inductor current ($R_{DS(ON)} \times I_{LX}$). The amplified current-sense signal and the internal slope-compensation signal sum together at the comparator inverting input. The PWM comparator turns off the internal high-side MOSFET when this sum exceeds the COMP voltage from the error amplifier.

Current Limit

The internal high-side MOSFET has a current limit of 8A (min). If the current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. The minimum duty cycle is limited to 10%. A synchronous rectifier current limit of 2A minimum protects the device from current flowing into LX.

When the negative current limit is exceeded, the device turns off the synchronous rectifier, forcing the inductor current to flow through the high-side MOSFET body diode and back to the input, until the beginning of the next cycle, or until the inductor current drops to zero. The MAX1945R/MAX1945S use a pulse-skip mode to prevent overheating during short-circuit output conditions. The device enters pulse-skip mode when the FB voltage drops below 300mV, limiting the current and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

Soft-Start

The MAX1945R/MAX1945S employs digital soft-start to reduce supply in-rush current during startup conditions. When the device exits undervoltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the digital soft-start circuitry slowly ramps up the voltages at REF and FB (see the *Typical Operating Characteristics*). An internal oscillator sets the soft-start time to 3.7ms (typ). Use a of 0.22µF capacitor (min) to reduce the susceptibility to switching noise.

Undervoltage Lockout (UVLO)

When V_{CC} drops below 2.35V, the UVLO circuit inhibits switching. Once V_{CC} rises above 2.4V, UVLO clears and the soft-start function activates.

Bootstrap (BST)

A capacitor connected between BST and LX and a Schottky diode connected from IN to BST generate the gate drive for the internal high-side N-channel MOSFET. When the low-side N-channel MOSFET is on, LX goes to PGND. IN charges the bootstrap capacitor through the Schottky diode. When the low-side N-channel MOSFET turns off and the high side N-channel MOSFET turns on, V_{LX} goes to V_{IN}. The Schottky diode prevents the capacitor from discharging into IN.

Frequency Select (SYNC)

The MAX1945R/MAX1945S operate in PWM mode with a selectable fixed frequency or synchronized to an external frequency. The devices switch at a frequency of 500kHz when SYNC is connected to ground. The devices switch at 1MHz with SYNC connected to V_{CC}. Apply an external frequency of 400kHz to 1.2MHz with 10% to 90% duty cycle at SYNC to synchronize the switching frequency of MAX1945R/MAX1945S.

Output Voltage Select

The MAX1945R/MAX1945S feature selectable fixed and adjustable output voltages. With FB connected to the output, the output voltage is 1.8V when FBSEL is at GND and 2.5V when FBSEL is at V_{CC} (Figure 1). When FBSEL is floating, connect FB to an external resistor divider from V_{OUT} to GND to set the output voltage from 0.8V to 85% of V_{IN} (Figure 2). Select R2 in the 1kΩ to 10kΩ range. Calculate R1 using the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.8V.

Shutdown Mode

Drive CTL1 and CTL2 to ground to shut down the MAX1945R/MAX1945S. In shutdown mode, the internal MOSFETs stop switching and LX goes to high impedance; REF and COMP go to ground.

Voltage Margining

The MAX1945R/MAX1945S provide selectable voltage margining. The MAX1945R provides ±4% voltage margining, and the MAX1945S provides ±9% voltage margining. CTL1 and CTL2 set the voltage margins (Table 1).

Table 1. Setting Voltage Margin

	CTL1	CTL2	V_{OUT}	
			MAX1945R	MAX1945S
Voltage Margin	0V	0V	OFF	OFF
	V_{CC}	V_{CC}	NOMINAL	NOMINAL
	V_{CC}	0V	-4%	-9%
	0V	V_{CC}	+4%	+9%

Thermal Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature (T_J) exceeds 165°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, causing a pulsed output during continuous overload conditions.The soft-start sequence begins after a thermal-shutdown condition.

Design Procedure

VCC Decoupling

Because of the high switching frequency and tight output tolerance, decouple V_{CC} with 0.1µF capacitor from V_{CC} to GND with a 10Ω resistor from V_{CC} to IN. Place the capacitor as close to VCC as possible.

Inductor Design

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{OSC} \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where LIR is the ratio of the inductor ripple current to average continuous current at a minimum duty cycle. Choose LIR between 20% to 40% of the maximum load current for best performance and stability.

Use a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Ferrite core types are often the best choice for performance. With any core material the core must be large enough not to saturate at the peak inductor current (I_{PEAK}).

$$I_{PEAK} = \left(1 + \frac{LIR}{2}\right) I_{OUT(MAX)}$$

Example:

V_{IN} = 3.3V

V_{OUT} = 1.8V

f_{OSC} = 500kHz

$I_{OUT(MAX)}$ = 6A

LIR = 30%

L = 1µH and I_{PEAK} = 6.9A

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs because of variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL are:

$$V_{RIPPLE(C)} = I_{P-P}/(8 \times C_{OUT} \times f_{SW}),\ V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = (I_{P-P}/t_{ON}) \times ESL \text{ or } (I_{P-P}/t_{OFF}) \times ESL, \text{ whichever is greater}$$

The peak inductor current (I_{P-P}) is:

$$I_{P-P} = ((V_{IN} - V_{OUT})/(f_{SW} \times L)) \times (V_{OUT}/V_{IN})$$

Example:

V_{IN} = 3.3V

V_{OUT} = 1.8V

f_{OSC} = 500kHz

$I_{OUT(MAX)}$ = 6A

LIR = 30%

L = 1µH

C_{OUT} = 180µF

$ESR_{(OUTPUT\ CAPACITOR)}$ = 30mΩ

$ESL_{(OUTPUT\ CAPACITOR)}$ = 2.5nH

$V_{RIPPLE(C)}$ = 2mV

$V_{RIPPLE(ESR)}$ = 45mV

$V_{RIPPLE(ESL)}$ = 4mV

V_{RIPPLE} = 51mV

Use these equations for initial capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output voltage ripple. Because the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with a larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages negligible. Load transient response depends on the selected output. During a load transient, the output instantly changes by ESR × I_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the Transient Response graphs in the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth.

A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The impedance of the input capacitor at the switching frequency should be less than that of the input source so that high-frequency switching currents do not pass through the input source but instead are shunted through the input capacitor. A high source impedance requires larger input capacitance. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \left(\frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

where I_{RIPPLE} is the input RMS ripple current.

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

Compensation Design

The double pole formed by the inductor and the output capacitor of most voltage-mode controllers introduces a large phase shift, which requires an elaborate compensation network to stabilize the control loop. The MAX1945R/MAX1945S controllers utilize a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, eliminating the double pole caused by the inductor and output capacitor, and greatly simplifying the compensation network. A simple Type 1 compensation with a single compensation resistor (R_C) and compensation capacitor (C_C) creates a stable and high bandwidth loop (Figure 1).

An internal transconductance error amplifier compensates the control loop. Connect a series resistor and capacitor between COMP (the output of the error amplifier) and GND, to form a pole-zero pair. The external inductor, internal current-sense circuitry, output capacitor, and external compensation circuit determine the loop-system stability. Choose the inductor and output capacitor based on performance, size, and cost. Additionally, select the compensation resistor and capacitor to optimize control-loop stability. The component values shown in the typical application circuit yield stable operation over a broad range of input-to-output voltages.

Compensating the voltage feedback loop depends on the type of output capacitors used. Common capacitors for output filtering: ceramic capacitors, polymer capacitors such as POSCAPs and SPCAPs, and electrolytic capacitors. Use either ceramic or polymer capacitors. Use polymer capacitors as the output capacitor when selecting 500kHz operation. At 500kHz switching, the voltage feedback loop is slower (about 50kHz to 60kHz) when compared to 1MHz switching. Therefore, a polymer capacitor's high capacitance for a given footprint improves the output response during a step load change. Because of its relative low ESR frequencies (about 20kHz to 80kHz), use Type 2 compensation. The additional high-frequency pole introduced in Type 2 compensation offsets the ESR zero introduced by the polymer capacitors to provide continuous attenuation above the ESR zero frequencies of the polymer capacitors. However, the presence of the parasitic capacitance at COMP and the high output impedance of the error amplifier already provide the required attenuation above the ESR frequencies. The following steps outline the design process of compensating the MAX1945 with polymer output capacitors with the components in the application circuits Figures 1 and 2.

Regulator DC Gain:

$$G_{DC} = \Delta V_{OUT}/\Delta V_{COMP} = gmc \times R_{OUT}$$

Load Impedance Pole Frequency:

$$fp_{LOAD} = 1/(2 \times \pi \times C_{OUT} \times (R_{OUT} + R_{ESR}))$$

Load Impedance Zero Frequency:

$$fz_{ESR} = 1/(2 \times \pi \times C_{OUT} \times R_{ESR})$$

where $R_{OUT} = V_{OUT}/I_{OUT(MAX)}$, and gmc = 18.2S.

The feedback divider has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where V_{FB} = 0.8V. The transconductance error amplifier has a DC gain, $G_{EA(DC)}$, of 70dB. The compensation capacitor, C_C, and the output resistance of the error amplifier, R_{OEA} (20MΩ), set the dominant pole. C_C and R_C set a compensation zero. Calculate the dominant pole frequency as:

$$fp = 1/(2\pi \times C_C \times R_{OEA})$$

Determine the compensation zero frequency as:

$$fz_{EA} = 1/(2\pi \times C_C \times R_C)$$

For best stability and response performance, set the closed-loop unity-gain frequency much higher than the load-impedance pole frequency. The closed-loop unity-gain crossover frequency must be less than one-fifth of the switching frequency. Set the crossover frequency to 10% to 15% of the switching frequency. The loop-gain equation at unity-gain frequency, f_C, is given by:

$$G_{EA} \times G_{DC} \times (fp_{LOAD}/f_C) \times (V_{FB}/V_{OUT}) = 1$$

where $G_{EA} = gm_{EA} \times R_C$, and gm_{EA} = 50µS, the transconductance of the voltage-error amplifier. Calculate R_C as:

$$R_C = (V_{OUT} \times f_C)/(gm_{EA} \times V_{FBx} \times G_{DC} \times fp_{LOAD})$$

Set the error-amplifier compensation zero formed by R_C and C_C equal to the load-impedance pole frequency, f_{PLOAD}, at maximum load. Calculate C_C as:

$$C_C = (C_{OUT} \times R_{OUT})/R_C$$

500kHz Switching

The following design example is for the application circuit shown in Figures 1 and 2:

V_{OUT} = 1.8V

$I_{OUT(MAX)}$ = 6A

C_{OUT} = 180µF

R_{ESR} = 0.04Ω

gm_{EA} = 50µs

gmc = 18.2s

f_{SWITCH} = 500kHz

$R_{OUT} = V_{OUT}/I_{OUT(MAX)}$ = 1.8V/6 A = 0.3Ω

$fp_{DC} = 1/(2\pi \times C_{OUT} \times (R_{OUT} + R_{ESR}) = 1/(2\pi \times 180 \times 10^{-6} \times (0.3 + 0.04) = 2.6kHz$.

$fz_{ESR} = 1/(2\pi \times C_{OUT}\ R_{ESR}) = 1/(2\pi \times 180 \times 10^{-6} \times 0.04) = 22.1kHz$.

Pick the closed-loop unity-gain crossover frequency (f_C) at 60kHz. Determine the switching regulator DC gain:

$$G_{DC} = gmc \times R_{OUT} = 18.2 \times 0.3 = 5.46$$

then:

$$R_C = (V_{OUT} \times f_C)/(gm_{EA} \times V_{FB} \times G_{DC} \times fp_{LOAD}) = (1.8 \times 60kHz)/(50 \times 10^{-6} \times 0.8 \times 5.46 \times 2.6kHz) \approx 190k\Omega$$

(1%), choose R_C = 180kΩ, 1%

$$C_C = (C_{OUT} \times (R_{OUT} + R_{ESR}))/R_C = (180uF \times (0.3 + 0.04))/180k\Omega \approx 340pF$$

, choose C_C = 330pF, 10%

Table 2 shows the recommended values for R_C and C_C for different output voltages.

1MHz Switching

Following procedure outlines the compensation process of the MAX1945 for 1MHz operation with all ceramic output capacitors (Figure 3). The basic regulator loop consists of a power modulator, an output-feedback divider, and an error amplifier. The switching regulator has a DC gain set by gmc × R_{OUT}, where gmc is the transconductance from the output voltage of the error amplifier to the output inductor current. The load impedance of the switching modulator consists of a pole-zero pair set by R_{OUT}, the output capacitor (C_{OUT}), and its ESR. The following equations define the power train of the switching regulator:

Regulator DC Gain:

$$G_{DC} = \Delta V_{OUT}/\Delta V_{COMP} = gmc \times R_{OUT}$$

Load-Impedance Pole Frequency:

$$fp_{LOAD} = 1/(2 \times \pi \times C_{OUT} \times (R_{OUT} + R_{ESR}))$$

Load-Impedance Zero Frequency:

$$fz_{ESR} = 1/(2 \times \pi \times C_{OUT} \times R_{ESR})$$

where, $R_{OUT} = V_{OUT}/I_{OUT(MAX)}$, and gmc = 18.2. The feedback divider has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is equal to 0.8V. The transconductance error amplifier has a DC gain, $G_{EA(DC)}$, of 70dB. The compensation capacitor, C_C, and the output resistance of the error amplifier, R_{OEA} (20MΩ), set the dominant pole. C_C and R_C set a compensation zero. Calculate the dominant pole frequency as:

$$fp_{EA} = 1/(2\pi \times C_C \times R_{OEA})$$

Determine the compensation zero frequency as:

$$fz_{EA} = 1/(2\pi \times C_C \times R_C)$$

For best stability and response performance, set the closed-loop unity-gain frequency much higher than the load impedance pole frequency. In addition, set the closed-loop unity-gain crossover frequency less than one-fifth of the switching frequency. However, the maxi-

Table 2. Compensation Values for Output Voltages (500kHz)

VOUT (V)	0.8	1.2	1.8	2.5	3.3
R_C	110kΩ	147kΩ	180kΩ	287kΩ	365kΩ
C_C	330pF	330pF	330pF	220pF	220pF

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

Table 3. Compensation Values for Output Voltages (1MHz)

VOUT (V)	0.8	1.2	1.8	2.2	3.3
R_C (1%)	100kΩ	100kΩ	178kΩ	178kΩ	249kΩ
C_C (10%)	330pF	330pF	100pF	100pF	100pF

mum zero-crossing frequency should be less than one-third of the load-impedance zero frequency, fz_{ESR}. The previous requirement on the ESR zero frequency applies to ceramic output capacitors.

The loop-gain equation at unity-gain frequency, f_C, is given by:

$$G_{EA(fc)} \times G_{DC} \times (f_{PLOAD}/f_C) \times (V_{FB}/V_{OUT}) = 1$$

where $G_{EA(fc)} = gm_{EA} \times R_C$, and gm_{EA} = 50µ, the transconductance of the voltage error amplifier. Calculate R_C as:

$$R_C = (V_{OUT} \times f_C)/(gm_{EA} \times V_{FBx} \times G_{DC} \times f_{PLOAD})$$

Set the error-amplifier compensation zero formed by R_C and C_C equal to the load-impedance pole frequency, f_{PLOAD}, at maximum load. Calculate C_C as follows:

$$C_C = (C_{OUT} \times R_{OUT})/R_C$$

As the load current decreases, the load-impedance pole also decreases; however, the switching regulator DC gain increases accordingly, resulting in a constant closed-loop unity-gain frequency. Table 3 shows the values for R_C and C_C at various output voltages. The values are based on 2 × 47µF output capacitors and a 0.68µH output inductance.

For C_{OUT} = 2 × 47µF and L = 0.68µH. Decrease R_C accordingly when using large values of C_{OUT} or L.

V_{OUT} = 1.8V

$I_{OUT(MAX)}$ = 6A

C_{OUT} = 2 × 47µF

R_{ESR} = 0.005Ω

gm_{EA} = 50µ

gmc = 18.2s

f_{SWITCH} = 1.0MHz

$R_{OUT} = V_{OUT}/I_{OUT(MAX)}$ = 1.8V/6A= 0.3Ω

$fp_{DC} = [1/(2\pi \times C_{OUT} \times (R_{OUT} + R_{ESR}))] = [1/(2 \times \pi \times 94 \times 10^{-6} \times (0.3 + 0.005))] = 5.554kHz$

Applications Information

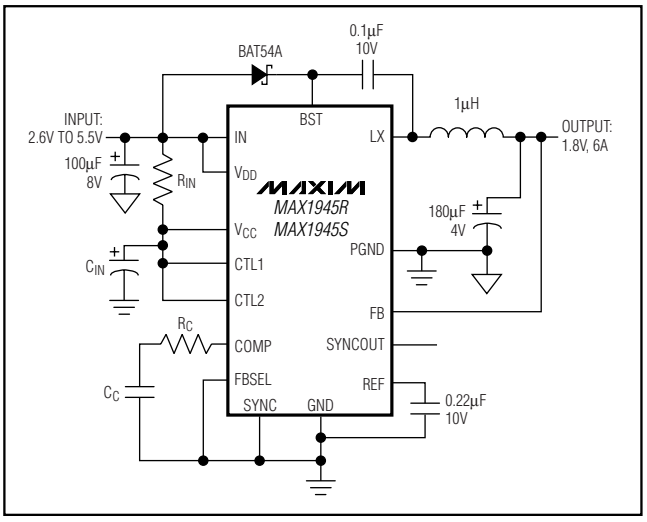


Figure 1. Typical Application Circuit (Fixed Output Voltage)

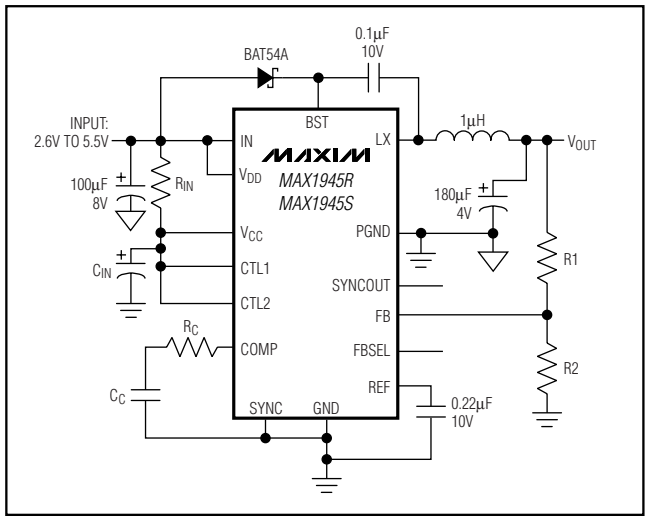


Figure 2. Typical Application Circuit (Adjustable Output Voltage)

$fz_{ESR} = [1/(2\pi \times C_{OUT} R_{ESR})] = [1/(2 \times \pi \times 94 \times 10^{-6} \times 0.005)] = 339kHz$.

For a 0.68µH output inductor, choose the closed-loop unity-gain crossover frequency (f_C) at 120kHz. Determine the switching regulator DC gain:

$$G_{DC} = gmc \times R_{OUT} = 18.2 \times 0.3 = 5.46$$

then:

$$R_C = (V_{OUT} \times f_C)/(gm_{EA} \times V_{FB} \times G_{DC} \times fp_{LOAD}) = (1.8 \times 120kHz)/(50 \times 10^{-6} \times 0.8 \times 5.46 \times 5.554kHz) \approx 178k\Omega\ (1\%)$$

$$C_C = (C_{OUT} \times R_{OUT})/R_C = (94\mu F \times 0.3)/178k\Omega \approx 156pF,$$ choose C_C = 100pF, 10%

Output Inductor: 0.68µH/12A, 5mΩ ESR (max), Coilcraft DO3316P-681HC

Output Capacitor C5: 2XJMK432BJ476MM

Input Capacitor C1: LMK432BJ226MM

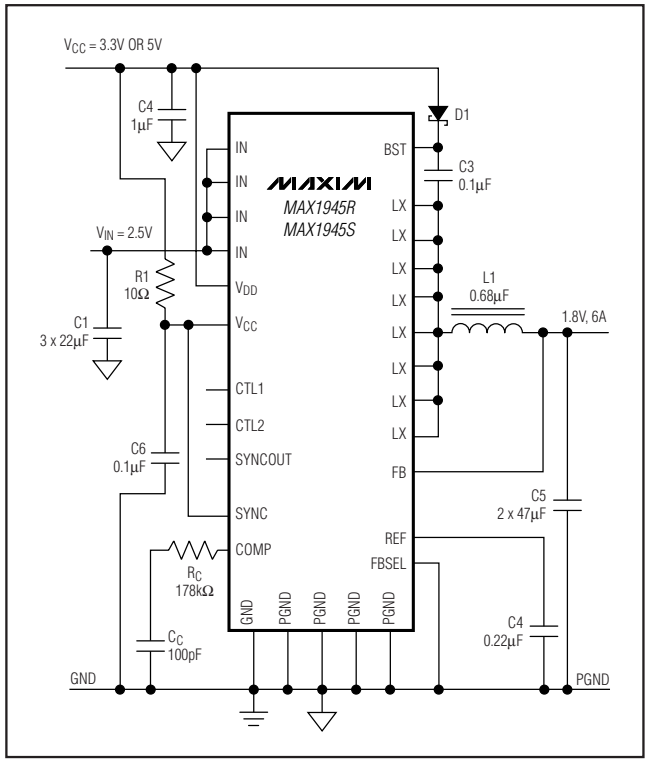


Figure 3. Typical Application Circuit with all ceramic capacitors (1MHz)

PC Board Layout Considerations

Careful PC board layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to the IC as possible. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate. Star connect both ground plane at output capacitor.
2) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by the high-side MOSFET, the low side MOSFET, and the input capacitors. Avoid vias in the switching paths.
4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).

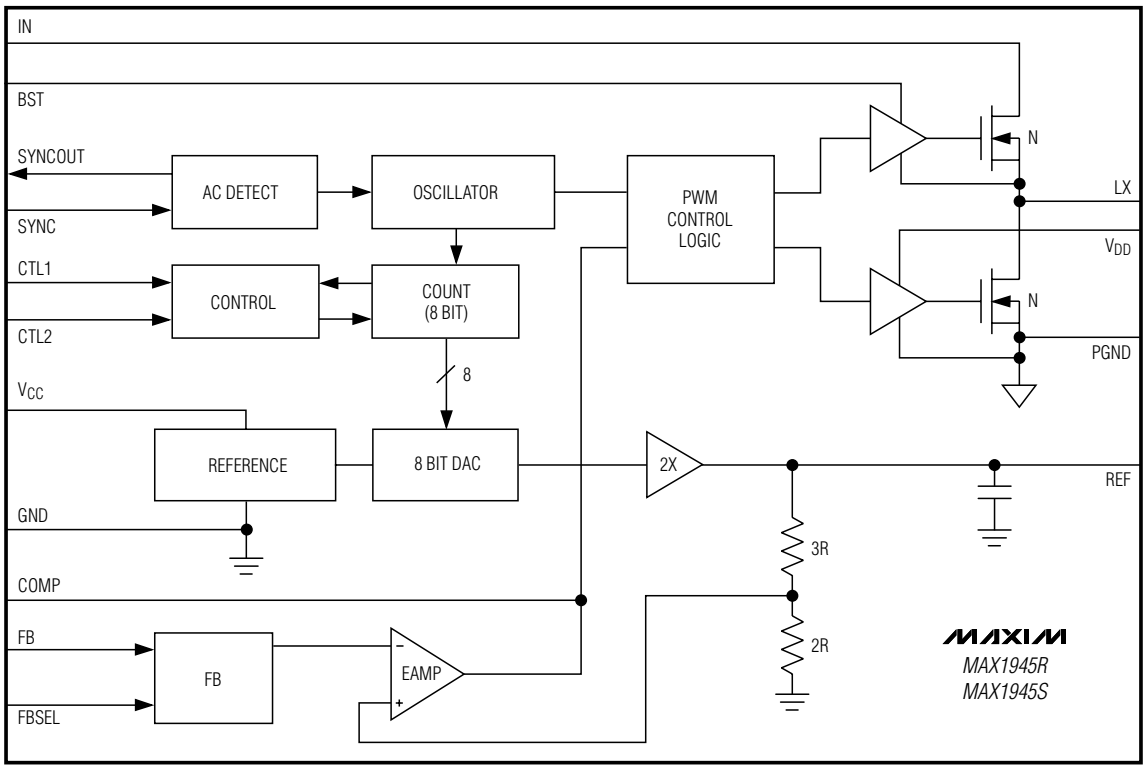
Chip Information

TRANSISTOR COUNT: 5000

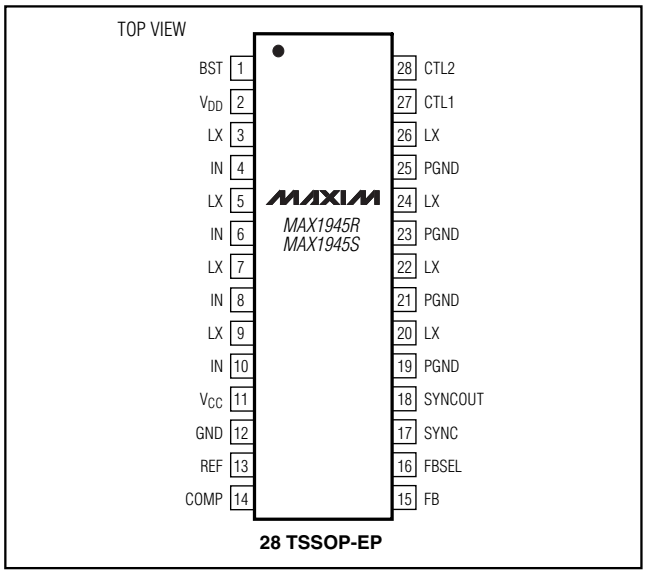
PROCESS: BiCMOS

1MHz, 1% Accurate, 6A Internal Switch Step-Down Regulators

Functional Diagram



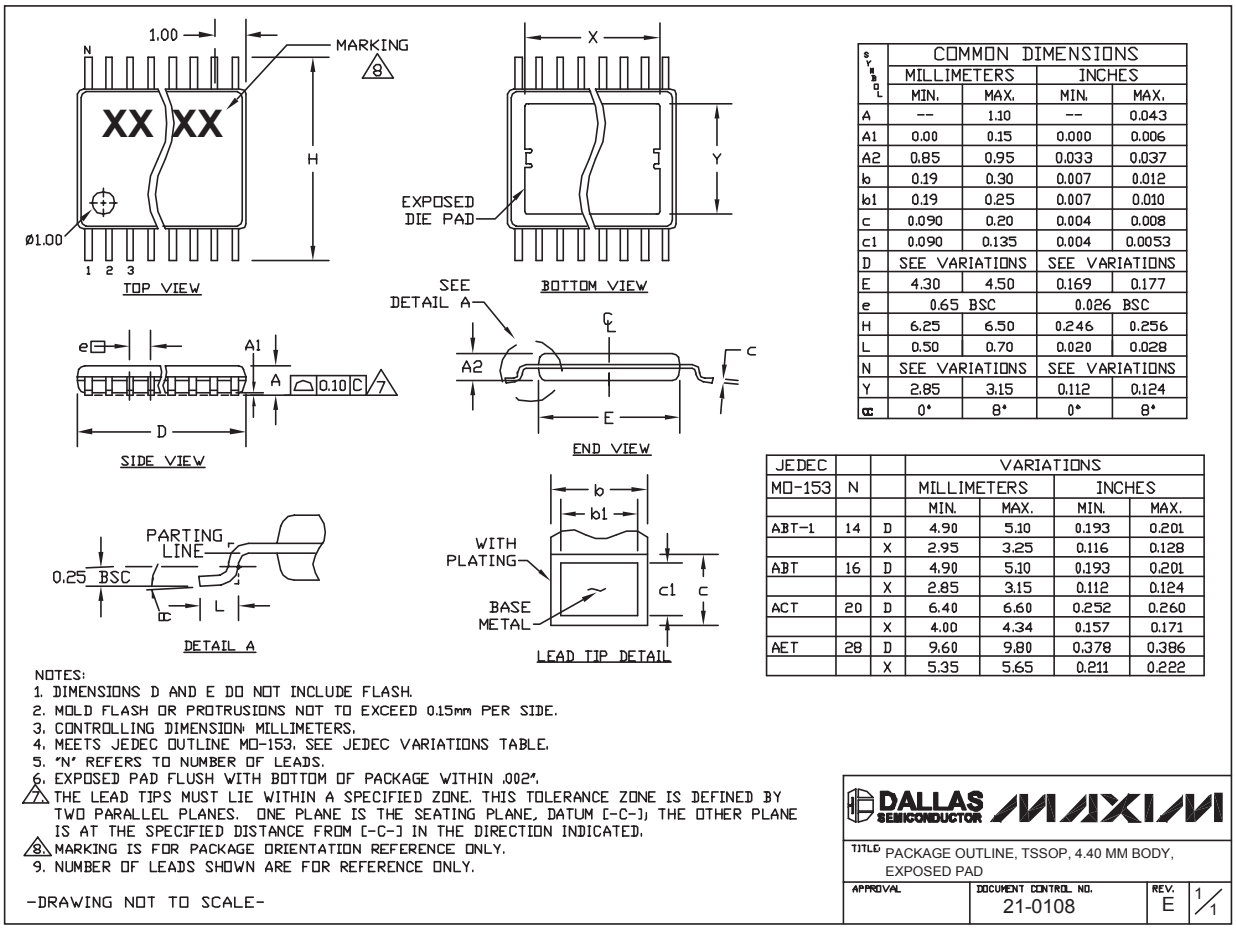
Pin Configuration



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.00	0.15	0.000	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD			
APPROVAL	DOCUMENT CONTROL NO. 21-0108	REV. E	1/1