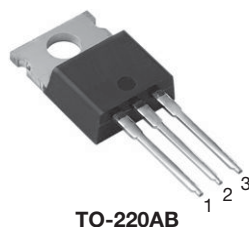
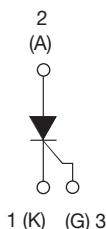




## Thyristor High Voltage, Phase Control SCR, 25 A



TO-220AB



## FEATURES

- Designed and qualified according to JEDEC®-JESD 47
- 125 °C max. operating junction temperature
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**  
Available

## APPLICATIONS

- Typical usage is in input rectification crowbar (soft start) and AC switch in motor control, UPS, welding, and battery charge.

## DESCRIPTION

The VS-25TTS... high voltage series of silicon controlled rectifiers are specifically designed for medium power switching and phase control applications. The glass passivation technology used has reliable operation up to 125 °C junction temperature.

## PRIMARY CHARACTERISTICS

$I_{T(AV)}$	16 A
$V_{DRM}/V_{RRM}$	800 V, 1200 V
$V_{TM}$	1.25 V
$I_{GT}$	45 mA
$T_J$	-40 °C to 125 °C
Package	TO-220AB
Circuit configuration	Single SCR

## OUTPUT CURRENT IN TYPICAL APPLICATIONS

APPLICATIONS	SINGLE-PHASE BRIDGE	THREE-PHASE BRIDGE	UNITS
Capacitive input filter $T_A = 55$ °C, $T_J = 125$ °C, common heatsink of 1 °C/W	18	22	A

## MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$	Sinusoidal waveform	16	A
$I_{RMS}$		25	
$V_{RRM}/V_{DRM}$		800/1200	V
$I_{TSM}$		320	A
$V_T$	16 A, $T_J = 25$ °C	1.25	V
$dV/dt$		500	V/ $\mu$ s
$dI/dt$		150	A/ $\mu$ s
$T_J$		-40 to 125	°C

## VOLTAGE RATINGS

PART NUMBER	$V_{RRM}$ , MAXIMUM PEAK REVERSE VOLTAGE V	$V_{DRM}$ , MAXIMUM PEAK DIRECT VOLTAGE V	$I_{RRM}/I_{DRM}$ AT 125 °C mA
VS-25TTS08PbF, VS-25TTS08-M3	800	800	10
VS-25TTS12PbF, VS-25TTS12-M3	1200	1200	

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS
			TYP.	MAX.	
Maximum average on-state current	$I_{T(AV)}$	$T_C = 93\text{ }^{\circ}\text{C}$ , 180° conduction half sine wave	16		A
Maximum RMS on-state current	$I_{RMS}$		25		
Maximum peak, one-cycle, non-repetitive surge current	$I_{TSM}$	10 ms sine pulse, rated $V_{RRM}$ applied	270		
		10 ms sine pulse, no voltage reapplied	320		
Maximum $I^2t$ for fusing	$I^2t$	10 ms sine pulse, rated $V_{RRM}$ applied	365		$A^2s$
		10 ms sine pulse, no voltage reapplied	515		
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1$ to 10 ms, no voltage reapplied	5152		$A^2\sqrt{s}$
Maximum on-state voltage drop	$V_{TM}$	16 A, $T_J = 25\text{ }^{\circ}\text{C}$	1.25		V
On-state slope resistance	$r_t$	$T_J = 125\text{ }^{\circ}\text{C}$	12.0		$m\Omega$
Threshold voltage	$V_{T(TO)}$		1.0		V
Maximum reverse and direct leakage current	$I_{RM}/I_{DM}$	$T_J = 25\text{ }^{\circ}\text{C}$	$V_R = \text{Rated } V_{RRM}/V_{DRM}$		mA
		$T_J = 125\text{ }^{\circ}\text{C}$			
Holding current	$I_H$	Anode supply = 6 V, resistive load, initial $I_T = 1\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	150	
Maximum latching current	$I_L$	Anode supply = 6 V, resistive load, $T_J = 25\text{ }^{\circ}\text{C}$	200		
Maximum rate of rise of off-state voltage	$dV/dt$	$T_J = T_J \text{ max.}$ , linear to $80\text{ }^{\circ}\text{C}$ , $V_{DRM} = R_g - k = \text{Open}$	500		V/ $\mu s$
Maximum rate of rise of turned-on current	$dI/dt$		150		A/ $\mu s$

**TRIGGERING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$		8.0	W
Maximum average gate power	$P_{G(AV)}$		2.0	
Maximum peak positive gate current	$+I_{GM}$		1.5	A
Maximum peak negative gate voltage	$-V_{GM}$		10	V
Maximum required DC gate current to trigger	$I_{GT}$	Anode supply = 6 V, resistive load, $T_J = -10\text{ }^{\circ}\text{C}$	60	mA
		Anode supply = 6 V, resistive load, $T_J = 25\text{ }^{\circ}\text{C}$	45	
		Anode supply = 6 V, resistive load, $T_J = 125\text{ }^{\circ}\text{C}$	20	
Maximum required DC gate voltage to trigger	$V_{GT}$	Anode supply = 6 V, resistive load, $T_J = -10\text{ }^{\circ}\text{C}$	2.5	V
		Anode supply = 6 V, resistive load, $T_J = 25\text{ }^{\circ}\text{C}$	2.0	
		Anode supply = 6 V, resistive load, $T_J = 125\text{ }^{\circ}\text{C}$	1.0	
Maximum DC gate voltage not to trigger	$V_{GD}$	$T_J = 125\text{ }^{\circ}\text{C}$ , $V_{DRM} = \text{Rated value}$	0.25	mA
Maximum DC gate current not to trigger	$I_{GD}$		2.0	

**SWITCHING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical turn-on time	$t_{gt}$	$T_J = 25\text{ }^{\circ}\text{C}$	0.9	$\mu s$
Typical reverse recovery time	$t_{rr}$	$T_J = 125\text{ }^{\circ}\text{C}$	4	
Typical turn-off time	$t_q$		110	



THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T <sub>J</sub> , T <sub>Stg</sub>		-40 to 125	°C
Maximum thermal resistance, junction to case	R <sub>thJC</sub>	DC operation	1.1	°C/W
Maximum thermal resistance, junction to ambient	R <sub>thJA</sub>		62	
Typical thermal resistance, case to heatsink	R <sub>thCS</sub>	Mounting surface, smooth and greased	0.5	
Approximate weight			2	g
			0.07	oz.
Mounting torque			6 (5)	kgf · cm (lbf · in)
			12 (10)	
Marking device		Case style TO-220AB	25TTS08	
			25TTS12	

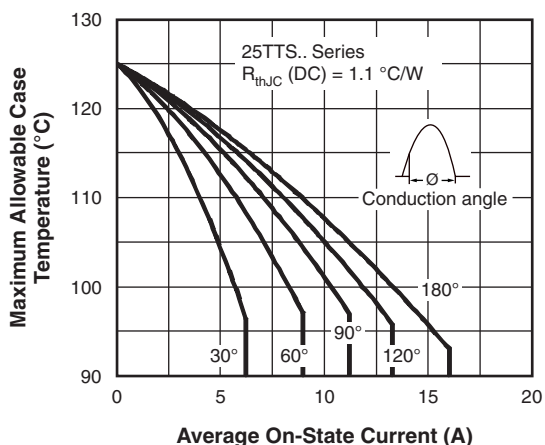


Fig. 1 - Current Rating Characteristics

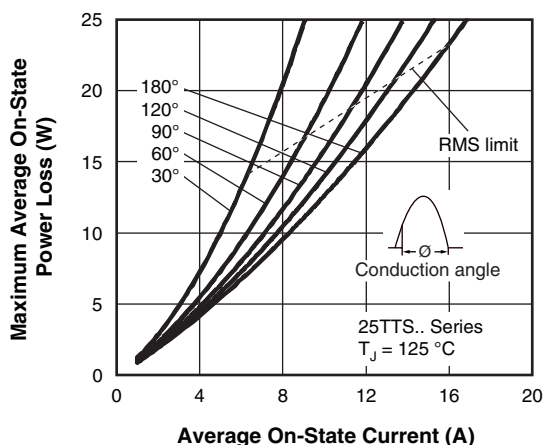


Fig. 3 - On-State Power Loss Characteristics

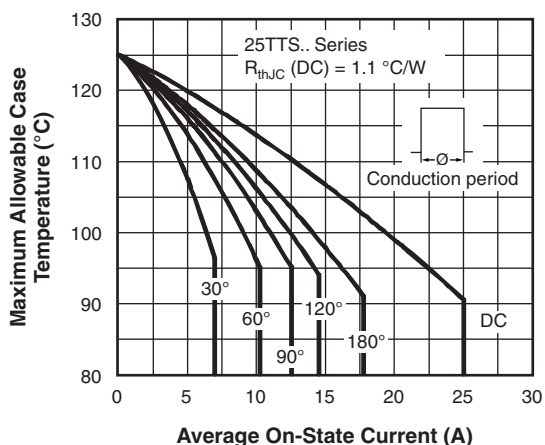


Fig. 2 - Current Rating Characteristics

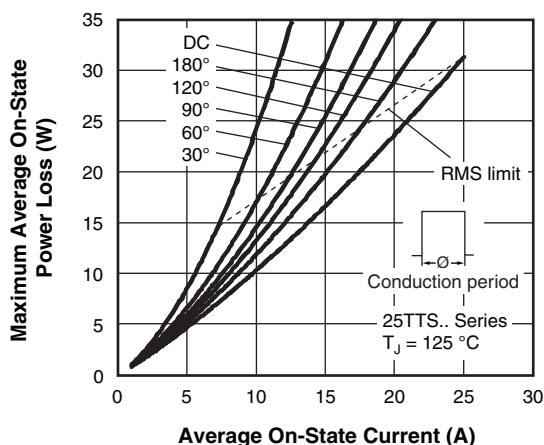


Fig. 4 - On-State Power Loss Characteristics

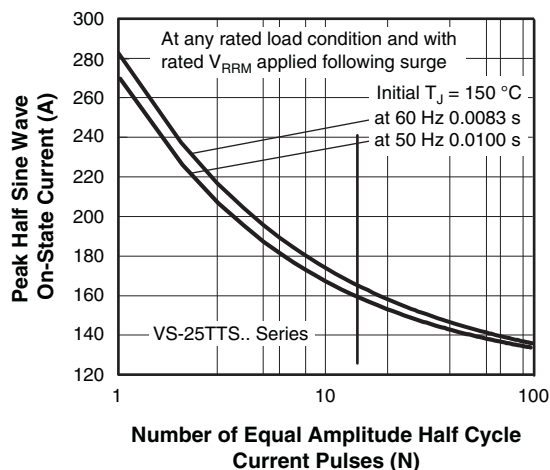


Fig. 5 - Maximum Non-Repetitive Surge Current

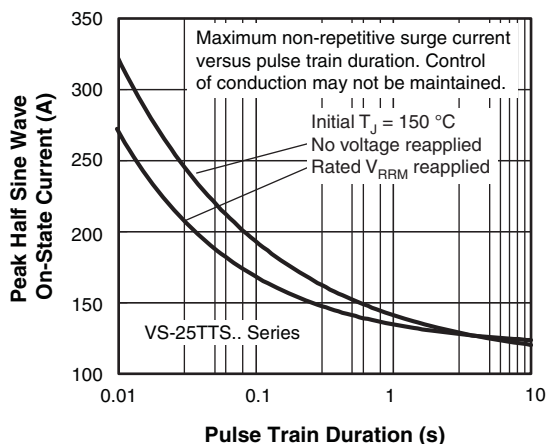


Fig. 6 - Maximum Non-Repetitive Surge Current

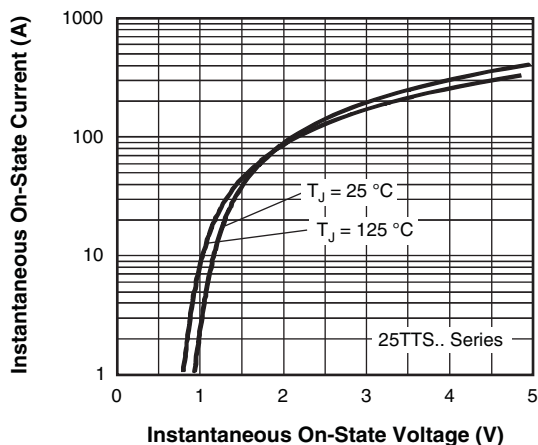


Fig. 7 - On-State Voltage Drop Characteristics

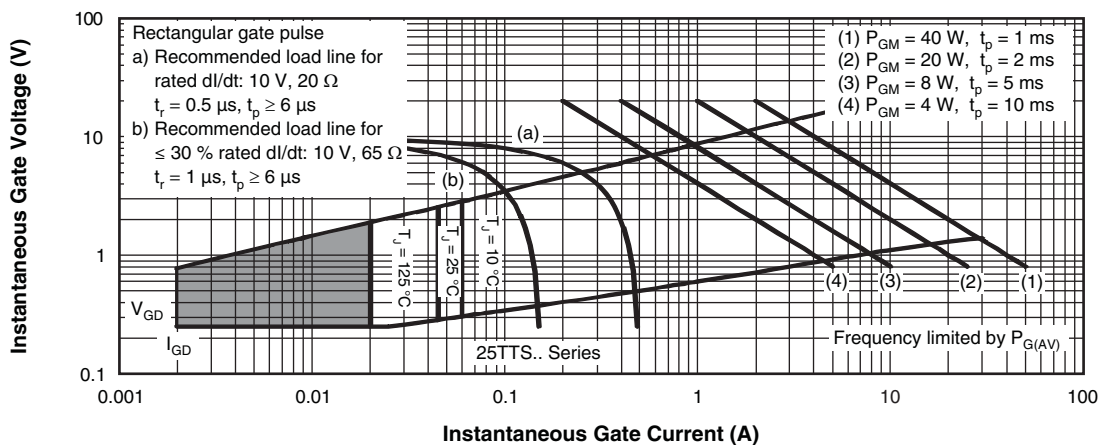


Fig. 8 - Gate Characteristics

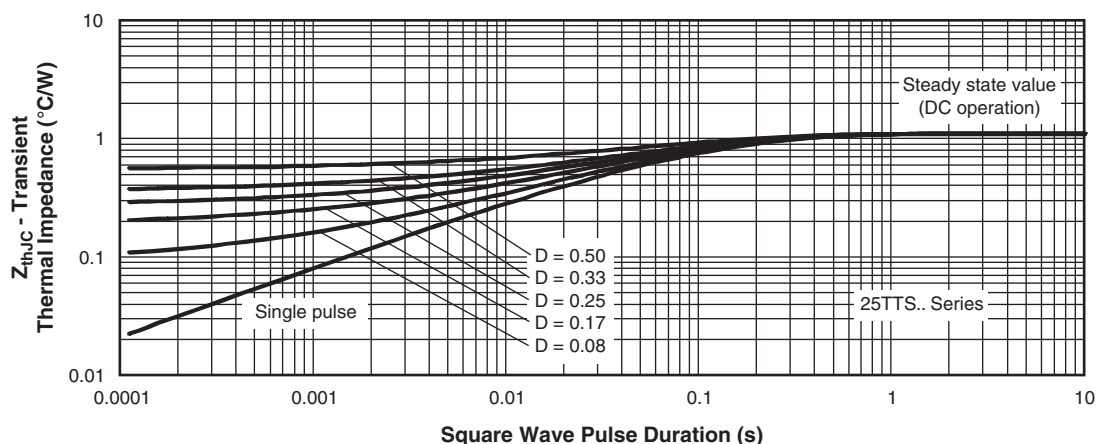


Fig. 9 - Thermal Impedance  $Z_{thJC}$  Characteristics

## ORDERING INFORMATION TABLE

Device code	VS-	25	T	T	S	12	PbF
	1	2	3	4	5	6	7
1	Vishay Semiconductors product						
2	Current rating (25 = 25 A)						
3	Circuit configuration: T = Single thyristor						
4	Package: T = TO-220AB						
5	Type of silicon: S = Standard recovery rectifier						
6	Voltage rating						
7	Environmental digit: PbF = Lead (Pb)-free and RoHS compliant -M3 = Halogen-free, RoHS compliant, and terminations lead (Pb)-free						

08 = 800 V  
12 = 1200 V

ORDERING INFORMATION (Example)			
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-25TTS08PbF	50	1000	Antistatic plastic tubes
VS-25TTS08-M3	50	1000	Antistatic plastic tubes
VS-25TTS12PbF	50	1000	Antistatic plastic tubes
VS-25TTS12-M3	50	1000	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS		
Dimensions		<a href="http://www.vishay.com/doc?95222">www.vishay.com/doc?95222</a>
Part marking information	TO-220AB PbF	<a href="http://www.vishay.com/doc?95225">www.vishay.com/doc?95225</a>
	TO-220AB -M3	<a href="http://www.vishay.com/doc?95028">www.vishay.com/doc?95028</a>

## TO-220AB

**DIMENSIONS** in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
E	10.11	10.51	0.398	0.414	3, 6
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° to 93°		

### Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, except A2 (maximum) and D2 (minimum) where dimensions are derived from the actual package outline



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