

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = +25^\circ C$
Q1	30V	25mΩ @ $V_{GS} = 10V$	6.5A
		29mΩ @ $V_{GS} = 4.5V$	6.1A
Q2	-30V	28mΩ @ $V_{GS} = -10V$	-6.2A
		38mΩ @ $V_{GS} = -4.5V$	-5.3A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

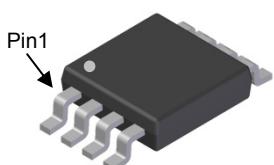
- DC-DC Converters
- Power Management Functions
- Backlighting

Features and Benefits

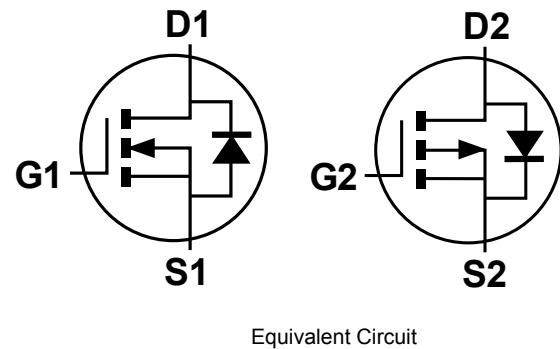
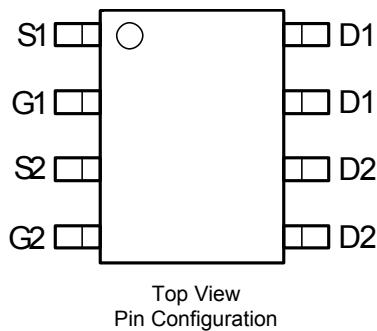
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.074 grams (approximate)



Top View



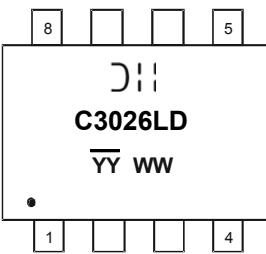
Ordering Information (Note 4)

Part Number	Case	Packaging
DMC3026LSD-13	SO-8	2,500/Tape & Reel

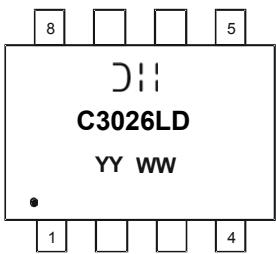
Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

DII = Manufacturer's Marking

C3026LD = Product Type Marking Code

YYWW = Date Code Marking

YY or YY = Year (ex: 14 = 2014)

WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings – Q1 and Q2 (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Q1	Q2	Units
Drain-Source Voltage	V_{DSS}	30	-30	V
Gate-Source Voltage	V_{GSS}	± 20	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	6.5 5.2
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	8.2 6.7
Maximum Body Diode Forward Current (Note 6)	I_S	2.2	-2.5	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)	I_{DM}	40	-40	A
Avalanche Current (Notes 7) $L = 0.1\text{mH}$	I_{AS}	14.5	22	A
Avalanche Energy (Notes 7) $L = 0.1\text{mH}$	E_{AS}	10.5	25	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	1.2	W
		0.8	
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	102	°C/W
		62	
Total Power Dissipation (Note 6)	P_D	1.6	W
		1.0	
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	78	°C/W
		47	
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	14.5	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics – Q1 (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	19	25	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 6\text{A}$
		—	22	29		$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 1.3\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	641	—	pF	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	66	—		
Reverse Transfer Capacitance	C_{rss}	—	51	—		
Gate Resistance	R_G	—	2.2	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	6	—	nC	$V_{DS} = 15\text{V}, I_D = 10\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	13.2	—		
Gate-Source Charge	Q_{gs}	—	1.7	—		
Gate-Drain Charge	Q_{gd}	—	2.2	—		
Turn-On Delay Time	$t_{D(on)}$	—	3.3	—	nS	$V_{GS} = 10\text{V}, V_{DD} = 15\text{V}, R_G = 6\Omega, I_D = 1\text{A}$
Turn-On Rise Time	t_r	—	4.4	—		
Turn-Off Delay Time	$t_{D(off)}$	—	22.3	—		
Turn-Off Fall Time	t_f	—	5.3	—		

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

7. UIS in production with $L = 0.1\text{mH}$, starting $T_A = +25^\circ\text{C}$.

8. Short duration pulse test used to minimize self-heating effect.

9. Guaranteed by design. Not subject to product testing.

Electrical Characteristics – Q2 (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$\text{V}_{\text{DS}} = -24\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$\text{V}_{\text{GS}} = \pm 20\text{V}$, $\text{V}_{\text{DS}} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$\text{V}_{\text{GS}(\text{th})}$	-1	—	-3	V	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$, $\text{I}_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$\text{R}_{\text{DS}(\text{ON})}$	—	21	28	$\text{m}\Omega$	$\text{V}_{\text{GS}} = -10\text{V}$, $\text{I}_D = -6\text{A}$
		—	29	38		$\text{V}_{\text{GS}} = -4.5\text{V}$, $\text{I}_D = -5\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_S = -1.3\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1241	—	pF	$\text{V}_{\text{DS}} = -15\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	146	—		
Reverse Transfer Capacitance	C_{rss}	—	110	—	nC	$\text{V}_{\text{DS}} = -15\text{V}$, $\text{I}_D = -7\text{A}$
Gate Resistance	R_{G}	—	14.8	—		
Total Gate Charge ($\text{V}_{\text{GS}} = -4.5\text{V}$)	Q_{g}	—	10.9	—	nS	$\text{V}_{\text{GS}} = -10\text{V}$, $\text{V}_{\text{DD}} = -15\text{V}$, $\text{R}_{\text{GEN}} = 6\Omega$, $\text{I}_D = -7\text{A}$
Total Gate Charge ($\text{V}_{\text{GS}} = -10\text{V}$)	Q_{g}	—	22	—		
Gate-Source Charge	Q_{gs}	—	3.5	—	nS	$\text{V}_{\text{GS}} = -10\text{V}$, $\text{V}_{\text{DD}} = -15\text{V}$, $\text{R}_{\text{GEN}} = 6\Omega$, $\text{I}_D = -7\text{A}$
Gate-Drain Charge	Q_{gd}	—	4.7	—		
Turn-On Delay Time	$\text{t}_{\text{D}(\text{on})}$	—	9.7	—		
Turn-On Rise Time	t_{r}	—	17.1	—		
Turn-Off Delay Time	$\text{t}_{\text{D}(\text{off})}$	—	60.5	—	nS	$\text{V}_{\text{GS}} = -10\text{V}$, $\text{V}_{\text{DD}} = -15\text{V}$, $\text{R}_{\text{GEN}} = 6\Omega$, $\text{I}_D = -7\text{A}$
Turn-Off Fall Time	t_{f}	—	40.4	—		

Notes: 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing.

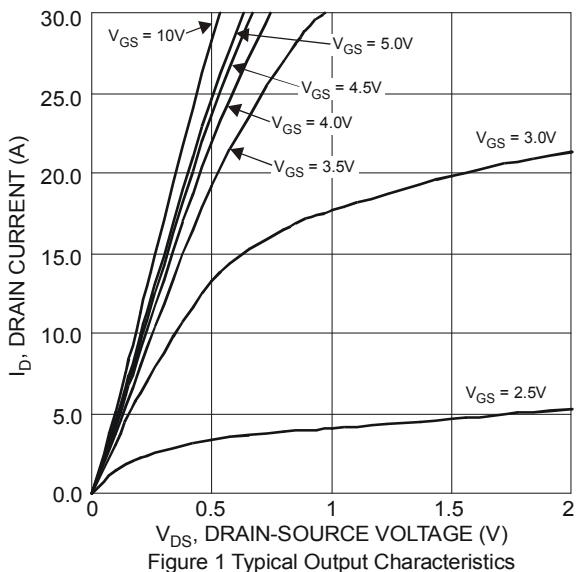


Figure 1 Typical Output Characteristics

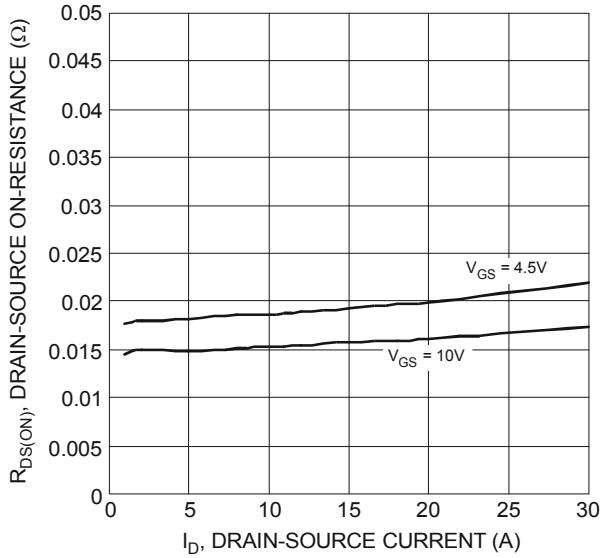


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

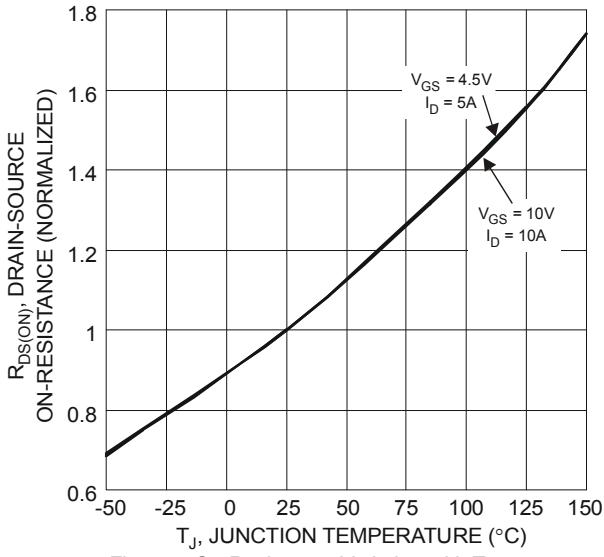


Figure 5 On-Resistance Variation with Temperature

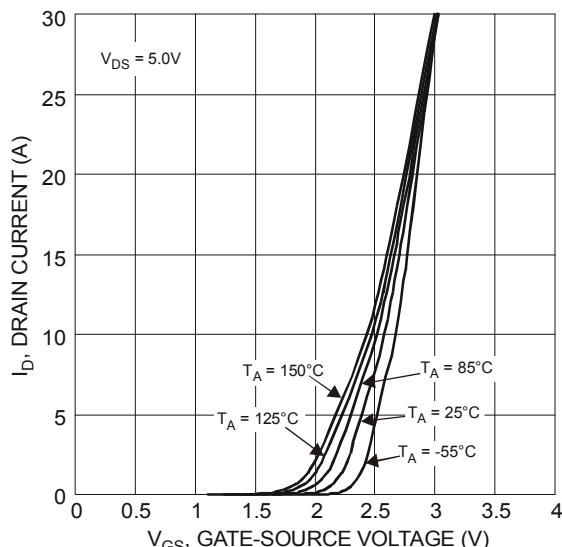


Figure 2 Typical Transfer Characteristics

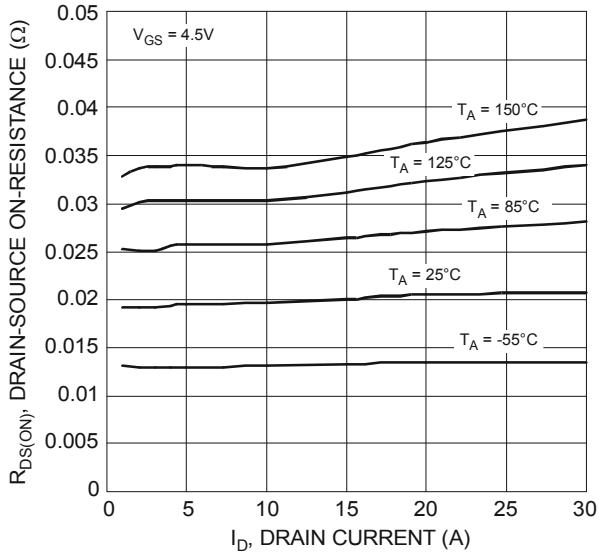


Figure 4 Typical On-Resistance vs.
Drain Current and Temperature

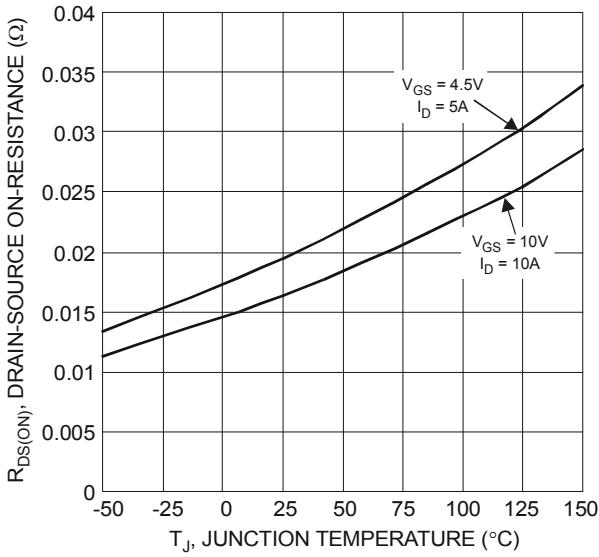


Figure 6 On-Resistance Variation with Temperature

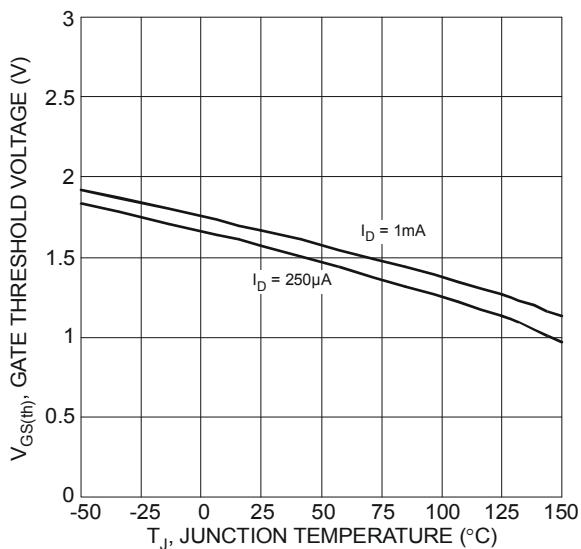


Figure 7 Gate Threshold Variation vs. Ambient Temperature

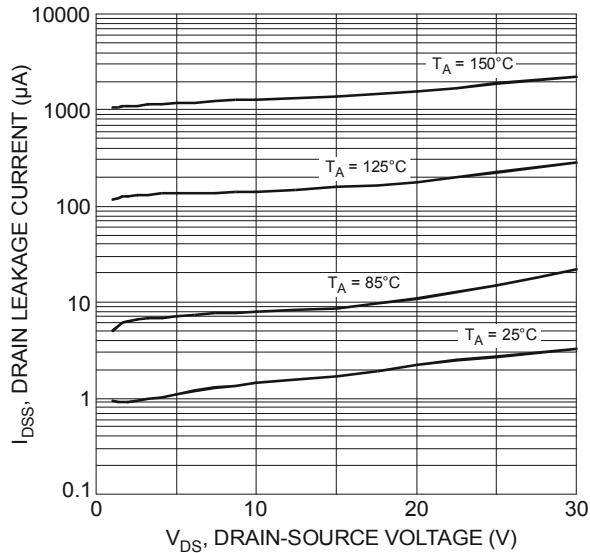


Figure 9 Typical Drain-Source Leakage Current vs. Voltage

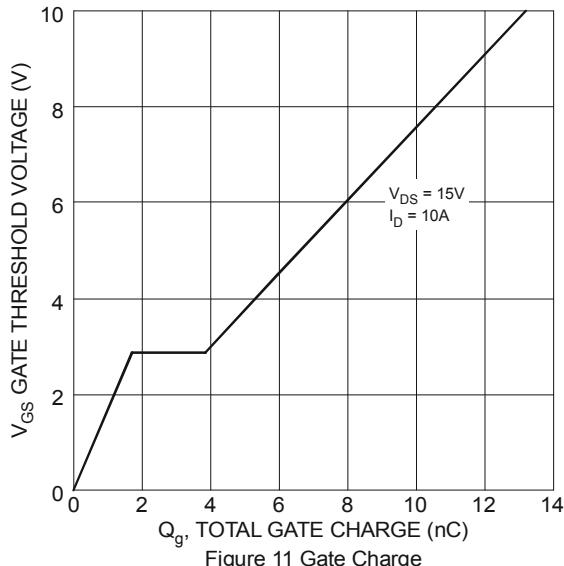


Figure 11 Gate Charge

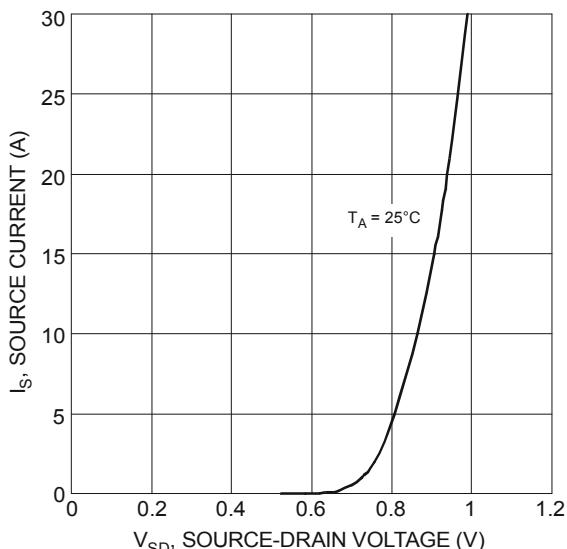


Figure 8 Diode Forward Voltage vs. Current

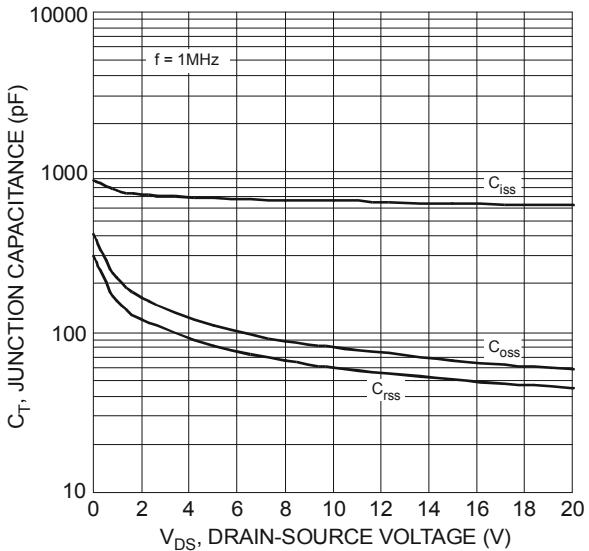


Figure 10 Typical Junction Capacitance

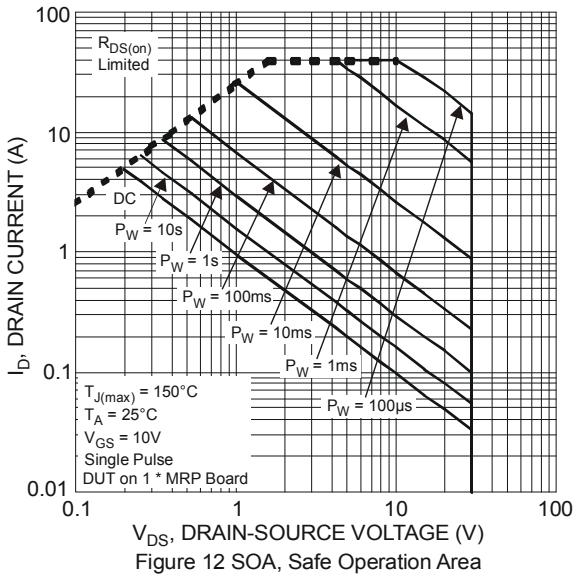


Figure 12 SOA, Safe Operation Area

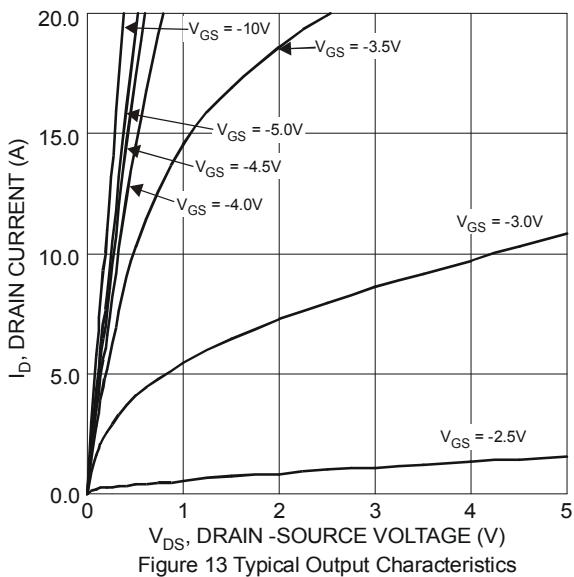


Figure 13 Typical Output Characteristics

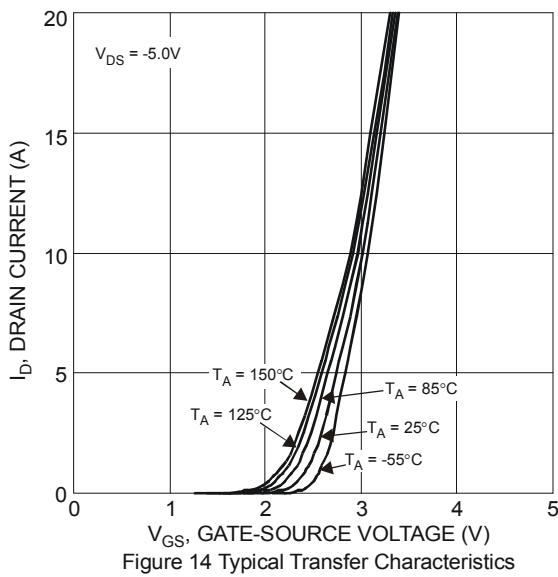


Figure 14 Typical Transfer Characteristics

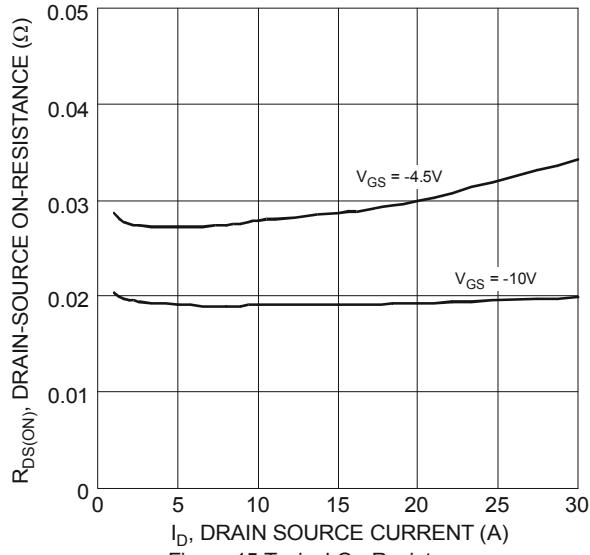


Figure 15 Typical On-Resistance vs.
Drain Current and Gate Voltage

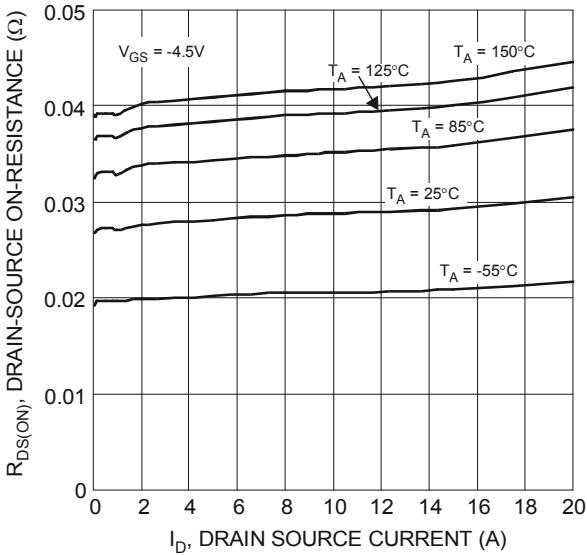


Figure 16 Typical On-Resistance vs.
Drain Current and Temperature

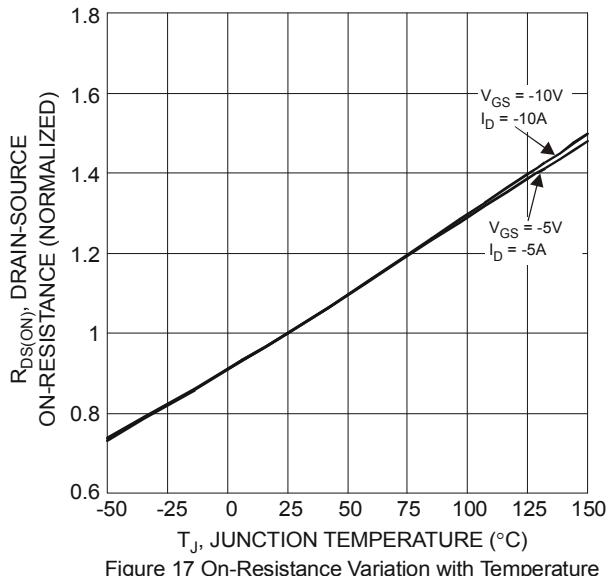


Figure 17 On-Resistance Variation with Temperature

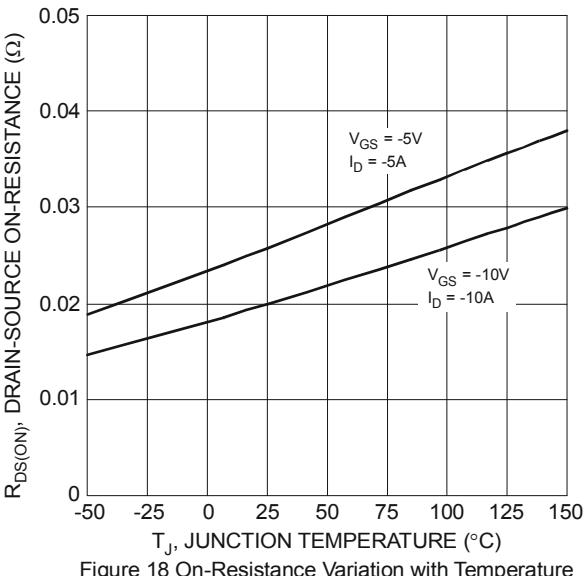


Figure 18 On-Resistance Variation with Temperature

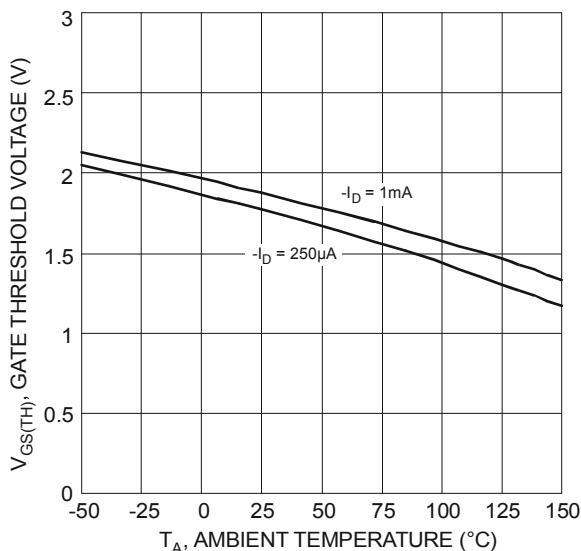


Figure 19 Gate Threshold Variation vs. Ambient Temperature

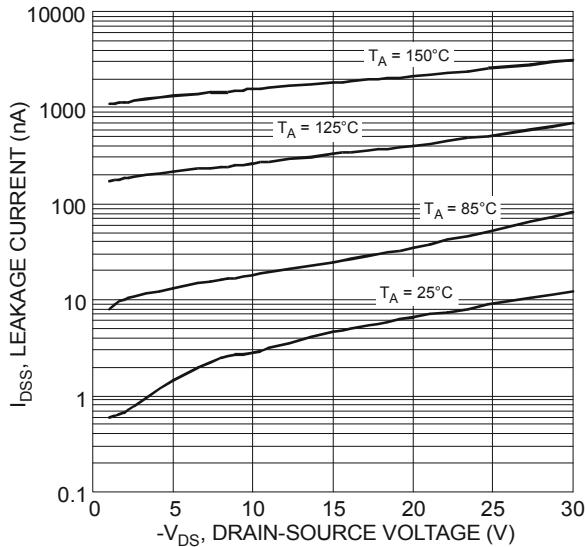


Figure 21 Typical Drain-Source Leakage Current vs. Voltage

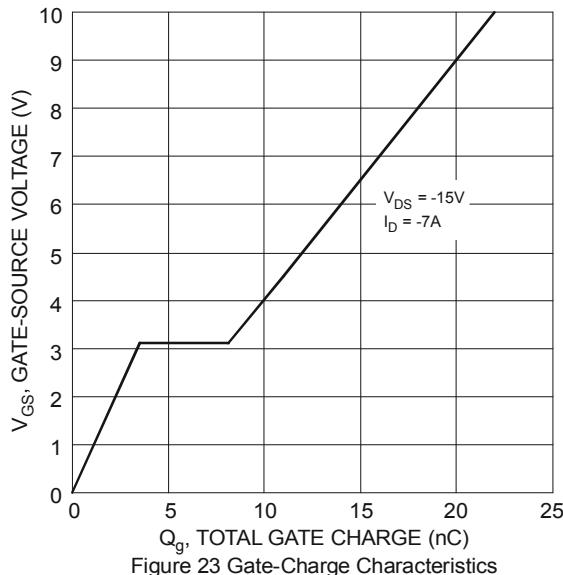


Figure 23 Gate-Charge Characteristics

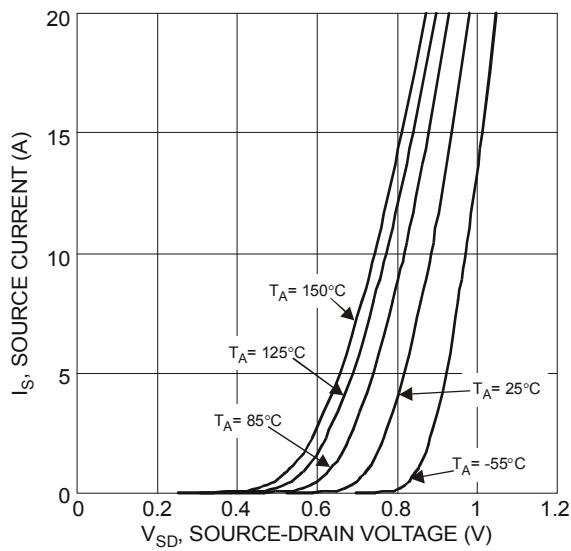


Figure 20 Diode Forward Voltage vs. Current

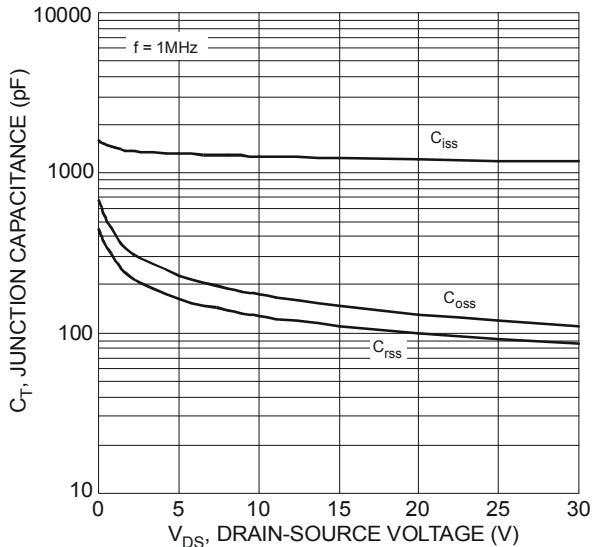


Figure 22 Typical Junction Capacitance

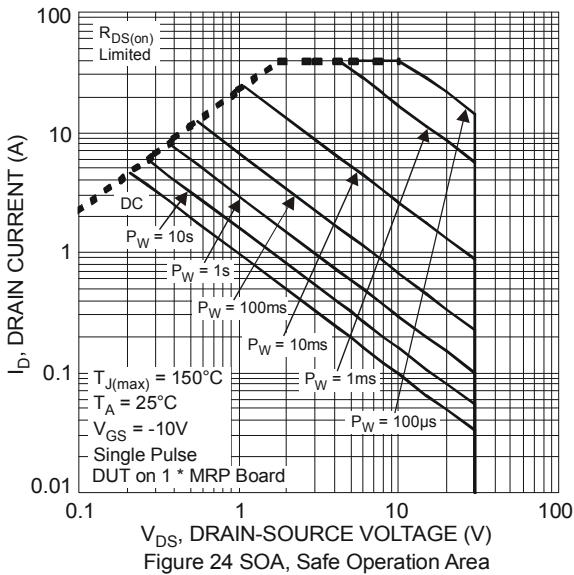
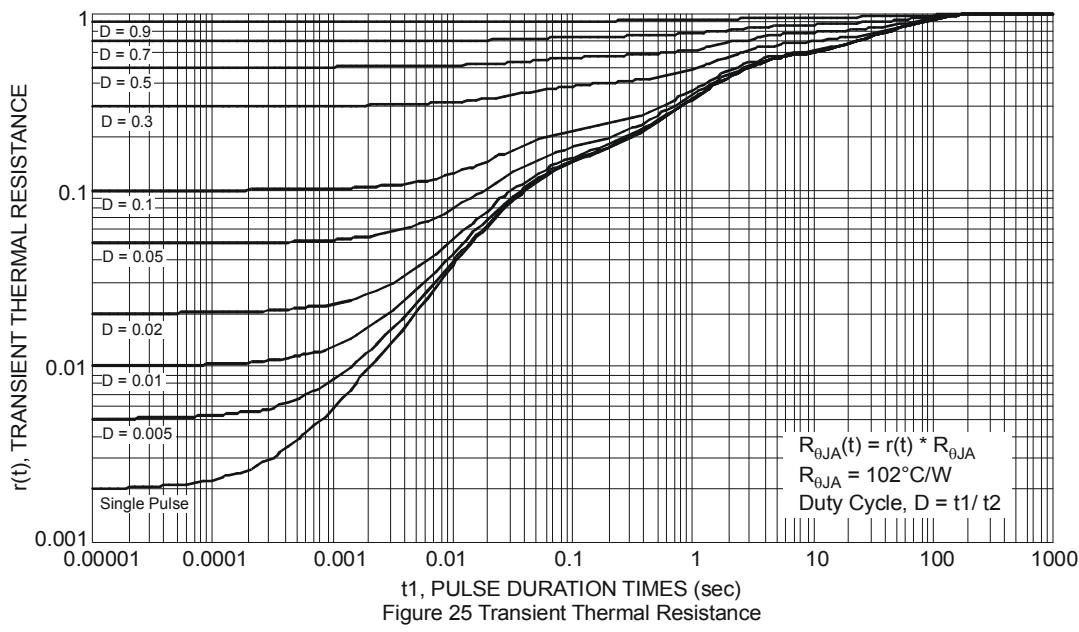
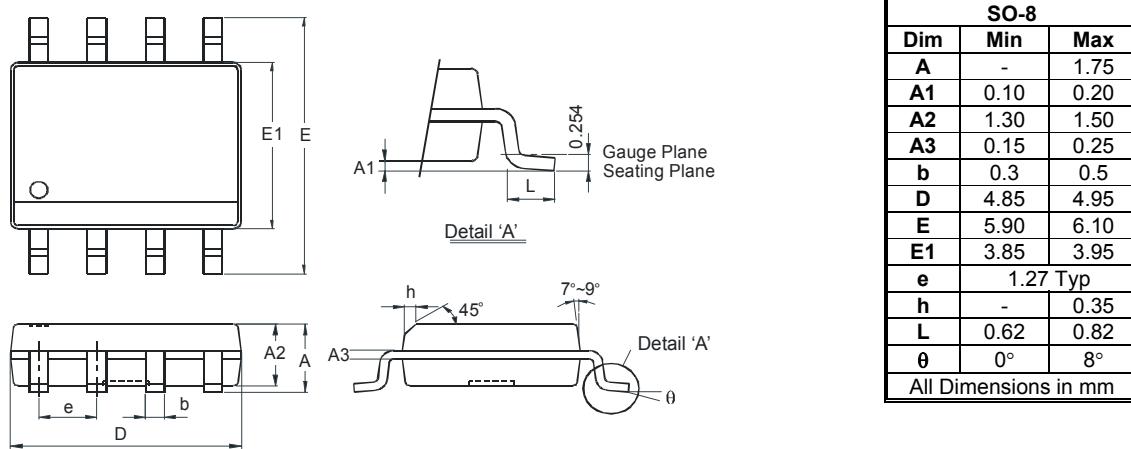


Figure 24 SOA, Safe Operation Area



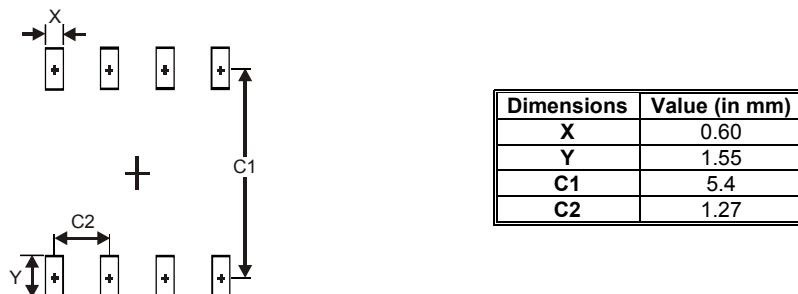
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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