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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H7N0401LD, H7N0401LS, H7N0401LM

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

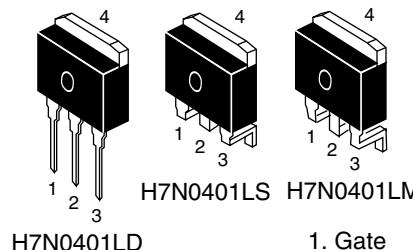
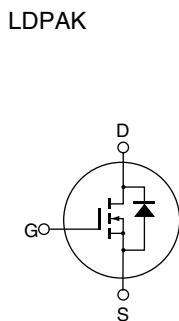
ADE-208-1527C (Z)

4th. Edition
May 2002

Features

- Low on-resistance
 $R_{DS(on)} = 3.1 \text{ m}\Omega \text{ typ.}$
- 4.5 V gate drive devices
- High Speed Switching

Outline



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	40	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	95	A
Drain peak current	I _D (pulse) ^{Note1}	380	A
Body-drain diode reverse drain current	I _{DR}	95	A
Avalanche current	I _{AP} ^{Note3}	70	A
Avalanche energy	E _{AR} ^{Note3}	650	mJ
Channel dissipation	Pch ^{Note2}	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%

2. Value at Tc = 25°C

3. Value at Tch = 25°C, Rg ≥ 50 Ω

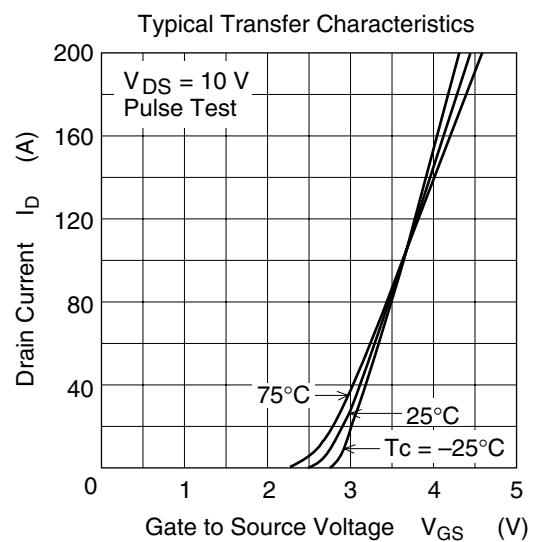
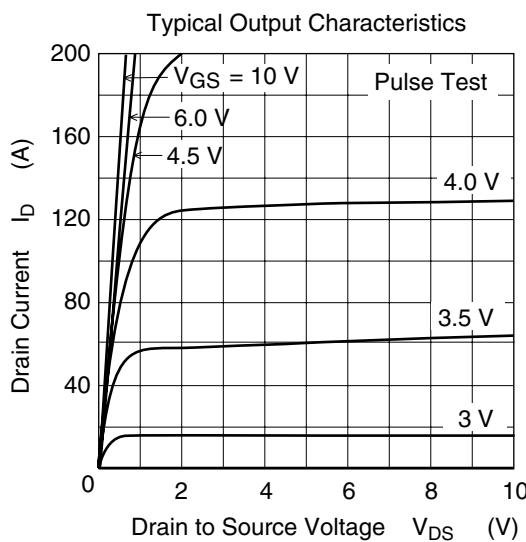
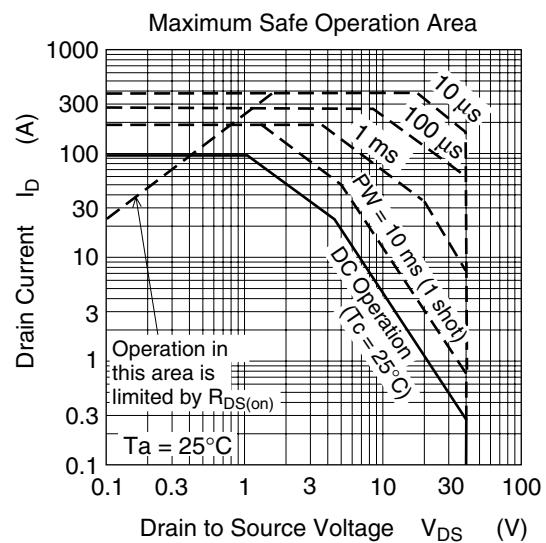
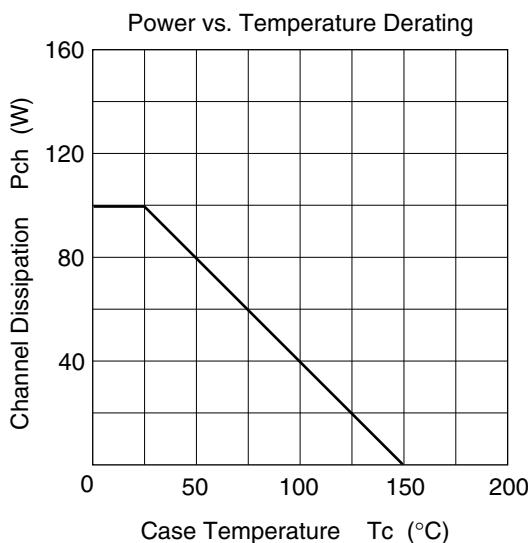
Electrical Characteristics

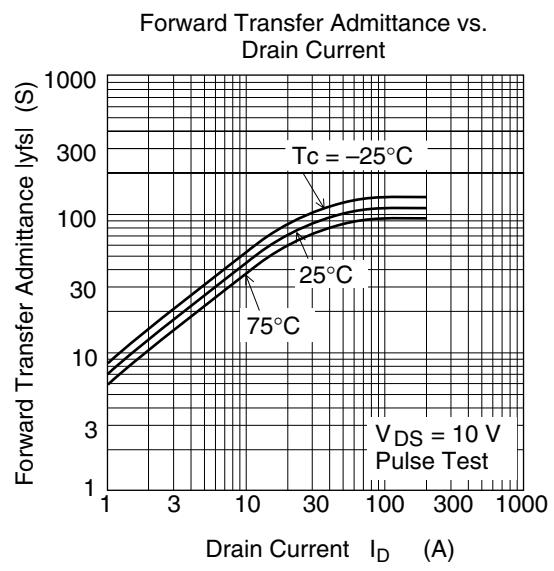
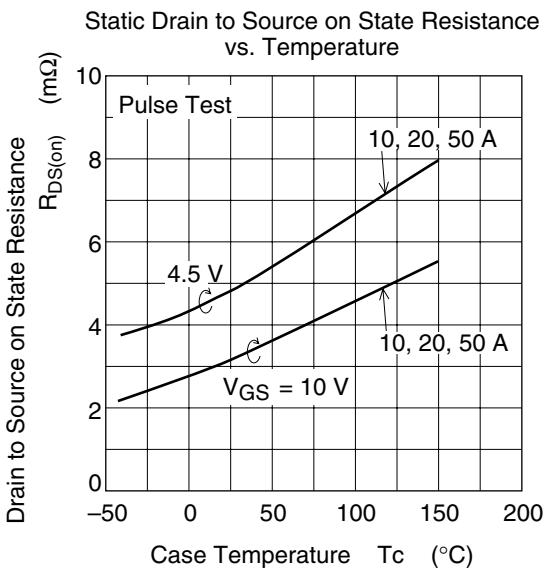
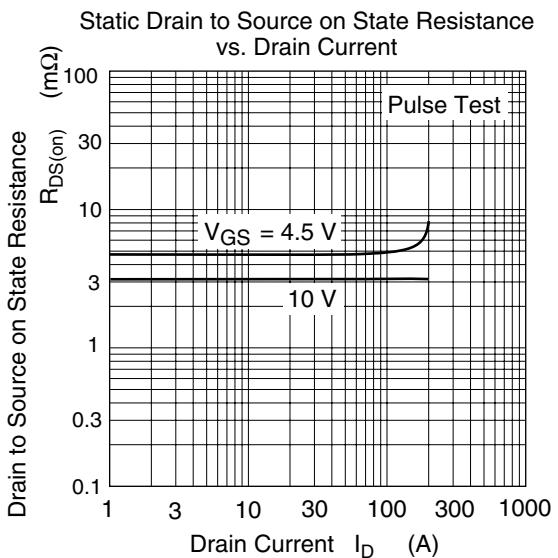
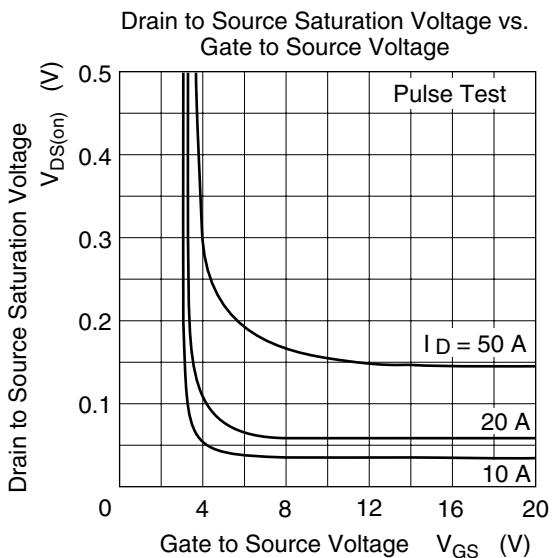
(Ta = 25°C)

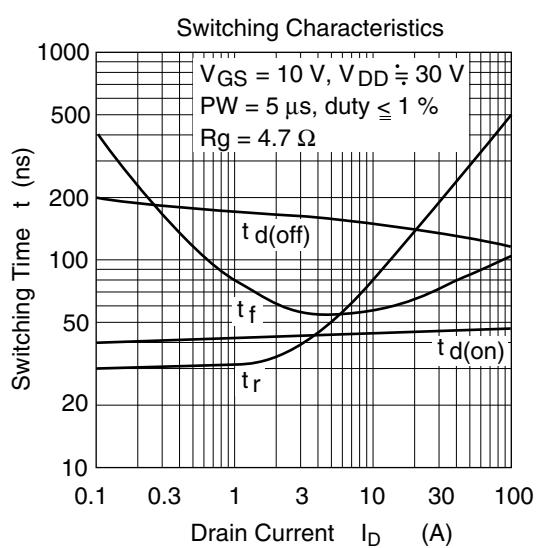
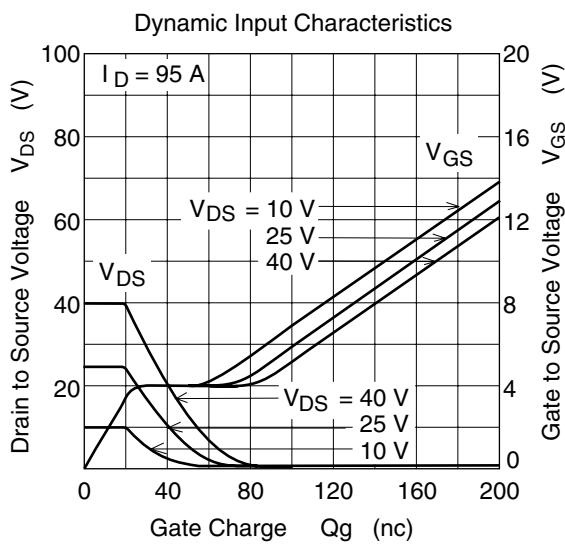
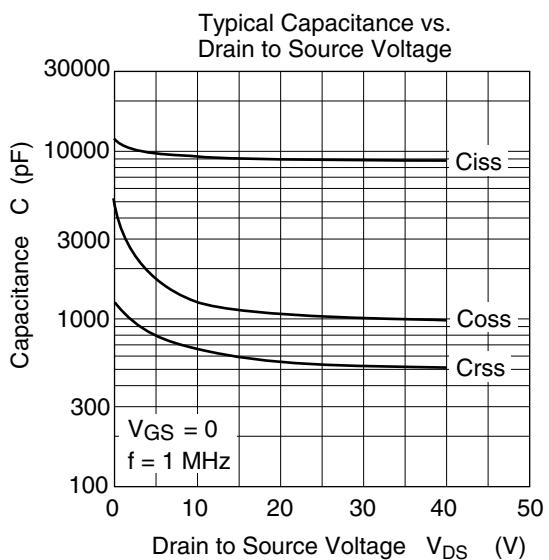
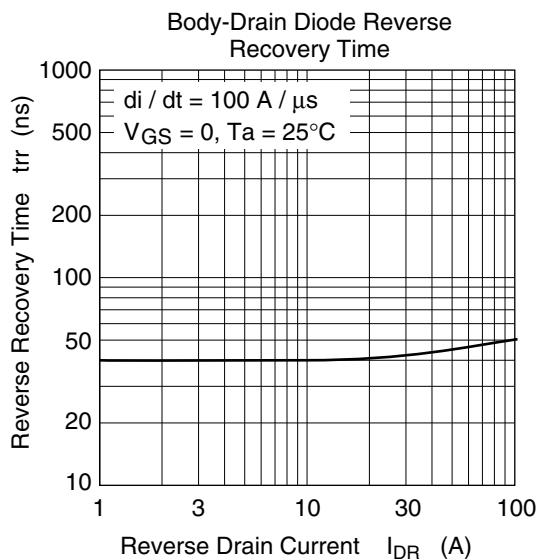
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	40	—	—	V	I _D = 10 mA, V _{GS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 40 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	μA	V _{GS} = ±20 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	1.5	—	2.5	V	V _{DS} = 10 V, I _D = 1 mA ^{Note 1}
Forward transfer admittance	y _{fs}	60	100	—	S	I _D = 47.5 A, V _{DS} = 10 V ^{Note 1}
Static drain to source on state resistance	R _{DS(on)}	—	3.1	4.2	mΩ	I _D = 47.5 A, V _{GS} = 10 V ^{Note 1}
Static drain to source on state resistance	R _{DS(on)}	—	4.8	7.0	mΩ	I _D = 47.5 A, V _{GS} = 4.5 V ^{Note 1}
Input capacitance	C _{iss}	—	9300	—	pF	V _{DS} = 10 V
Output capacitance	C _{oss}	—	1300	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	670	—	pF	f = 1 MHz
Total gate charge	Q _g	—	160	—	nc	V _{DD} = 25 V
Gate to source charge	Q _{gs}	—	36	—	nc	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	40	—	nc	I _D = 95 A
Turn-on delay time	t _{d(on)}	—	45	—	ns	V _{GS} = 10 V
Rise time	t _r	—	270	—	ns	I _D = 47.5 A
Turn-off delay time	t _{d(off)}	—	130	—	ns	R _L = 0.63 Ω
Fall time	t _f	—	85	—	ns	R _G = 4.7 Ω
Body-drain diode forward voltage	V _{DF}	—	0.95	—	V	I _F = 95 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	50	—	ns	I _F = 95 A, V _{GS} = 0 dI/dt = 100 A/μs

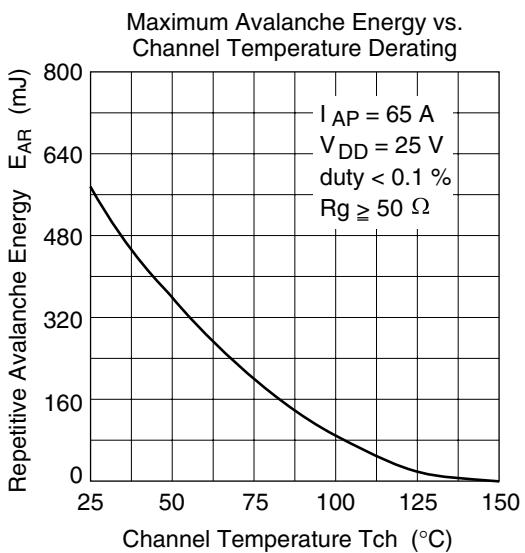
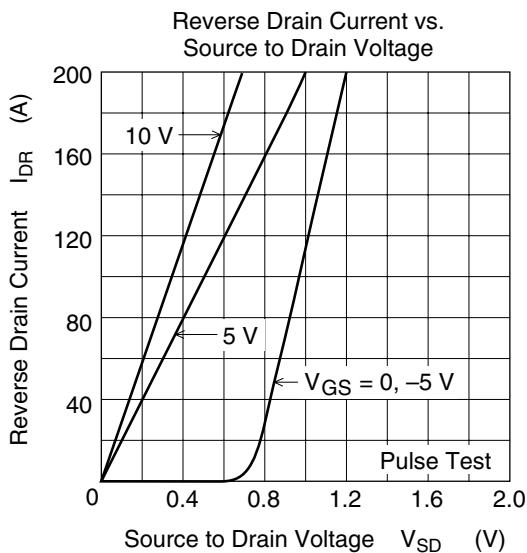
Notes: 1. Pulse test

Main Characteristics

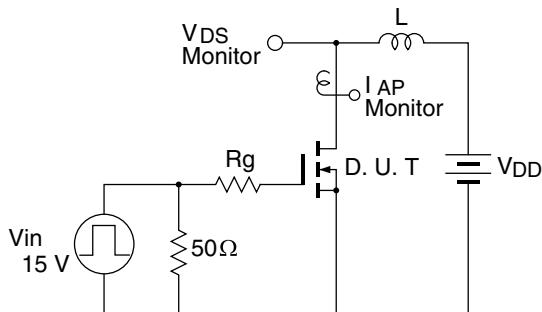




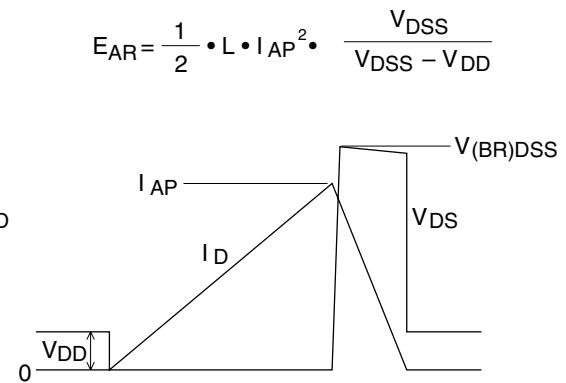


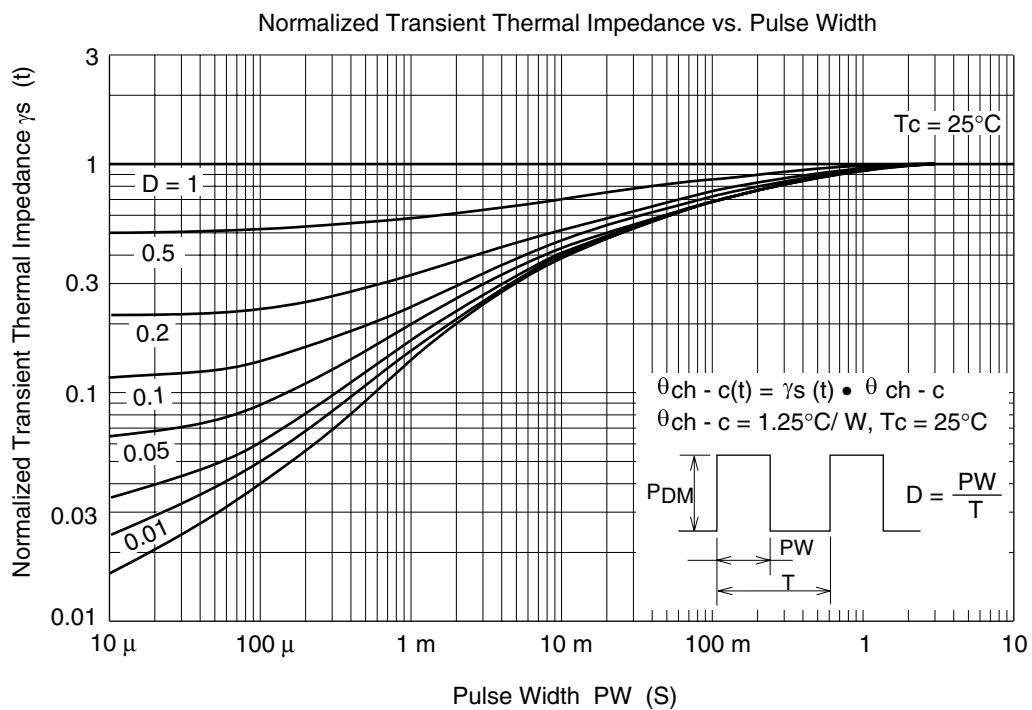


Avalanche Test Circuit

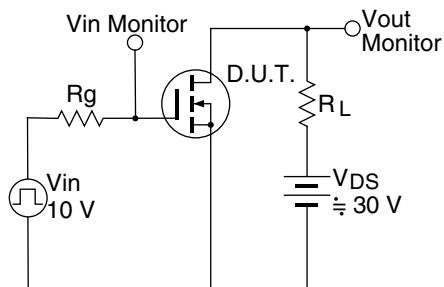


Avalanche Waveform

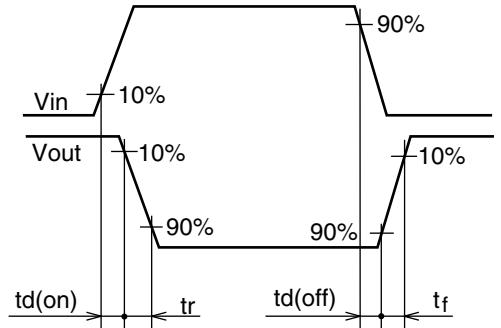




Switching Time Test Circuit

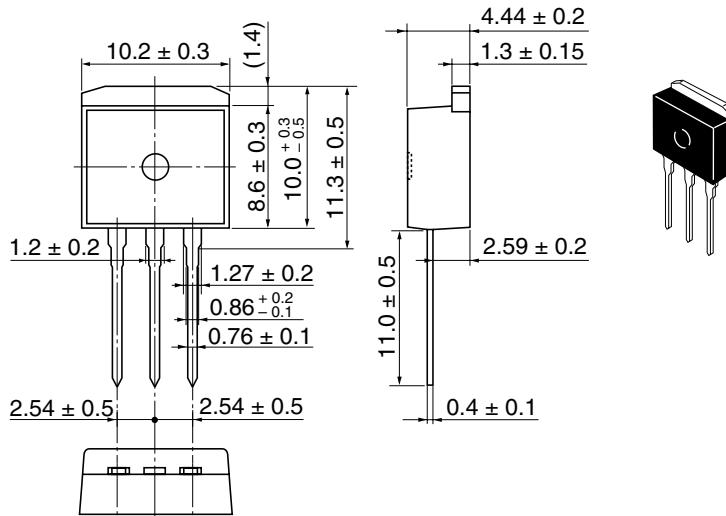


Waveform



Package Dimensions

As of January, 2002
Unit: mm

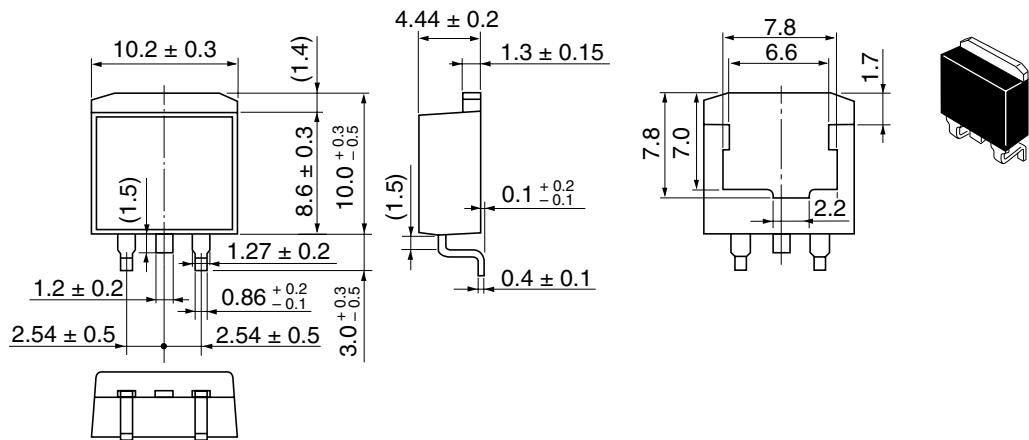


Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

H7N0401LD, H7N0401LS, H7N0401LM

As of January, 2002

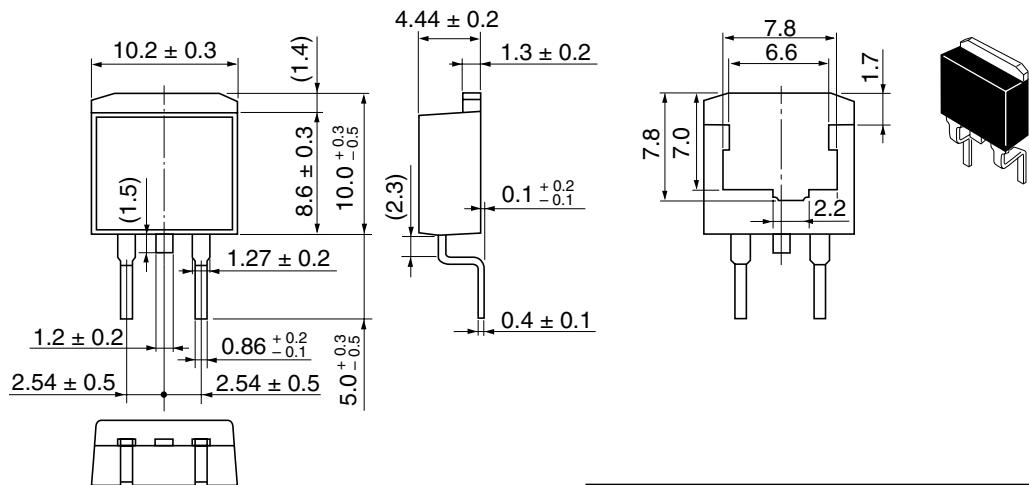
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

As of January, 2002

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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