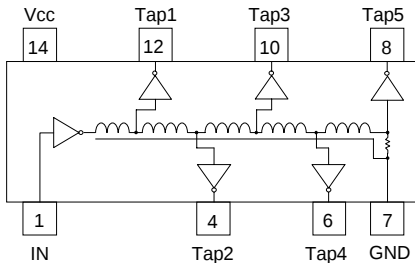


DTZM Series FAST / TTL Buffered 5-Tap Delay Modules

- 14-Pin Package Commercial and Mil-Grade Versions
- FAST/TTL Logic Buffered
- 5 Equal Delay Taps
- Operating Temperature Ranges 0°C to +70°C, or -55°C to +125°C
- 8-Pin Versions: FAMDM Series
SIP Versions: FSIDM Series
- Low Voltage CMOS Versions refer to LVMDM / LVIDM Series

DTZM 14-Pin Schematic



Electrical Specifications at 25°C

TTL Buffered 5 Tap Modules		Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
Part Number	Mil-Grade P/N	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
DTZM1-9	DTZM3-9M	5.0	6.0	7.0	8.0	9 ± 1.0	** 1.0 ± 0.5
DTZM1-13	DTZM3-13M	5.0	7.0	9.0	11.0	13 ± 1.5	** 2.0 ± 0.8
DTZM1-17	DTZM3-17M	5.0	8.0	11.0	14.0	17 ± 1.5	3.0 ± 1.0
DTZM1-20	DTZM3-20M	4.0	8.0	12.0	16.0	20 ± 1.5	4.0 ± 1.5
DTZM1-25	DTZM3-25M	5.0	10.0	15.0	20.0	25 ± 2.0	5.0 ± 2.0
DTZM1-30	DTZM3-30M	6.0	12.0	18.0	24.0	30 ± 2.0	6.0 ± 2.0
DTZM1-35	DTZM3-35M	7.0	14.0	21.0	28.0	35 ± 2.0	7.0 ± 2.0
DTZM1-40	DTZM3-40M	8.0	16.0	24.0	32.0	40 ± 2.0	8.0 ± 2.0
DTZM1-45	DTZM3-45M	9.0	18.0	27.0	36.0	45 ± 2.25	9.0 ± 2.0
DTZM1-50	DTZM3-50M	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
DTZM1-60	DTZM3-60M	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
DTZM1-75	DTZM3-75M	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
DTZM1-80	DTZM3-80M	16.0	32.0	48.0	64.0	80 ± 4.0	16 ± 2.5
DTZM1-100	DTZM3-100M	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
DTZM1-125	DTZM3-125M	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
DTZM1-150	DTZM3-150M	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
DTZM1-200	DTZM3-200M	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
DTZM1-250	DTZM3-250M	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
DTZM1-300	DTZM3-300M	60.0	120.0	180.0	240.0	300 ± 15.0	60 ± 6.0
DTZM1-350	DTZM3-350M	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 7.0
DTZM1-400	DTZM3-400M	80.0	160.0	240.0	320.0	400 ± 20.0	80 ± 8.0
DTZM1-500	DTZM3-500M	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10.0
DTZM1-800	DTZM3-800M	160.0	320.0	480.0	640.0	800 ± 40.0	160 ± 16.0

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
 Input Pulse Voltage 3.20V
 Input Pulse Rise Time 3.0 ns max.
 Input Pulse Width / Period 1000 / 2000 ns
 1. Measurements made at 25°C
 2. Delay Times measured at 1.50V level of leading edge.
 3. Rise Times measured from 0.75V to 2.40V.
 4. 10pf probe and fixture load on output under test.

** These part numbers do not have 5 equal taps.
 Tap-to-Tap Delays reference Tap 1.

Dimensions in Inches (mm)

Commercial Grade 14-Pin Package with Unused Leads Removed
 as per Schematic. (For Mil-Grade DTZM3 the Height is 0.335")

OPERATING SPECIFICATIONS

V_{CC} Supply Voltage 5.00 ± 0.25 VDC
 I_{CC} Supply Current 48 mA Maximum
 Logic "1" Input: V_{IH} 2.00 V min., 5.50 V max.
 I_{IH} 20 µA max. @ 2.70V
 Logic "0" Input: V_{IL} 0.80 V max.
 I_{IL} -0.6 mA mA
 V_{OH} Logic "1" Voltage Out 2.40 V min.
 V_{OL} Logic "0" Voltage Out 0.50 V max.
 P_{WI} Input Pulse Width 40% of Delay min.
 Operating Temperature Range 0° to 70°C
 Storage Temperature Range -65° to +150°C

P/N Description

DTZM1 - XXX X

Buffered 5 Tap Delays:

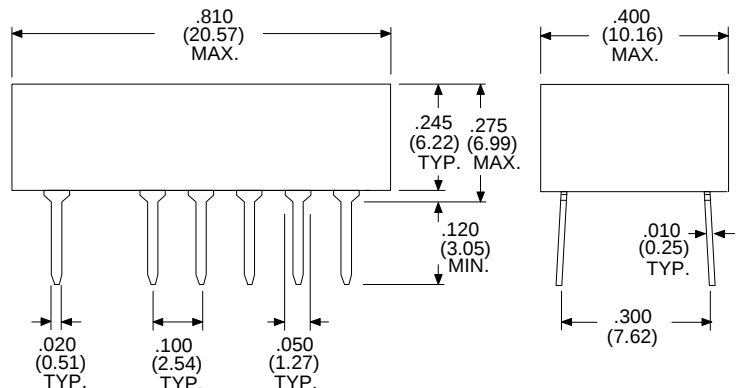
14-pin Com'l: DTZM1
 14-pin MIL: DTZM3

Total Delay in nanoseconds (ns)

Temp. Range Blank = Commercial
 M = Mil-Grade

Examples: DTZM1-25 = 25ns (5ns per tap)
 74F, 14-Pin Thru-hole

DTZM3-50M = 50ns (10ns per tap)
 74F, 14-Pin, Mil-Grade



MIL-GRADE: DTZM3 Military Grade delay lines use integrated circuits screened to MIL-STD-883B with an operating temperature range of -55 to +125°C. These devices have a package height of .335"

Auto-Insertable DIP and Surface Mount Versions:

*Refer to **FAIDM** Series, same 14-pin footprint.*

*For space saving, refer to **FAMDM** 8-pin Series*

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

DTZM13 9901