

## 2K x 8 Dual-Port Static RAM

### Features

- True dual-ported memory cells that enable simultaneous reads of the same memory location
- 2K x 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power:  $I_{CC} = 110$  mA (maximum)
- Fully asynchronous operation
- Automatic power-down
- Master CY7C132/CY7C136/CY7C136A<sup>[1]</sup> easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- BUSY output flag on CY7C132/CY7C136/CY7C136A;  
BUSY input on CY7C142/CY7C146
- INT flag for port to port communication (52-Pin PLCC/PQFP versions)
- CY7C136, CY7C136A, and CY7C146 available in 52-pin PLCC and 52-pin PQFP packages
- Pb-free packages available

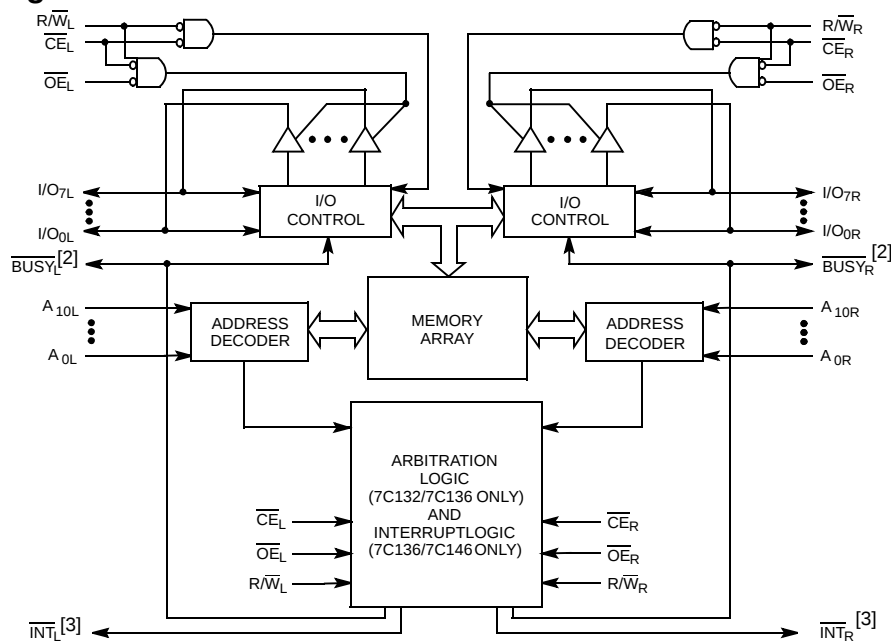
### Functional Description

The CY7C132, CY7C136, CY7C136A, CY7C142, and CY7C146 are high speed CMOS 2K x 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CY7C132, CY7C136, and CY7C136A can be used as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM, in conjunction with the CY7C142/CY7C146 SLAVE dual-port device. They are used in systems that require 16-bit or greater word widths. This is the solution to applications that require shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ( $\overline{CE}$ ), write enable ( $\overline{R/W}$ ), and output enable ( $\overline{OE}$ ). BUSY flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the 52-pin PLCC version. BUSY signals that the port is trying to access the same location currently being accessed by the other port. On the PLCC version, INT is an interrupt flag indicating that data is placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power-down feature is controlled independently on each port by the chip enable ( $\overline{CE}$ ) pins.

### Logic Block Diagram



#### Notes

1. CY7C136 and CY7C136A are functionally identical.
2. CY7C132/CY7C136/CY7C136A (Master): BUSY is open drain output and requires pull up resistor. CY7C142/CY7C146 (Slave): BUSY is input.
3. Open drain outputs; pull up resistor required.

## Pinouts

Figure 1. 52-Pin PLCC (Top View)

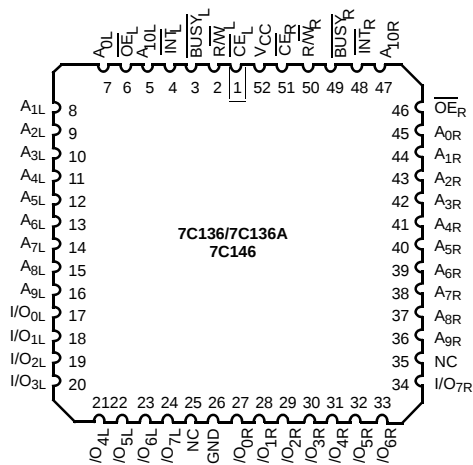
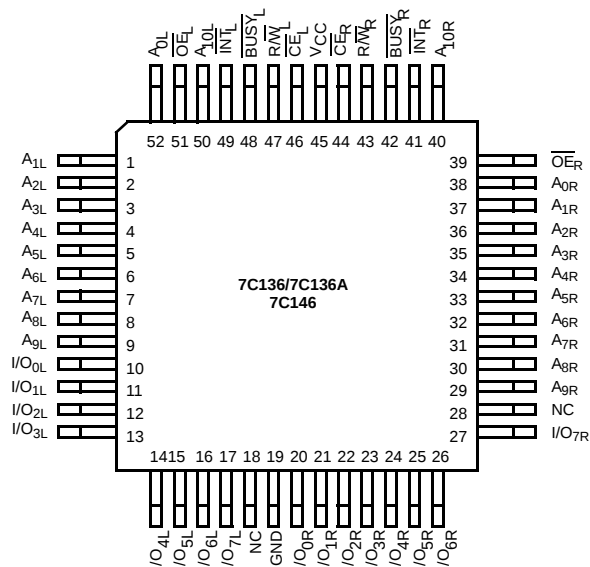


Figure 2. 52-Pin PQFP (Top View)



## Selection Guide

| Specification             |           | 7C136-15 <sup>[4]</sup><br>7C146-15 | 7C132-25 <sup>[4]</sup><br>7C136-25<br>7C142-25<br>7C146-25 | 7C132-30<br>7C136-30<br>7C142-30<br>7C146-30 | 7C132-35<br>7C136-35<br>7C142-35<br>7C146-35 | 7C132-45<br>7C136-45<br>7C142-45<br>7C146-45 | 7C132-55<br>7C136-55<br>7C136A-55<br>7C142-55<br>7C146-55 | Unit |
|---------------------------|-----------|-------------------------------------|-------------------------------------------------------------|----------------------------------------------|----------------------------------------------|----------------------------------------------|-----------------------------------------------------------|------|
| Maximum Access Time       |           | 15                                  | 25                                                          | 30                                           | 35                                           | 45                                           | 55                                                        | ns   |
| Maximum Operating Current | Com'I/Ind | 190                                 | 170                                                         | 170                                          | 120                                          | 120                                          | 110                                                       | mA   |
| Maximum Standby Current   | Com'I/Ind | 75                                  | 65                                                          | 65                                           | 45                                           | 45                                           | 35                                                        | mA   |

Shaded areas contain preliminary information.

### Note:

4. 15 ns and 25 ns version available in PQFP and PLCC packages only.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with  
Power Applied ..... -55 °C to +125 °C

Supply voltage to ground potential  
(Pin 48 to Pin 24) ..... -0.5 V to +7.0 V

DC voltage applied to outputs  
in High Z State ..... -0.5 V to +7.0 V

DC input voltage ..... -3.5 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V  
(per MIL-STD-883, Method 3015)

Latch up Current ..... > 200 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0 °C to +70 °C      | 5 V ± 10%       |
| Industrial | -40 °C to +85 °C    | 5 V ± 10%       |

## Electrical Characteristics

Over the Operating Range

| Parameter        | Description                                 | Test Conditions                                                                                                                                                                                          | 7C136-15 <sup>[4]</sup><br>7C146-15 |      | 7C132-30 <sup>[4]</sup><br>7C136-25,<br>30<br>7C142-30<br>7C146-25,<br>30 |      | 7C132-35,4<br>5<br>7C136-35,4<br>5<br>7C142-35,4<br>5<br>7C146-35,4<br>5 |      | 7C132-55<br>7C136-55<br>7C136A-55<br>7C142-55<br>7C146-55 |      | Unit |
|------------------|---------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|------|---------------------------------------------------------------------------|------|--------------------------------------------------------------------------|------|-----------------------------------------------------------|------|------|
|                  |                                             |                                                                                                                                                                                                          | Min                                 | Max  | Min                                                                       | Max  | Min                                                                      | Max  | Min                                                       | Max  |      |
| V <sub>OH</sub>  | Output HIGH voltage                         | V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA                                                                                                                                                         | 2.4                                 |      | 2.4                                                                       |      | 2.4                                                                      |      | 2.4                                                       |      | V    |
| V <sub>OL</sub>  | Output LOW voltage                          | I <sub>OL</sub> = 4.0 mA                                                                                                                                                                                 |                                     | 0.4  |                                                                           | 0.4  |                                                                          | 0.4  |                                                           | 0.4  | V    |
|                  |                                             | I <sub>OL</sub> = 16.0 mA <sup>[5]</sup>                                                                                                                                                                 |                                     | 0.5  |                                                                           | 0.5  |                                                                          | 0.5  |                                                           | 0.5  |      |
| V <sub>IH</sub>  | Input HIGH voltage                          |                                                                                                                                                                                                          | 2.2                                 |      | 2.2                                                                       |      | 2.2                                                                      |      | 2.2                                                       |      | V    |
| V <sub>IL</sub>  | Input LOW voltage                           |                                                                                                                                                                                                          |                                     | 0.8  |                                                                           | 0.8  |                                                                          | 0.8  |                                                           | 0.8  | V    |
| I <sub>IX</sub>  | Input load current                          | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                                                                   | -5                                  | +5   | -5                                                                        | +5   | -5                                                                       | +5   | -5                                                        | +5   | μA   |
| I <sub>OZ</sub>  | Output leakage current                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled                                                                                                                                                 | -5                                  | +5   | -5                                                                        | +5   | -5                                                                       | +5   | -5                                                        | +5   | μA   |
| I <sub>OS</sub>  | Output short circuit current <sup>[6]</sup> | V <sub>CC</sub> = Max, V <sub>OUT</sub> = GND                                                                                                                                                            |                                     | -350 |                                                                           | -350 |                                                                          | -350 |                                                           | -350 | mA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current    | $\overline{CE} = V_{IL}$ , Outputs Open,<br>f = f <sub>MAX</sub> <sup>[7]</sup>                                                                                                                          |                                     | 190  |                                                                           | 170  |                                                                          | 120  |                                                           | 110  | mA   |
| I <sub>SB1</sub> | Standby current both ports, TTL Inputs      | $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ ,<br>f = f <sub>MAX</sub> <sup>[7]</sup>                                                                                                             |                                     | 75   |                                                                           | 65   |                                                                          | 45   |                                                           | 35   | mA   |
| I <sub>SB2</sub> | Standby Current One Port, TTL Inputs        | $\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ ,<br>Active Port Outputs Open,<br>f = f <sub>MAX</sub> <sup>[7]</sup>                                                                                 |                                     | 135  |                                                                           | 115  |                                                                          | 90   |                                                           | 75   | mA   |
| I <sub>SB3</sub> | Standby Current Both Ports, CMOS Inputs     | Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0                                                      |                                     | 15   |                                                                           | 15   |                                                                          | 15   |                                                           | 15   | mA   |
| I <sub>SB4</sub> | Standby Current One Port, CMOS Inputs       | One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2$ V, V <sub>IN</sub> > V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> < 0.2 V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[7]</sup> |                                     | 125  |                                                                           | 105  |                                                                          | 85   |                                                           | 70   | mA   |

### Notes

5. BUSY and INT pins only.

6. Duration of the short circuit should not exceed 30 seconds.

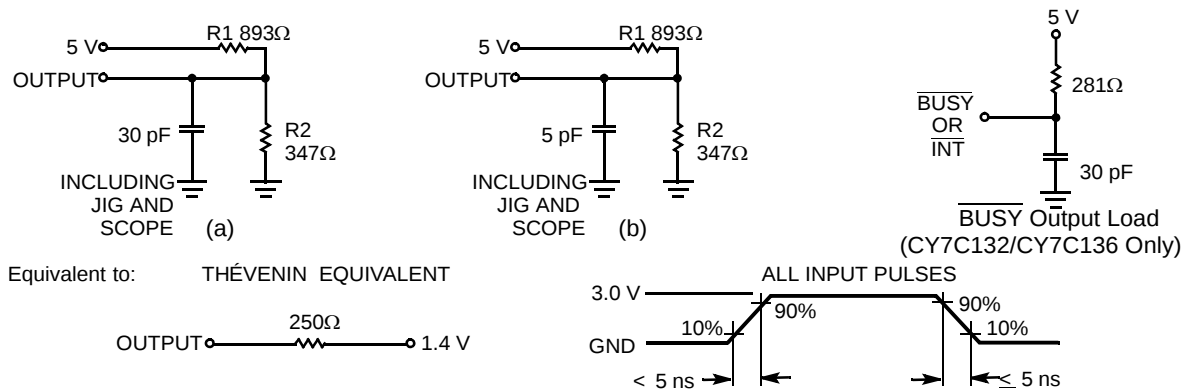
7. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>rc</sub> and using AC Test Waveforms input levels of GND to 3 V.

## Capacitance

This parameter is guaranteed but not tested.

| Parameter | Description        | Test Conditions                                                         | Max | Unit |
|-----------|--------------------|-------------------------------------------------------------------------|-----|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$ | 15  | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                         | 10  | pF   |

**Figure 3. AC Test Loads and Waveforms**



## Switching Characteristics

Over the Operating Range (Speeds -15, -25, -30) <sup>[8]</sup>

| Parameter         | Description                                                  | 7C136-15 <sup>[4]</sup><br>7C146-15 |     | 7C132-25 <sup>[4]</sup><br>7C136-25<br>7C142-25<br>7C146-25 |     | 7C132-30<br>7C136-30<br>7C142-30<br>7C146-30 |     | Unit |
|-------------------|--------------------------------------------------------------|-------------------------------------|-----|-------------------------------------------------------------|-----|----------------------------------------------|-----|------|
|                   |                                                              | Min                                 | Max | Min                                                         | Max | Min                                          | Max |      |
| Read Cycle        |                                                              |                                     |     |                                                             |     |                                              |     |      |
| t <sub>RC</sub>   | Read Cycle Time                                              | 15                                  |     | 25                                                          |     | 30                                           |     | ns   |
| t <sub>AA</sub>   | Address to Data Valid <sup>[9]</sup>                         |                                     | 15  |                                                             | 25  |                                              | 30  | ns   |
| t <sub>OHA</sub>  | Data Hold from Address Change                                | 0                                   |     | 0                                                           |     | 0                                            |     | ns   |
| t <sub>ACE</sub>  | $\overline{\text{CE}}$ LOW to Data Valid <sup>[9]</sup>      |                                     | 15  |                                                             | 25  |                                              | 30  | ns   |
| t <sub>DOE</sub>  | $\overline{\text{OE}}$ LOW to Data Valid <sup>[9]</sup>      |                                     | 10  |                                                             | 15  |                                              | 20  | ns   |
| t <sub>LZOE</sub> | $\overline{\text{OE}}$ LOW to Low Z <sup>[7, 10]</sup>       | 3                                   |     | 3                                                           |     | 3                                            |     | ns   |
| t <sub>HZOE</sub> | $\overline{\text{OE}}$ HIGH to High Z <sup>[7, 10, 11]</sup> |                                     | 10  |                                                             | 15  |                                              | 15  | ns   |
| t <sub>LZCE</sub> | $\overline{\text{CE}}$ LOW to Low Z <sup>[7, 10]</sup>       | 3                                   |     | 5                                                           |     | 5                                            |     | ns   |
| t <sub>HZCE</sub> | $\overline{\text{CE}}$ HIGH to High Z <sup>[7, 10, 11]</sup> |                                     | 10  |                                                             | 15  |                                              | 15  | ns   |
| t <sub>PU</sub>   | $\overline{\text{CE}}$ LOW to power-up <sup>[7]</sup>        | 0                                   |     | 0                                                           |     | 0                                            |     | ns   |
| t <sub>PD</sub>   | $\overline{\text{CE}}$ HIGH to power-down <sup>[7]</sup>     |                                     | 15  |                                                             | 25  |                                              | 25  | ns   |

Shaded areas contain preliminary information.

### Notes

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified  $I_{OL}/I_{OH}$ , and 30 pF load capacitance.
- AC test conditions use  $V_{OH} = 1.6\text{ V}$  and  $V_{OL} = 1.4\text{ V}$ .
- At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
- $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{HZOE}$ ,  $t_{LZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are tested with  $C_L = 5\text{ pF}$  as in (b) of [AC Test Loads and Waveforms](#). Transition is measured  $\pm 500\text{ mV}$  from steady state voltage.

## Switching Characteristics

Over the Operating Range (Speeds -15, -25, -30) <sup>[8]</sup> (continued)

| Parameter                        | Description                                                                        | 7C136-15 <sup>[4]</sup><br>7C146-15 |         | 7C132-25 <sup>[4]</sup><br>7C136-25<br>7C142-25<br>7C146-25 |         | 7C132-30<br>7C136-30<br>7C142-30<br>7C146-30 |         | Unit |
|----------------------------------|------------------------------------------------------------------------------------|-------------------------------------|---------|-------------------------------------------------------------|---------|----------------------------------------------|---------|------|
|                                  |                                                                                    | Min                                 | Max     | Min                                                         | Max     | Min                                          | Max     |      |
| Write Cycle <sup>[12]</sup>      |                                                                                    |                                     |         |                                                             |         |                                              |         |      |
| t <sub>WC</sub>                  | Write Cycle Time                                                                   | 15                                  |         | 25                                                          |         | 30                                           |         | ns   |
| t <sub>SCE</sub>                 | $\overline{\text{CE}}$ LOW to Write End                                            | 12                                  |         | 20                                                          |         | 25                                           |         | ns   |
| t <sub>AW</sub>                  | Address Setup to Write End                                                         | 12                                  |         | 20                                                          |         | 25                                           |         | ns   |
| t <sub>HA</sub>                  | Address Hold from Write End                                                        | 2                                   |         | 2                                                           |         | 2                                            |         | ns   |
| t <sub>SA</sub>                  | Address Setup to Write Start                                                       | 0                                   |         | 0                                                           |         | 0                                            |         | ns   |
| t <sub>PWE</sub>                 | R/W Pulse Width                                                                    | 12                                  |         | 15                                                          |         | 25                                           |         | ns   |
| t <sub>SD</sub>                  | Data Setup to Write End                                                            | 10                                  |         | 15                                                          |         | 15                                           |         | ns   |
| t <sub>HD</sub>                  | Data Hold from Write End                                                           | 0                                   |         | 0                                                           |         | 0                                            |         | ns   |
| t <sub>HZWE</sub>                | R/W LOW to High Z <sup>[7]</sup>                                                   |                                     | 10      |                                                             | 15      |                                              | 15      | ns   |
| t <sub>LZWE</sub>                | R/W HIGH to Low Z <sup>[7]</sup>                                                   | 0                                   |         | 0                                                           |         | 0                                            |         | ns   |
| Busy/Interrupt Timing            |                                                                                    |                                     |         |                                                             |         |                                              |         |      |
| t <sub>BLA</sub>                 | $\overline{\text{BUSY}}$ LOW from Address Match                                    |                                     | 15      |                                                             | 20      |                                              | 20      | ns   |
| t <sub>BHA</sub>                 | $\overline{\text{BUSY}}$ HIGH from Address Mismatch <sup>[13]</sup>                |                                     | 15      |                                                             | 20      |                                              | 20      | ns   |
| t <sub>BLC</sub>                 | $\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW                       |                                     | 15      |                                                             | 20      |                                              | 20      | ns   |
| t <sub>BHC</sub>                 | $\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH <sup>[13]</sup>     |                                     | 15      |                                                             | 20      |                                              | 20      | ns   |
| t <sub>PS</sub>                  | Port Set Up for Priority                                                           | 5                                   |         | 5                                                           |         | 5                                            |         | ns   |
| t <sub>WB</sub>                  | R/W LOW after $\overline{\text{BUSY}}$ LOW <sup>[14]</sup>                         | 0                                   |         | 0                                                           |         | 0                                            |         | ns   |
| t <sub>WH</sub>                  | R/W HIGH after $\overline{\text{BUSY}}$ HIGH                                       | 13                                  |         | 20                                                          |         | 30                                           |         | ns   |
| t <sub>BDD</sub>                 | $\overline{\text{BUSY}}$ HIGH to Valid Data                                        |                                     | 15      |                                                             | 25      |                                              | 30      | ns   |
| t <sub>DDD</sub>                 | Write Data Valid to Read Data Valid                                                |                                     | Note 15 |                                                             | Note 15 |                                              | Note 15 | ns   |
| t <sub>WDD</sub>                 | Write Pulse to Data Delay                                                          |                                     | Note 15 |                                                             | Note 15 |                                              | Note 15 | ns   |
| Interrupt Timing <sup>[16]</sup> |                                                                                    |                                     |         |                                                             |         |                                              |         |      |
| t <sub>WINS</sub>                | R/W to $\overline{\text{INTERRUPT}}$ Set Time                                      |                                     | 15      |                                                             | 25      |                                              | 25      | ns   |
| t <sub>EINS</sub>                | $\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Set Time                   |                                     | 15      |                                                             | 25      |                                              | 25      | ns   |
| t <sub>INS</sub>                 | Address to $\overline{\text{INTERRUPT}}$ Set Time                                  |                                     | 15      |                                                             | 25      |                                              | 25      | ns   |
| t <sub>OINR</sub>                | $\overline{\text{OE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time <sup>[13]</sup> |                                     | 15      |                                                             | 25      |                                              | 25      | ns   |
| t <sub>EINR</sub>                | $\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time <sup>[13]</sup> |                                     | 15      |                                                             | 25      |                                              | 25      | ns   |
| t <sub>INR</sub>                 | Address to $\overline{\text{INTERRUPT}}$ Reset Time <sup>[13]</sup>                |                                     | 15      |                                                             | 25      |                                              | 25      | ns   |

Shaded areas contain preliminary information.

### Notes

12. The internal write time of the memory is defined by the overlap of CE LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.

13. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

14. CY7C142/CY7C146 only.

15. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:

BUSY on Port B goes HIGH.

Port B's address toggled.

CE for Port B is toggled.

R/W for Port B is toggled during valid read.

16. 52-pin PLCC and PQFP versions only.

## Switching Characteristics

Over the Operating Range (Speeds -35, -45, -55) <sup>[8]</sup>

| Parameter                   | Description                                     | 7C132-35<br>7C136-35<br>7C142-35<br>7C146-35 |         | 7C132-45<br>7C136-45<br>7C142-45<br>7C146-45 |         | 7C132-55<br>7C136-55<br>7C136A-55<br>7C142-55<br>7C146-55 |         | Unit |
|-----------------------------|-------------------------------------------------|----------------------------------------------|---------|----------------------------------------------|---------|-----------------------------------------------------------|---------|------|
|                             |                                                 | Min                                          | Max     | Min                                          | Max     | Min                                                       | Max     |      |
| Read Cycle                  |                                                 |                                              |         |                                              |         |                                                           |         |      |
| t <sub>RC</sub>             | Read Cycle Time                                 | 35                                           |         | 45                                           |         | 55                                                        |         | ns   |
| t <sub>AA</sub>             | Address to Data Valid <sup>[9]</sup>            |                                              | 35      |                                              | 45      |                                                           | 55      | ns   |
| t <sub>OHA</sub>            | Data Hold from Address Change                   | 0                                            |         | 0                                            |         | 0                                                         |         | ns   |
| t <sub>ACE</sub>            | CE LOW to Data Valid <sup>[9]</sup>             |                                              | 35      |                                              | 45      |                                                           | 55      | ns   |
| t <sub>DOE</sub>            | OE LOW to Data Valid <sup>[9]</sup>             |                                              | 20      |                                              | 25      |                                                           | 25      | ns   |
| t <sub>LZOE</sub>           | OE LOW to Low Z <sup>[7, 10]</sup>              | 3                                            |         | 3                                            |         | 3                                                         |         | ns   |
| t <sub>HZOE</sub>           | OE HIGH to High Z <sup>[7, 10, 11]</sup>        |                                              | 20      |                                              | 20      |                                                           | 25      | ns   |
| t <sub>LZCE</sub>           | CE LOW to Low Z <sup>[7, 10]</sup>              | 5                                            |         | 5                                            |         | 5                                                         |         | ns   |
| t <sub>HZCE</sub>           | CE HIGH to High Z <sup>[7, 10, 11]</sup>        |                                              | 20      |                                              | 20      |                                                           | 25      | ns   |
| t <sub>PU</sub>             | CE LOW to power-up <sup>[7]</sup>               | 0                                            |         | 0                                            |         | 0                                                         |         | ns   |
| t <sub>PD</sub>             | CE HIGH to power-down <sup>[7]</sup>            |                                              | 35      |                                              | 35      |                                                           | 35      | ns   |
| Write Cycle <sup>[12]</sup> |                                                 |                                              |         |                                              |         |                                                           |         |      |
| t <sub>WC</sub>             | Write Cycle Time                                | 35                                           |         | 45                                           |         | 55                                                        |         | ns   |
| t <sub>SCE</sub>            | CE LOW to Write End                             | 30                                           |         | 35                                           |         | 40                                                        |         | ns   |
| t <sub>AW</sub>             | Address Setup to Write End                      | 30                                           |         | 35                                           |         | 40                                                        |         | ns   |
| t <sub>HA</sub>             | Address Hold from Write End                     | 2                                            |         | 2                                            |         | 2                                                         |         | ns   |
| t <sub>SA</sub>             | Address Setup to Write Start                    | 0                                            |         | 0                                            |         | 0                                                         |         | ns   |
| t <sub>PWE</sub>            | R/W Pulse Width                                 | 25                                           |         | 30                                           |         | 30                                                        |         | ns   |
| t <sub>SD</sub>             | Data Setup to Write End                         | 15                                           |         | 20                                           |         | 20                                                        |         | ns   |
| t <sub>HD</sub>             | Data Hold from Write End                        | 0                                            |         | 0                                            |         | 0                                                         |         | ns   |
| t <sub>HZWE</sub>           | R/W LOW to High Z <sup>[7]</sup>                |                                              | 20      |                                              | 20      |                                                           | 25      | ns   |
| t <sub>LZWE</sub>           | R/W HIGH to Low Z <sup>[7]</sup>                | 0                                            |         | 0                                            |         | 0                                                         |         | ns   |
| Busy/Interrupt Timing       |                                                 |                                              |         |                                              |         |                                                           |         |      |
| t <sub>BLA</sub>            | BUSY LOW from Address Match                     |                                              | 20      |                                              | 25      |                                                           | 30      | ns   |
| t <sub>BHA</sub>            | BUSY HIGH from Address Mismatch <sup>[13]</sup> |                                              | 20      |                                              | 25      |                                                           | 30      | ns   |
| t <sub>BLC</sub>            | BUSY LOW from CE LOW                            |                                              | 20      |                                              | 25      |                                                           | 30      | ns   |
| t <sub>BHC</sub>            | BUSY HIGH from CE HIGH <sup>[13]</sup>          |                                              | 20      |                                              | 25      |                                                           | 30      | ns   |
| t <sub>PS</sub>             | Port Set Up for Priority                        | 5                                            |         | 5                                            |         | 5                                                         |         | ns   |
| t <sub>WB</sub>             | R/W LOW after BUSY LOW <sup>[14]</sup>          | 0                                            |         | 0                                            |         | 0                                                         |         | ns   |
| t <sub>WH</sub>             | R/W HIGH after BUSY HIGH                        | 30                                           |         | 35                                           |         | 35                                                        |         | ns   |
| t <sub>BDD</sub>            | BUSY HIGH to Valid Data                         |                                              | 35      |                                              | 45      |                                                           | 45      | ns   |
| t <sub>DDD</sub>            | Write Data Valid to Read Data Valid             |                                              | Note 15 |                                              | Note 15 |                                                           | Note 15 | ns   |
| t <sub>WDD</sub>            | Write Pulse to Data Delay                       |                                              | Note 15 |                                              | Note 15 |                                                           | Note 15 | ns   |

## Switching Characteristics

Over the Operating Range (Speeds -35, -45, -55) <sup>[8]</sup> (continued)

| Parameter         | Description                                              | 7C132-35<br>7C136-35<br>7C142-35<br>7C146-35 |     | 7C132-45<br>7C136-45<br>7C142-45<br>7C146-45 |     | 7C132-55<br>7C136-55<br>7C136A-55<br>7C142-55<br>7C146-55 |     | Unit |
|-------------------|----------------------------------------------------------|----------------------------------------------|-----|----------------------------------------------|-----|-----------------------------------------------------------|-----|------|
|                   |                                                          | Min                                          | Max | Min                                          | Max | Min                                                       | Max |      |
|                   |                                                          | Interrupt Timing <sup>[16]</sup>             |     |                                              |     |                                                           |     |      |
| t <sub>WINS</sub> | R/W to <u>INTERRUPT</u> Set Time                         |                                              | 25  |                                              | 35  |                                                           | 45  | ns   |
| t <sub>EINS</sub> | <u>CE</u> to <u>INTERRUPT</u> Set Time                   |                                              | 25  |                                              | 35  |                                                           | 45  | ns   |
| t <sub>INS</sub>  | Address to <u>INTERRUPT</u> Set Time                     |                                              | 25  |                                              | 35  |                                                           | 45  | ns   |
| t <sub>OINR</sub> | <u>OE</u> to <u>INTERRUPT</u> Reset Time <sup>[13]</sup> |                                              | 25  |                                              | 35  |                                                           | 45  | ns   |
| t <sub>EINR</sub> | <u>CE</u> to <u>INTERRUPT</u> Reset Time <sup>[13]</sup> |                                              | 25  |                                              | 35  |                                                           | 45  | ns   |
| t <sub>INR</sub>  | Address to <u>INTERRUPT</u> Reset Time <sup>[13]</sup>   |                                              | 25  |                                              | 35  |                                                           | 45  | ns   |

## Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port-Address Access) <sup>[17, 18]</sup>

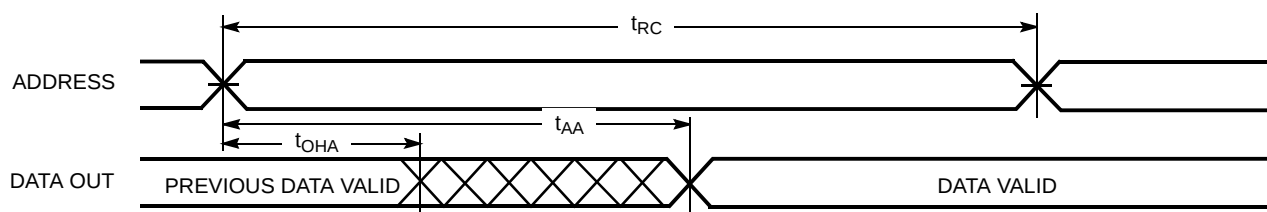
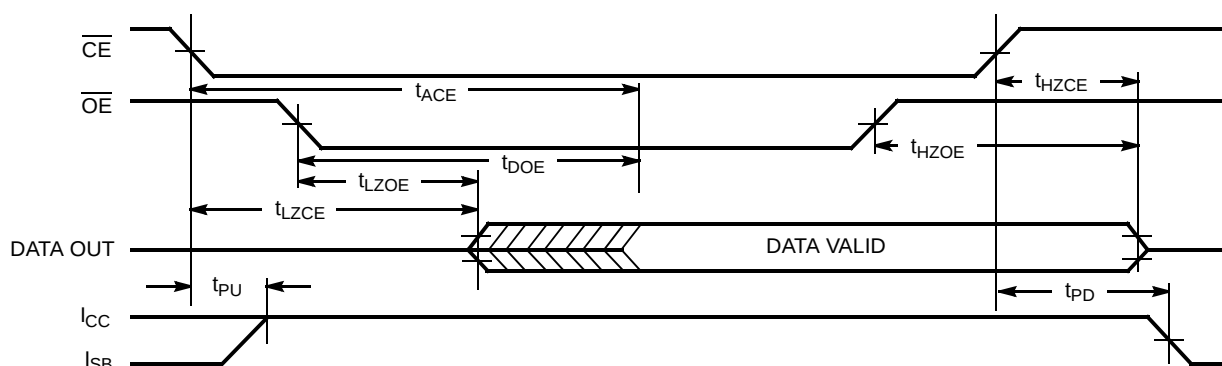


Figure 5. Read Cycle No. 2 (Either Port- $\overline{CE}/\overline{OE}$ ) <sup>[17, 19]</sup>



### Notes

17. R/W is HIGH for read cycle.
18. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
19. Address valid prior to or coincident with CE transition LOW.

## Switching Waveforms (continued)

Figure 6. Read Cycle No. 3 (Read with  $\overline{\text{BUSY}}$  Master: CY7C132 and CY7C136/CY7C136A)

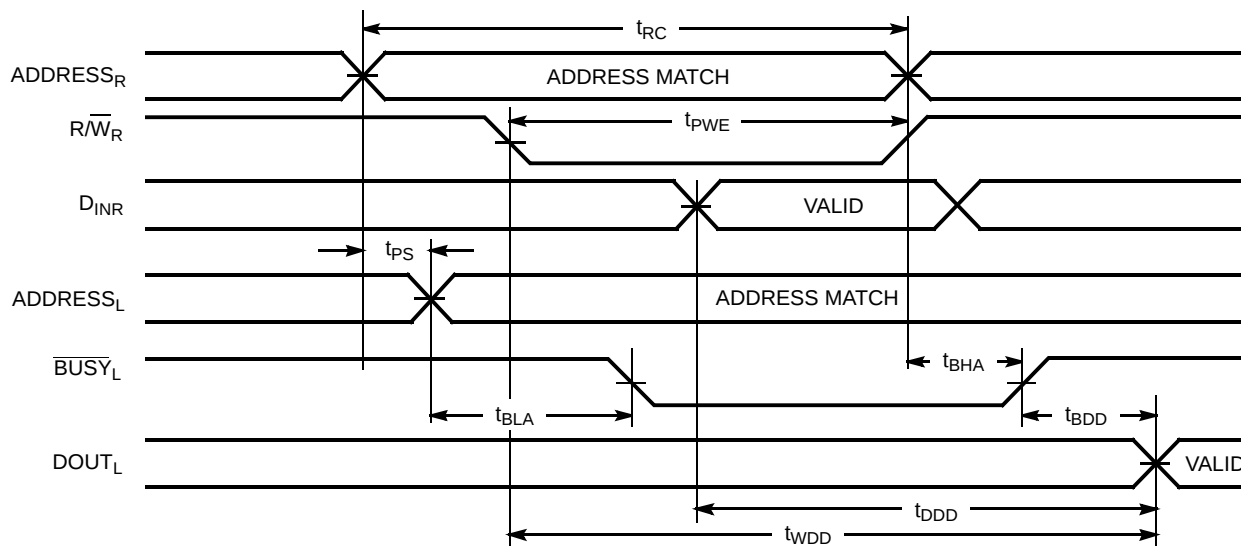
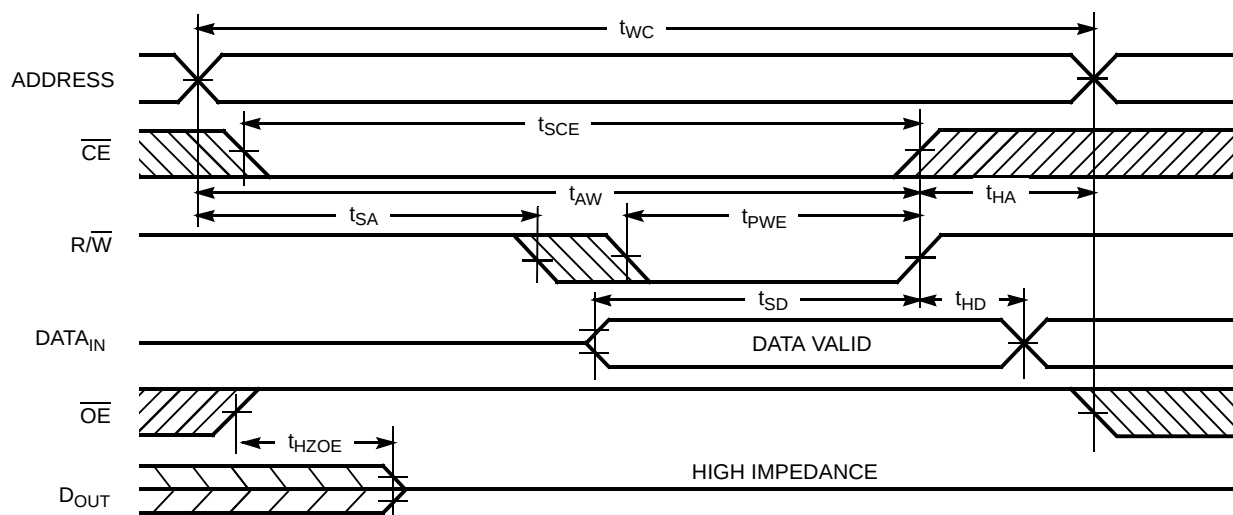


Figure 7. Write Cycle No.1 ( $\overline{\text{OE}}$  Three-States Data I/Os—Either Port) [12, 20]

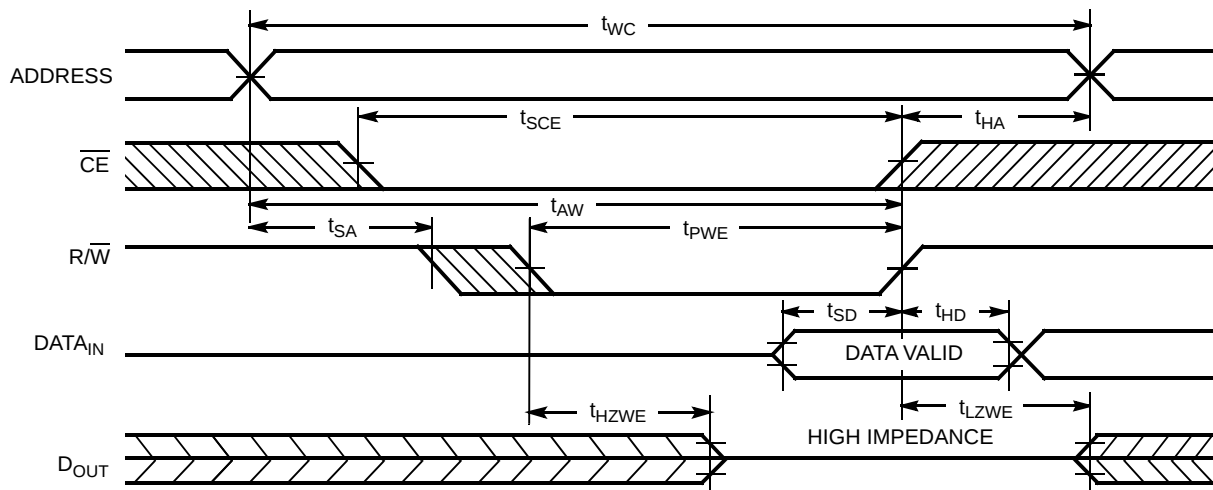


### Note

20. If  $\overline{\text{OE}}$  is LOW during a  $\text{R}/\overline{\text{W}}$  controlled write cycle, the write pulse width must be the larger of  $t_{\text{PWE}}$  or  $t_{\text{HZOE}} + t_{\text{SD}}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{\text{SD}}$ .

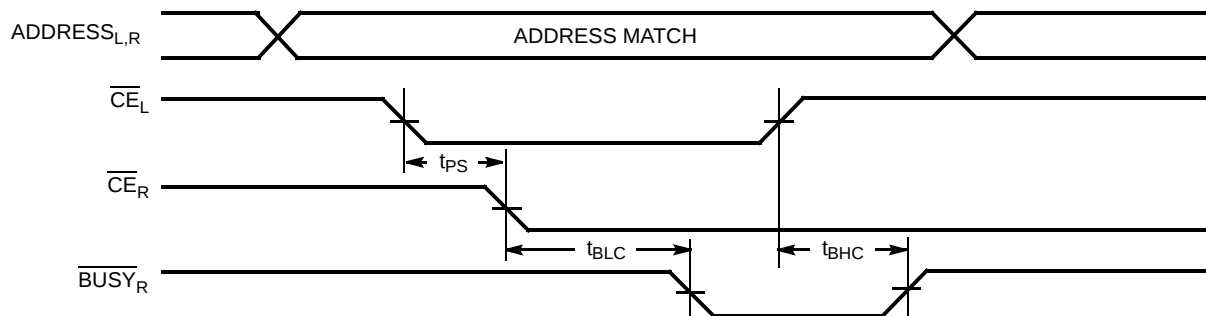
## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port)<sup>[12, 21]</sup>**

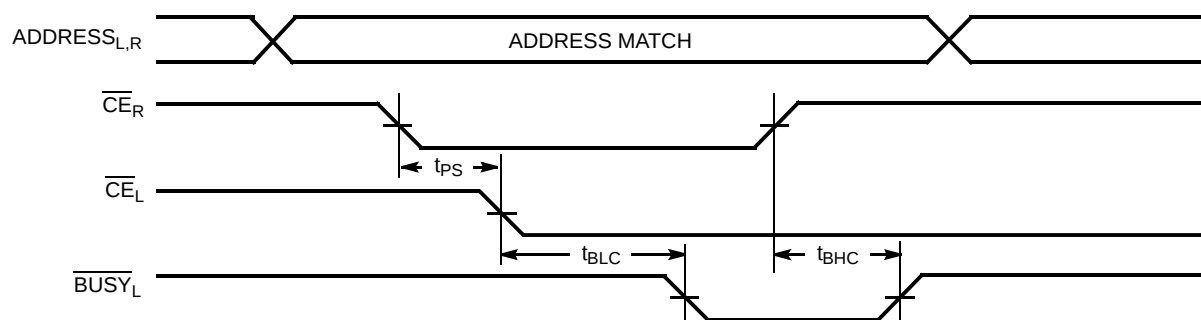


**Figure 9. Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)**

**$\overline{CE}_L$  Valid First:**



**$\overline{CE}_R$  Valid First:**



### Note

21. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high impedance state.

## Switching Waveforms (continued)

Figure 10. Busy Timing Diagram No. 2 (Address Arbitration)

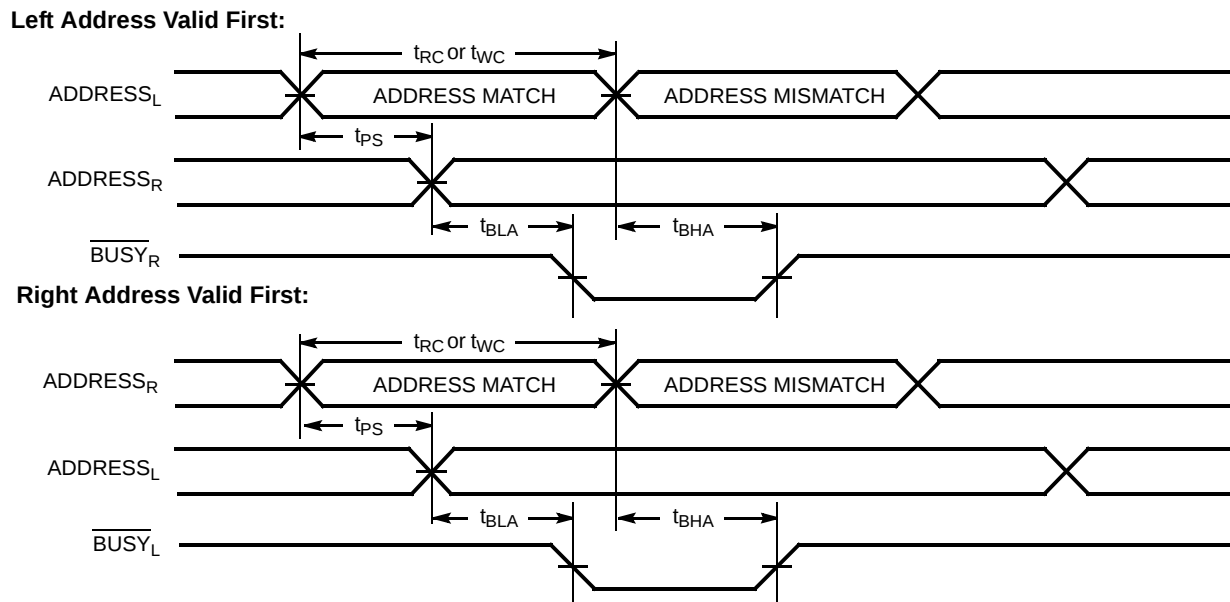
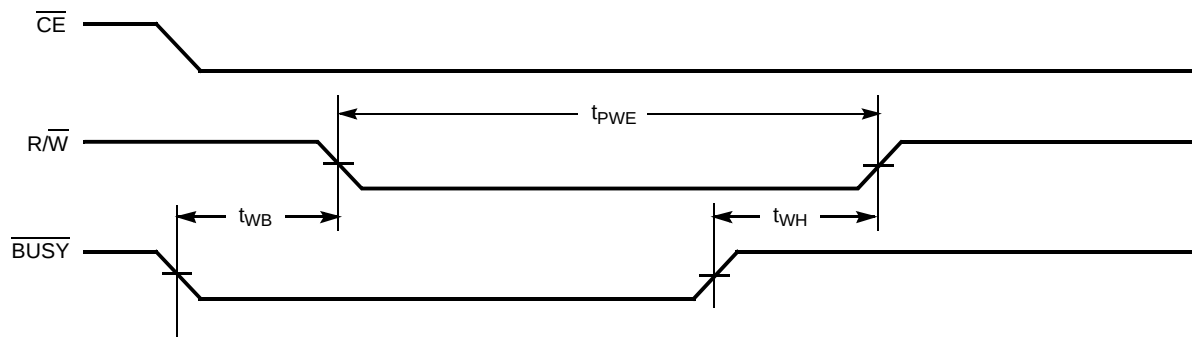


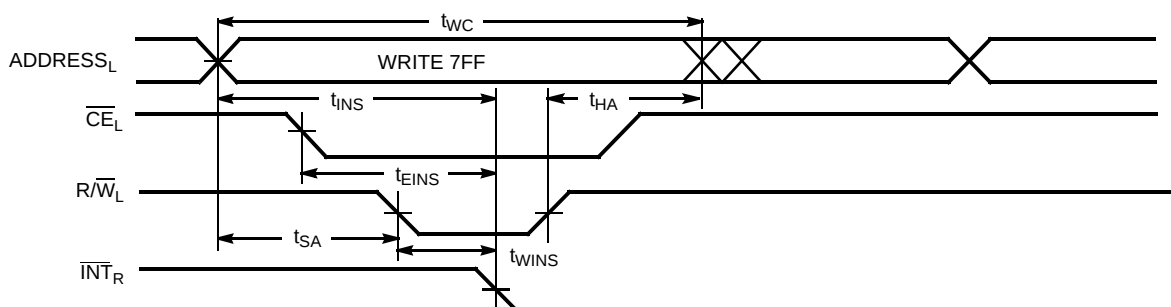
Figure 11. Busy Timing Diagram No. 3 (Write with  $\overline{\text{BUSY}}$ , Slave: CY7C142/CY7C146)



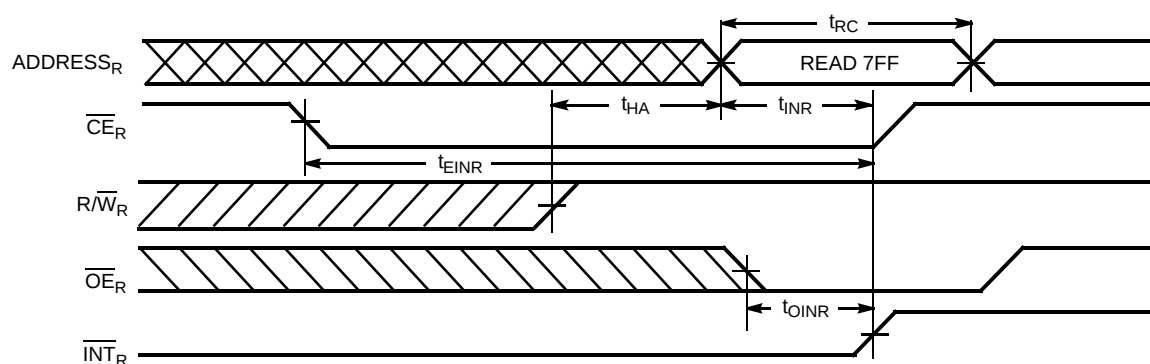
## Switching Waveforms (continued)

### Interrupt Timing Diagrams <sup>[16]</sup>

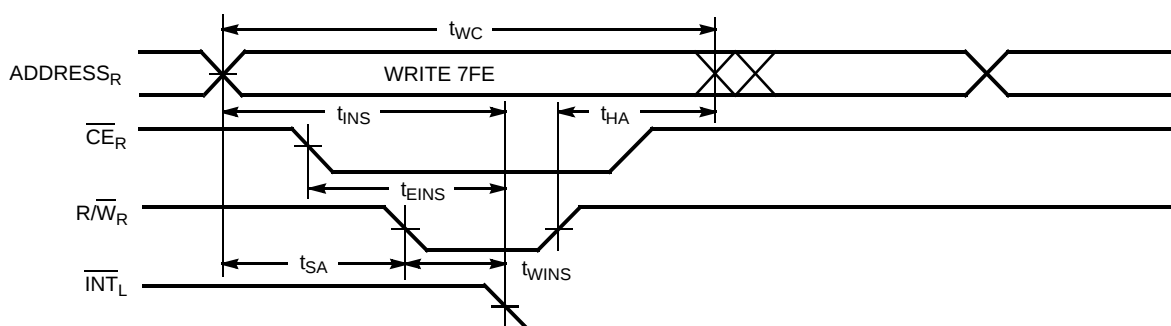
**Figure 12. Left Side Sets  $\overline{\text{INT}}_R$**



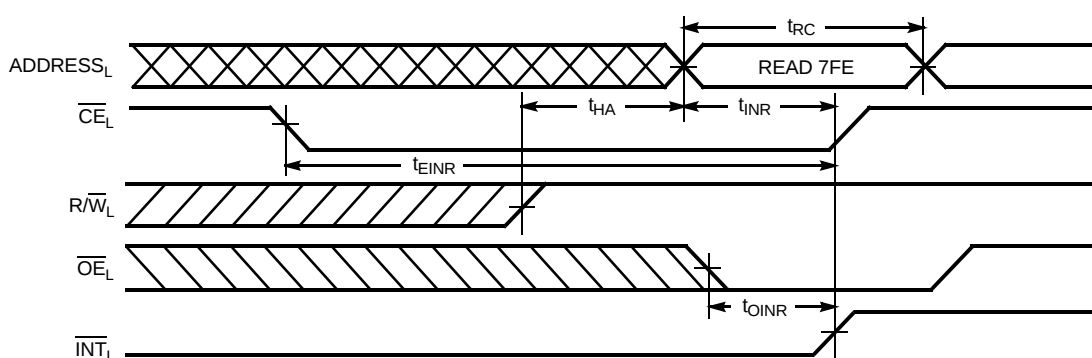
**Figure 13. Right Side Clears  $\overline{\text{INT}}_R$**



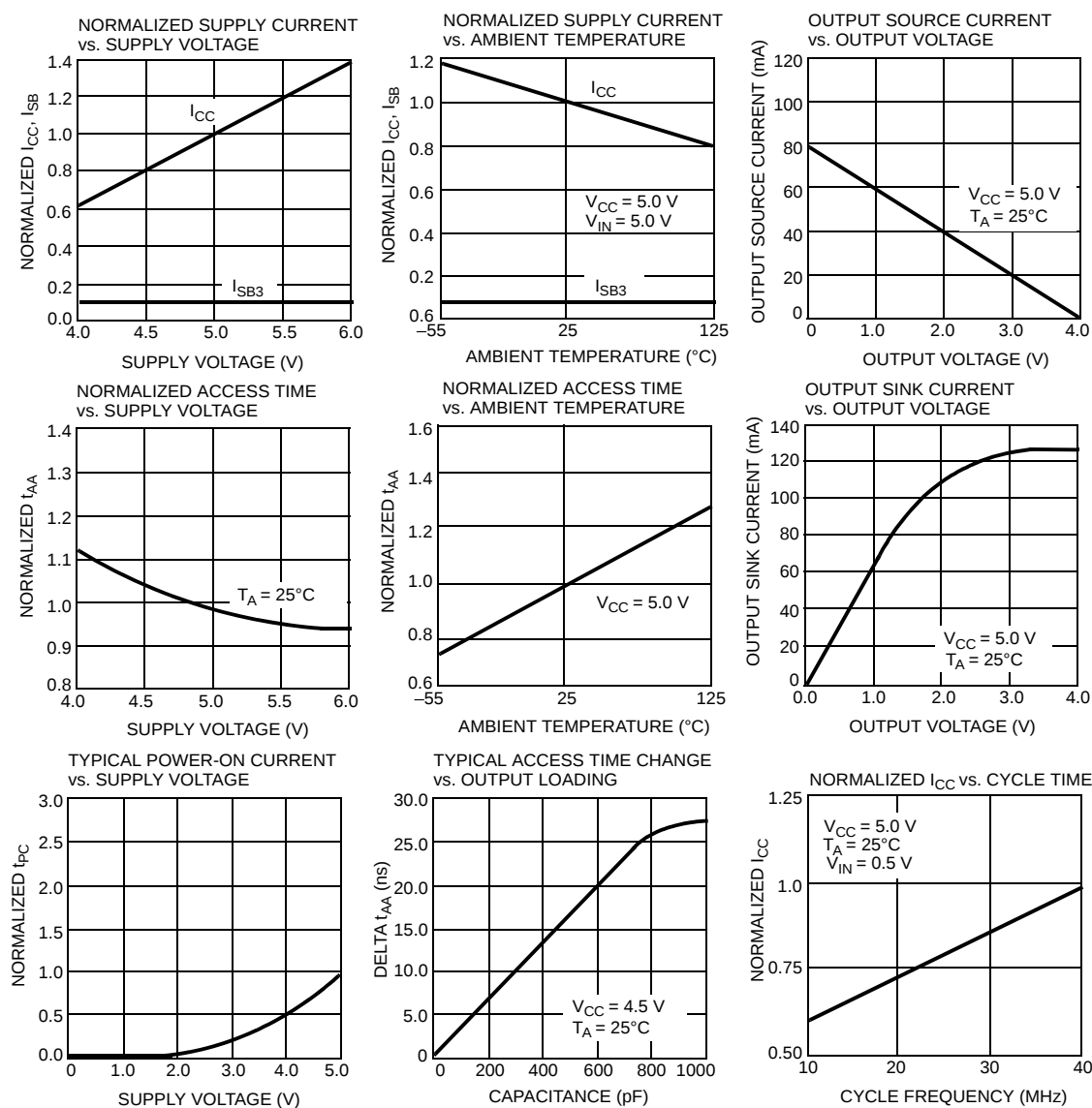
**Figure 14. Right Side Sets  $\overline{\text{INT}}_L$**



**Figure 15. Right Side Clears  $\overline{\text{INT}}_L$**



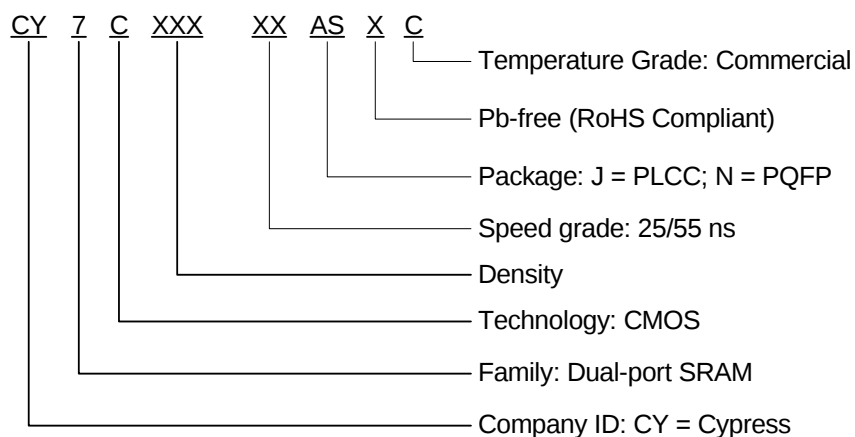
**Figure 16. Typical DC and AC Characteristics**



## Ordering Information

| Speed (ns) | Ordering Code  | Package Diagram | Package Type                                 | Operating Range |
|------------|----------------|-----------------|----------------------------------------------|-----------------|
| 25         | CY7C136-25JXC  | 51-85004        | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | Commercial      |
|            | CY7C136-25NC   | 51-85042        | 52-Pin Plastic Quad Flatpack                 |                 |
|            | CY7C136-25NXC  |                 | 52-Pin Plastic Quad Flatpack (Pb-Free)       |                 |
|            | CY7C136-25JXI  | 51-85004        | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | Industrial      |
| 55         | CY7C136-55JXC  | 51-85004        | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | Commercial      |
|            |                |                 |                                              |                 |
|            | CY7C136-55NXC  | 51-85042        | 52-Pin Plastic Quad Flatpack (Pb-Free)       |                 |
|            |                |                 |                                              |                 |
|            | CY7C136A-55JXI | 51-85004        | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | Industrial      |
|            | CY7C136A-55NXI | 51-85042        | 52-Pin Plastic Quad Flatpack (Pb-Free)       |                 |
| 55         | CY7C146-55JXC  | 51-85004        | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | Commercial      |

## Ordering Code Definitions





## Acronyms

| Acronym | Description                             |
|---------|-----------------------------------------|
| CMOS    | complementary metal oxide semiconductor |
| I/O     | input/output                            |
| PLCC    | plastic leaded chip carrier             |
| SRAM    | static random access memory             |
| TQFP    | thin quad plastic flatpack              |
| TTL     | transistion transistor logic            |

## Document Conventions

### Units of Measure

Table 1.

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | mega hertz      |
| μA     | microamperes    |
| mA     | milliamperes    |
| mV     | millivolts      |
| ns     | nanoseconds     |
| Ω      | ohms            |
| pF     | picofarad       |
| V      | volts           |
| W      | watts           |

## Document History Page

| Document Title: CY7C132, CY7C136, CY7C136A, CY7C142, CY7C146 2K x 8 Dual-Port Static RAM<br>Document Number: 38-06031 |         |                 |                 |                                                                                                                                                                                                 |
|-----------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                              | ECN     | Submission Date | Orig. of Change | Description of Change                                                                                                                                                                           |
| **                                                                                                                    | 110171  | 10/21/01        | SZV             | Change from Spec number: 38-06031                                                                                                                                                               |
| *A                                                                                                                    | 128959  | 09/03/03        | JFU             | Added CY7C136-55NI to Order Information                                                                                                                                                         |
| *B                                                                                                                    | 236748  | See ECN         | YDT             | Removed cross information from features section                                                                                                                                                 |
| *C                                                                                                                    | 393184  | See ECN         | YIM             | Added Pb-Free Logo<br>Added Pb-Free parts to ordering information:<br>CY7C136-25JXC, CY7C136-25NXC, CY7C136-55JXC, CY7C136-55NXC,<br>CY7C136-55JXI, CY7C136-55NXI, CY7C146-25JXC, CY7C146-55JXC |
| *D                                                                                                                    | 2623658 | 12/17/08        | VKN/PYRS        | Added CY7C136-25JXI part<br>Removed CY7C132/142 from the Ordering information table<br>Removed 48-Pin DIP and 52-Pin Square LCC package from the data sheet                                     |
| *E                                                                                                                    | 2678221 | 03/24/2009      | VKN/AESA        | Added CY7C136A-55JXI, and CY7C136A-55NXI parts.                                                                                                                                                 |
| *F                                                                                                                    | 2896210 | 03/22/2010      | RAME            | Updated Ordering Information<br>Updated Package Diagrams                                                                                                                                        |
| *G                                                                                                                    | 3094400 | 11/24/10        | ADMU            | Removed partnumber CY7C136-55JI from the ordering information table.<br>Added ordering code definitions.                                                                                        |
| *H                                                                                                                    | 3403652 | 10/14/2011      | ADMU            | Removed pruned part CY7C136-55JC, CY7C136-55NC from<br><a href="#">Ordering Information</a><br>Updated <a href="#">Package Diagrams</a> .<br>Updated template.                                  |

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