TEXAS INSTRUMENTS

DAC5674 EVM

User's Guide

September 2003 *Wireless Infrastructure Products*

SWRU007

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within an input voltage range of 0 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 40°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Overview

This user's guide document gives a general overview of the DAC5674 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

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1.1 Purpose

The DAC5674 EVM provides a platform for evaluating the DAC5674 digital-to-analog converter (DAC) under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Digital inputs to the DAC can be provided with CMOS level signals up to 200 MSPS through a 40-pin header. This enables the user to provide high-speed digital data to the DAC5674.

The analog output from the DAC is available via SMA connectors. Because of its flexible design, the analog output of the DAC5674 can be configured to drive a 50-Ω terminated cable using a 4:1 or 1:1 impedance ratio transformer, or single-ended referred to GND.

The EVM allows for different clock configurations. The user can input a differential ECL/PECL or TTL/CMOS level signal, to be used to generate a single-ended or differential clock source. See the clock section for proper configuration and operation.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog, digital, PLL, and I/O supply.

In addition to the internal bandgap reference provided by the DAC5674 device, options on the EVM allow external reference to be provided to the DAC.

1.3 Power Requirements

The demonstration board has four power inputs. The first, +3.3VA, is required to be +3.3 Vdc at banana jack J9 with the return going to J11. This is the analog supply for the DAC5674. The second, +1.8 VD, is required to be +1.8 Vdc at banana jack J14 with the return to J16. This is the digital +1.8-V supply for the DAC5674. The third, +3.3VCLK, is required to be +3.3 Vdc at banana jack J10 with the return at J13. This is the digital supply for the internal PLL circuitry. The fourth, +1.8/3.3VD_IO, is required to be either +1.8 or +3.3 Vdc at banana jack J12 with the return at J15. This is the supply for the digital I/Os. The EVM can be powered using only two supplies, but powering from four separate supplies provides higher performance.

Note: Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 DAC5674 EVM Operational Procedure

The DAC5674 EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The demonstration board comes with the following factory-set configuration:

- Differential clock mode using transformer T2 and a clock input at J4
- Transformer coupled output using transformer T1
- The converter is set to operate with internal reference. Jumper W2 is installed between pins 1 and 2.
- Full-scale output current set to 20 mA through R_{BIAS} resistor R1
- The DAC5674 output is enabled (sleep mode disabled). Jumper W3 is installed between pins 1 and 2.
- Reset operation controlled through S1. Jumper W5 is installed between pins 2 and 3.
- Internal PLL is disabled. Jumper W4 is installed between pins 1 and 2.

Chapter 2

PCB Layout and Parts List

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a 4-layer, 3.3-inch × 5.75-inch, 0.062-inch thick PCB using FR-4 material. Figure 2−1 through Figure 2−4 show the PCB layout for the EVM.

Figure 2−1. Top Layer 1

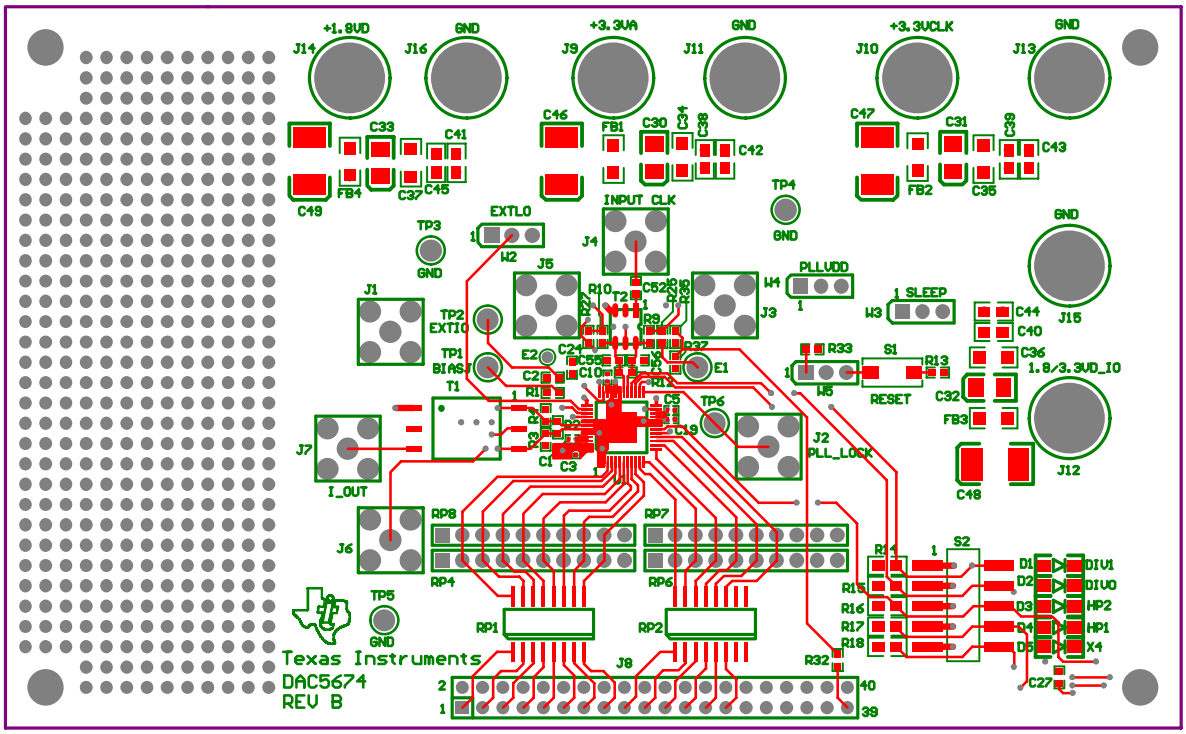


Figure 2−2. Layer 2, Ground Plane

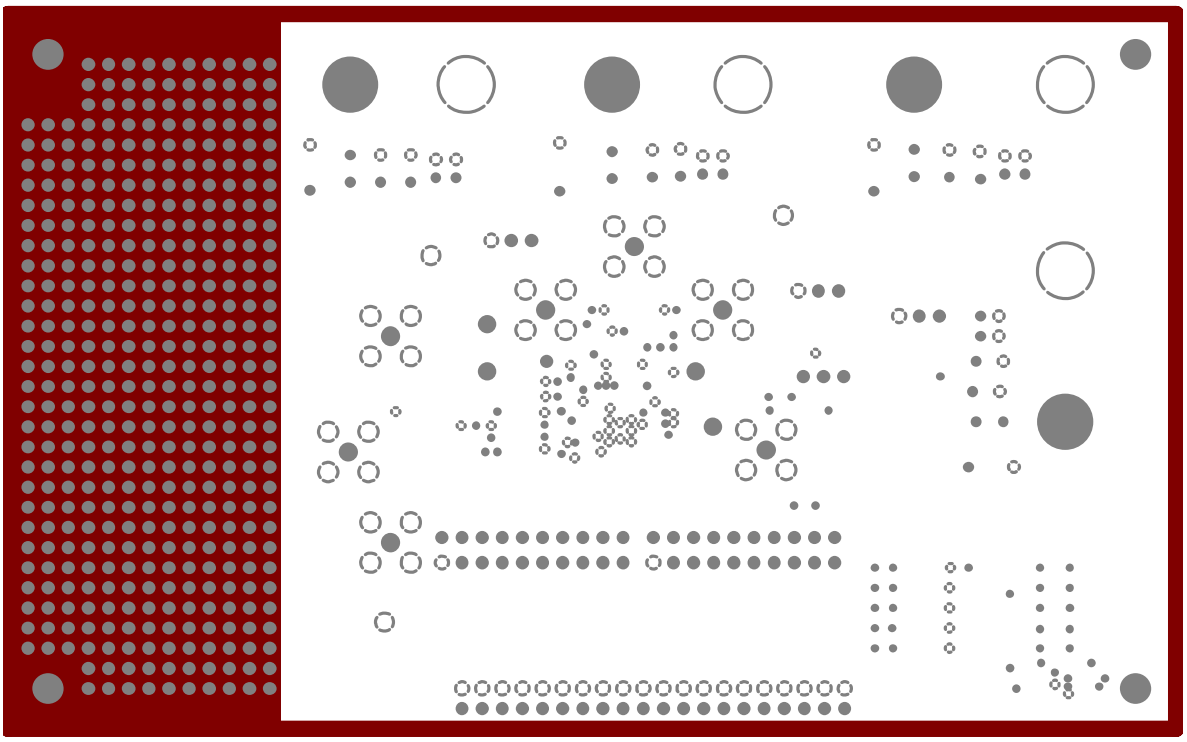


Figure 2−3. Layer 3, Power Plane

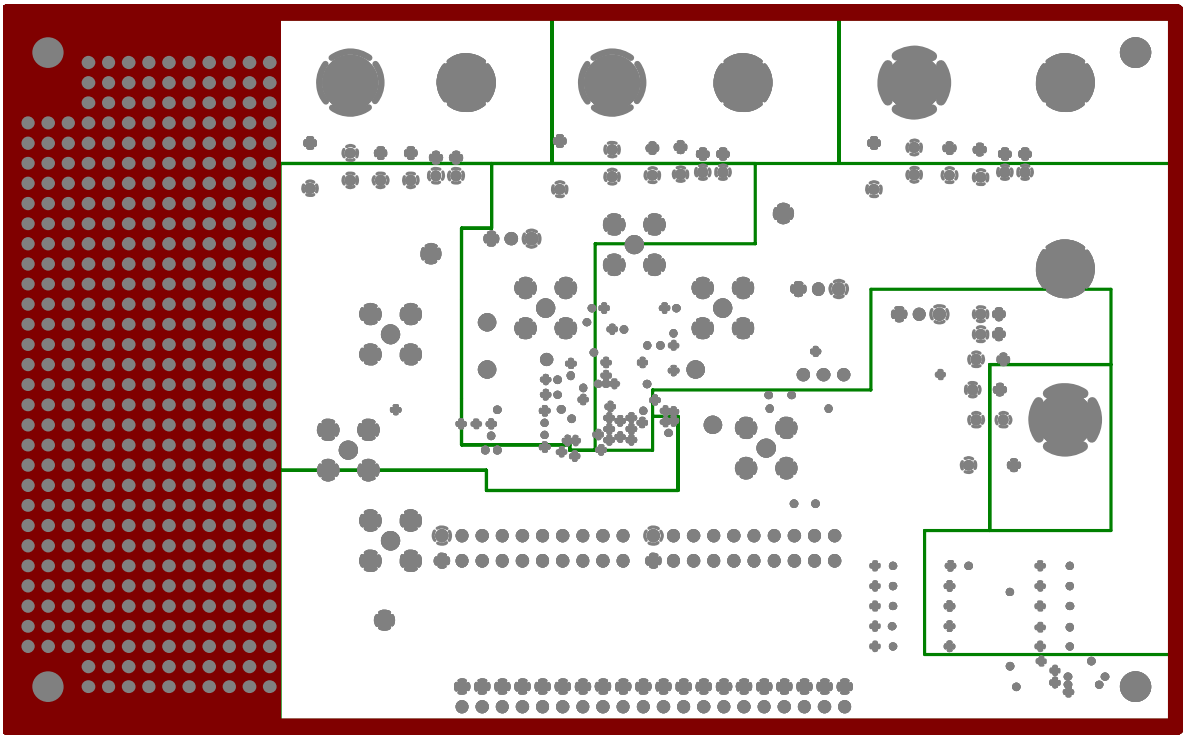
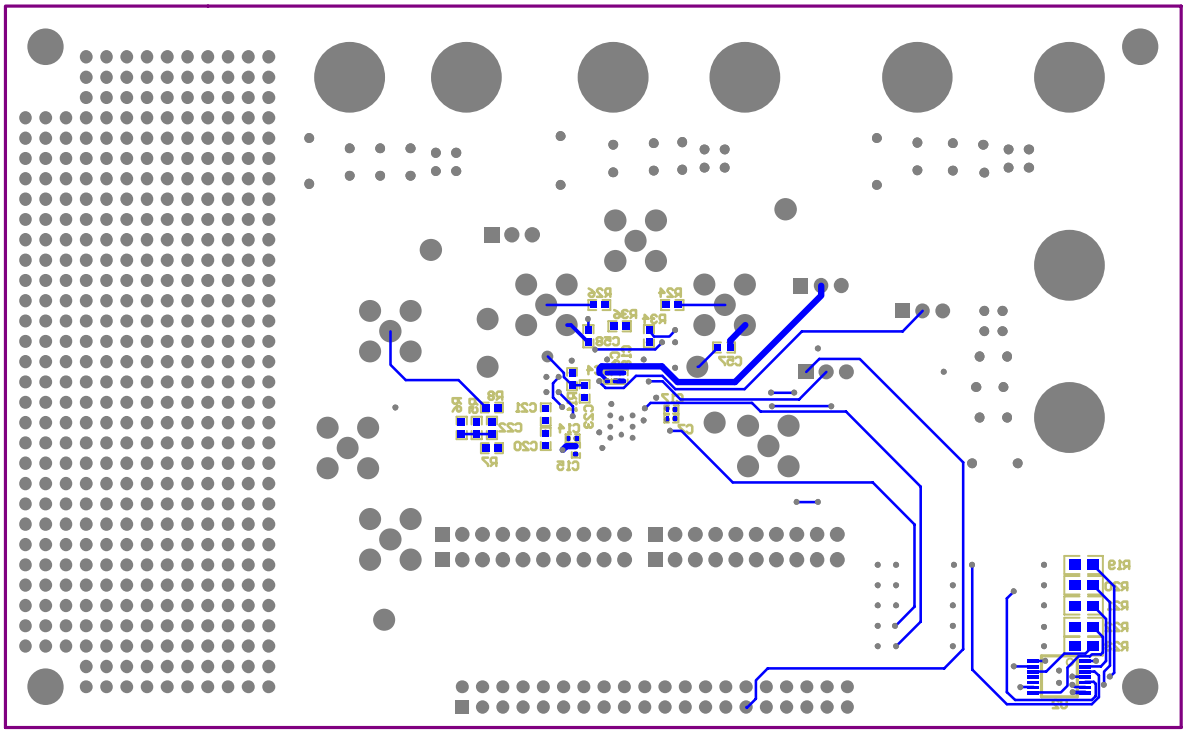


Figure 2−4. Bottom Layer



2.2 Parts List

Table 2−1 lists the parts used in constructing the EVM.

Table 2−1. DAC5674 EVM Parts List

Description	Qty.	Part Number	Mfg.	Ref. Des.	
				Installed	Not Installed
22-pF, 50-V, 5% capacitor	0	06035A220JAT2A	AVX		C20, C21
100-pF, 50-V, 5% capacitor	1	ECU-V1H101JCG	Panasonic	C23	
0.01-µF, 16-V, 10% capacitor	2	06035A103KAT2A	AVX	C24, C52	C25, C55, C56
0.01-µF, 100-V, 5% capacitor	4	08055C103KAT2A	AVX	C42−C45	
0.1-µF, 16-V, 10% capacitor	17	08055C104JAT2A	AVX	C1 −C7, C10, C14, C15, C17−C19, C22, C27, C57, C58	
0.1-µF, 100-V, 10% capacitor	4	ECJ-2VB1C104K	Panasonic	C38−C41	
1-µF, 16-V, 10% capacitor	4	ECJ-3YB1C105K	Panasonic	C34−C37	
10-µF, 10-V, 10% capacitor	4	GRM42X5R106K10	Murata	C30−C33	
47-µF, 10-V, 10%, tantalum capacitor	4	10TPA47M	Sanyo	C46−C49	
DAC5674	1	DAC5674IDW	TI	U1	
Ferrite bead	4	D01608C-472	Coil Craft	FB1−FB4	
3POS header	4	TSW-150-07-L-S	Samtec	W2−W5	
40-pin header	1	TSW-120-07-L-D	Samtec	J8	
Red banana jacks	4	ST-351A	Allied	J9, J10, J12, J14	
Black banana jacks	4	ST-351B	Allied	J11, J13, J15, J16	
Green LED	5	LN1351C-(TR)	Panasonic	D1−D5	
0-Ω, 1/16-W, 1% resistor	1	ERJ-3EKF0R00V	Panasonic	R6	R5, R7−R10, R34, R36
10-Ω, 1/16-W, 1% resistor	1	ERJ-3EKF10R0	Panasonic	R32	
49.9-Ω, 1/16-W, 1% resistor	6	ERJ-3EKF49R9V	Panasonic	R3, R4, R24−R27	
100-Ω , 1/8-W, 1% resistor	1	ERA-3YEB100	Panasonic	R2	
200-Ω, 1/10-W, 1% resistor	5	ERJ-6ENF2000	Panasonic	R19−R23	
200-Ω, 1/16-W, 0.1% resistor	2	ERA-3YEB200	Panasonic	R11, R12	
1-kΩ, 1/8-W, 1% resistor	0	ERJ-3EKF1001	Panasonic		R35, R37
1-kΩ, 1/8-W, 1% resistor	5	ERJ-6ENF1001	Panasonic	R14−R18	
2-kΩ, 1/16-W, 1% resistor	1	ERJ-6ENF2001	Panasonic	R1	
10K-kΩ, 1/8-W, 1% resistor	2	ERJ-3EKF1002	Panasonic	R13, R33	
22-Ω resistor pack	2	4816P-001-220	Bourns	RP1, RP2	
51-Ω resistor pack	2	770-101-R51	CTS	RP4, RP6	RP7, RP8

Table 2−1. DAC5674 EVM Parts List (Continued)

Description	Qty.	Part Number	Mfg.	Ref. Des.	
				Installed	Not Installed
SW-PB switch	1	EVQ-PJX04M	Panasonic	S1	
Switch	1	SD05HOSK	CK	S2	
SMA connectors	3	713-4339 (901-144-8RFX)	Allied	J2, J4, J7	J1, J3, J5, J6
SN74LVC04A	1	SN74LVC04APW	TI	U2	
Standoff, hex (1/4 × 1”)	4	219-2063	Allied		
Black test point	3	5001K	Keystone	TP3, TP4, TP5	
Red test point	3	5000K	Keystone	TP1, TP2, TP6	
Transformer	1	T1-1T-KK8	Mini-Circuits	T1	
Transformer	1	TCM4-1	Mini-Circuits	T2	

Chapter 3

Circuit Description

This chapter provides descriptions of the primary functional circuits on the DAC5674 EVM.

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3.1 Circuit Function

The following paragraphs describe the EVM circuits.

3.1.1 Input Clock

The DAC5674 EVM default operation setting is with a differential input clock sent to the DAC5674. A 500-mV p-p, 0-V offset, 50% duty-cycle external sinewave is applied to SMA connector J4 and converted to a differential clock input to the DAC5674 by transformer T2. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC5674 converter, the clock source should feature very low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance.

3.1.1.1 Differential ECL/PECL Input Clock

The EVM can be configured for differential ECL/PECL input clock mode by configuring the board per Table 3−1 and applying the appropriate ECL/PECL common mode voltage at terminal E1 (VTT). Use J3 and J5 to input the external differential ECL/PECL clock signals.

3.1.1.2 Single-Ended Input Clock

The EVM can be configured for single-ended input clock mode by configuring the board per Table 3−1. SMA connector J3 or header J8 can be used to input the external TTL/CMOS clock signal.

Table 3−1. EVM Clock Configuration

Clock Configuration	Components Installed†	Components Not Installed
Sinewave (Default)	R12, T2, C52	R9, R10, R34, R35, R36, R37, C55, C56
ECL or PECL	R9 (0.01-µF cap.), R10 (0.01-µF cap.)	R36, R12, R34, R35, R37, T2, C55, C56
Single ended TTL/CMOS from J3	R9, C55	R10, R12, R25, R34, R35, R37, T2, C56
Single ended TTL/CMOS from J8	R34, R37, C55	R9, R10, R12, R35, T2, C56

† All component values are per the schematic except where shown in parentheses.

3.1.2 Input Data

The DAC5674 EVM can accept 3.3-V CMOS logic level data inputs through the 40-pin header J8 per Table 3−2. The board provides 50-Ω termination to ground and series dampening resistors to minimize digital ringing and switching noise. J8 also provides a path for an input clock (see Table 3−1 for proper board configuration).

Table 3−2. Input Connector J8

J8 Pin	Description	J8 Pin	Description	J8 Pin	Description
1	CMOS data bit 13 (MSB)	15	CMOS data bit 6	29	Reset
2	GND	16	GND	30	GND
3	CMOS data bit 12	17	CMOS data bit 5	31	
4	GND	18	GND	32	GND
5	CMOS data bit 11	19	CMOS data bit 4	33	
6	GND	20	GND	34	GND
7	CMOS data bit 10	21	CMOS data bit 3	35	
8	GND	22	GND	36	GND
9	CMOS data bit 9	23	CMOS data bit 2	37	
10	GND	24	GND	38	GND
11	CMOS data bit 8	25	CMOS data bit 1	39	SCLK_IN
12	GND	26	GND	40	GND
13	CMOS data bit 7	27	CMOS data bit 0 (LSB)		
14	GND	28	GND		

3.1.3 Output Data

The DAC5674 EVM can be configured to drive a doubly terminated 50-Ω cable or provide unbuffered differential outputs.

3.1.3.1 Transformer Coupled Signal Output

The factory-set configuration of the demonstration board provides the user with a single-ended output signal at SMA connector J7. The DAC5674 is configured to drive a doubly terminated 50-Ω cable using a 1:1 impedance ratio transformer, a 100-Ω terminating resistor R2, and the center tap of T1 connected to ground per Table 3−3. When using a 4:1 impedance ratio transformer, configure the EVM per Table 3−3. The common mode input voltage of T1 can be adjusted by using the resistor divider network R5 and R6.

Table 3−3. Transformer Output Configuration

Configuration	Components Installed†	Components Not Installed
1:1 Impedance ratio transfomer	R2, R3, R4, R6, C22, T1 (1:1)	R5, R7, R8, C20, C21
4:1 Impedance ratio transfomer	R3 (100), R4 (100), R6, C22, T1 (4:1)	R2, R5, R7, R8, C20, C21

† All component values are per the schematic except where shown in parenthesis.

3.1.3.2 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows: remove R2, C20, C21, and T1; Install R3, R4, R7, R8, J1 and J6.

3.1.4 Internal Reference Operation

The full-scale output current is set by applying an external resistor (R1) between the BIASJ pin of the DAC5674 and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying R1 or changing the externally applied reference voltage. The full-scale output current, $IOUT_{FS}$, is defined as follows:

$$IOUT_{FS} = 32 \times (V_{EXTIO}/R1)$$

where V_{EXTIO} is the voltage at pin EXTIO. This voltage is 1.2 V typical when using the internally provided bandgap reference voltage source.

3.1.5 External Reference Operation

The internal reference can be disabled and overridden by an external reference by connecting a voltage source to terminal TP2 (EXT_I/O) and connecting EXTLO to AVDD. The specified range for external reference voltages should be observed (see the DAC5674 data sheet (SLWS148) for details).

3.1.6 Sleep Mode

The DAC5674 EVM provides a means of placing the DAC5674 into a power-down mode. This mode is activated by placing jumper W3 between pins 2 and 3.

3.1.7 Filter Control

The DAC5674 has two inputs, HP1 and HP2, which control the internal interpolation filters (FIR1 and FIR2) mode of operation. When these inputs are set to a logic high, the filters are configured for high-pass response. When set to a logic low, the filters are configured for low-pass response. A third input, X4, allows the user to bypass Interpolation Filter 1. When X4 is set to a logic low, Filter 1 is bypassed. See the data sheet (SLWS148) for more information.

3.1.8 PLL Divider Control

The DAC5674 has two inputs, DIV0 and DIV1, which control the internal PLL prescaler divide ratio setting. These two signals, along with the three filter control signals, are all controlled by DIP switch S2 on the EVM. All control signals are in the logic low level when the DIP switch is in the closed position. See the data sheet (SLWS148) for more information.

Chapter 4

Schematics

This chapter contains the EVM schematic diagrams.

Revision History		
REV	ECN Number	Approved

U1
DAC5674

J8
40PIN_IDC

RP7 (Note 1) 10PIN_SIP_RPACK
RP8 (Note 1) 10PIN_SIP_RPACK
RP1 22
RP2 22
RP4 10PIN_SIP_RPACK
RP6 10PIN_SIP_RPACK

J6 SMA (Note 1)
J7 I_OUT
J1 SMA (Note 1)
J2 SMA
T1 T1-1T-KK81
E2
TP1 RED
TP2 RED
TP6 RED
W1
W2
W3
W4
W5
S1 SW-PB

NOTE 1. PART IS NOT INSTALLED

Engineer: J. SETON			
Drawn By: Y. DEWONCK	SIZE:	DATE: 4-Sep-2003	REV: B
FILE:			SHEET: 1 OF: 3

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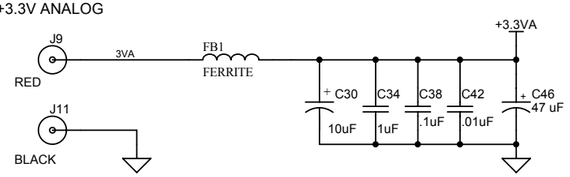
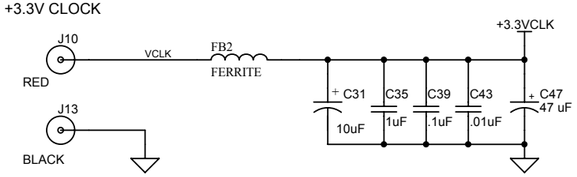
Title: DAC5674

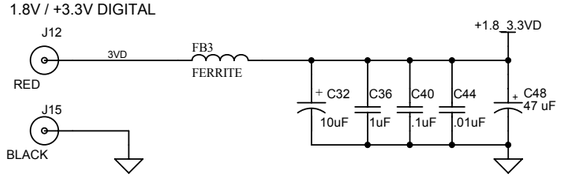
+3.3V ANALOG



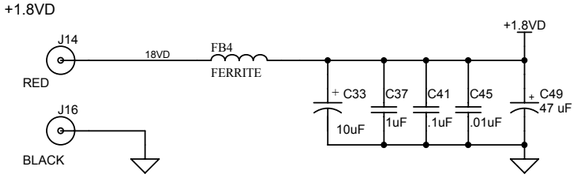
+3.3V CLOCK

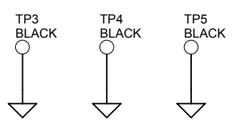


1.8V / +3.3V DIGITAL



+1.8VD





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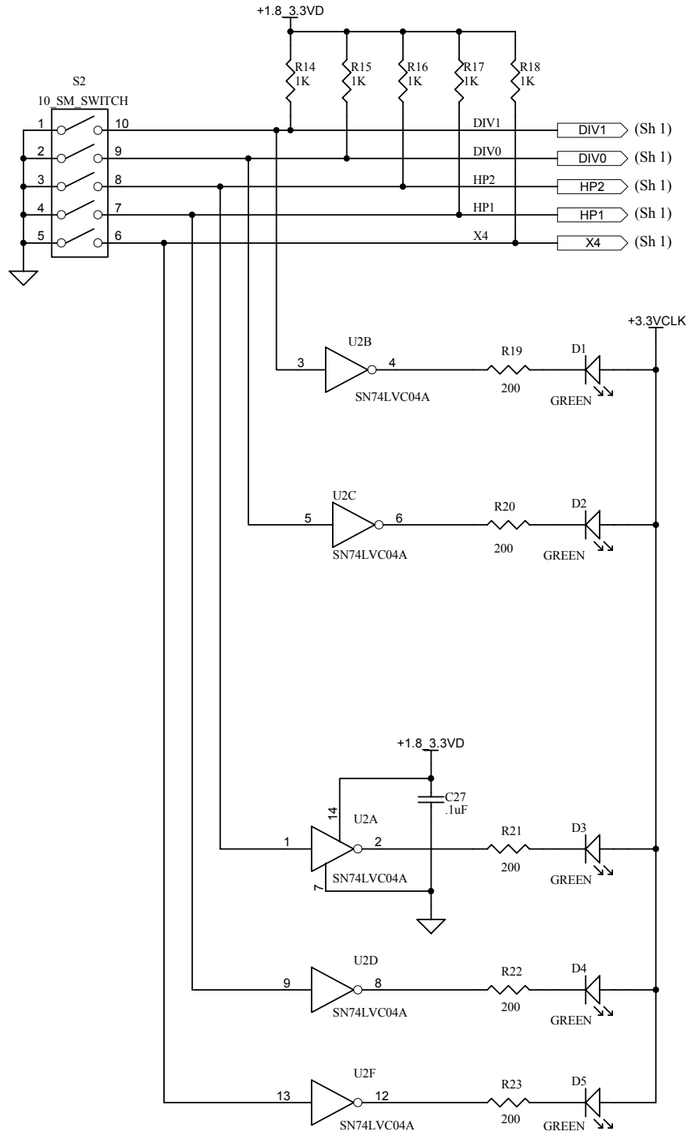
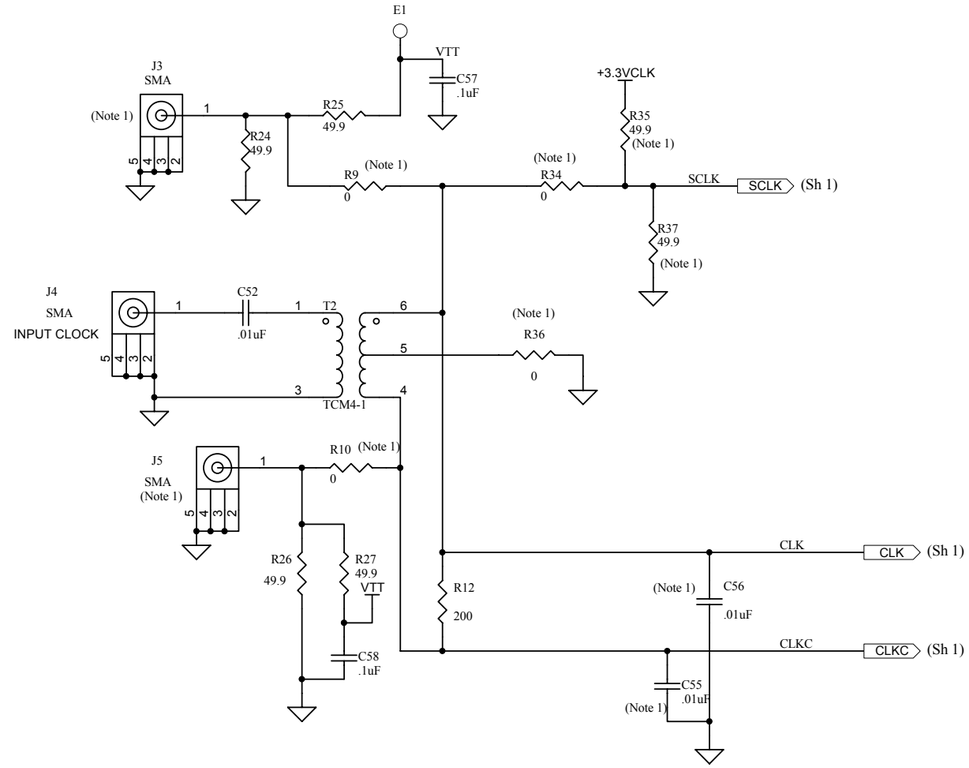
Engineer: J. SETON			
Drawn By: Y. DEWONCK	SIZE:	DATE: 4-Sep-2003	REV: B
FILE:			SHEET: 2 OF: 3





NOTE 1. PART IS NOT INSTALLED

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