

FDMC2523P

P-Channel QFET®

-150V, -3A, 1.5Ω

Features

- Low Crss (typical 10pF)
- Fast Switching
- Low gate charge (typical 6.2 nC)
- Improved dv / dt capability
- RoHS compliant

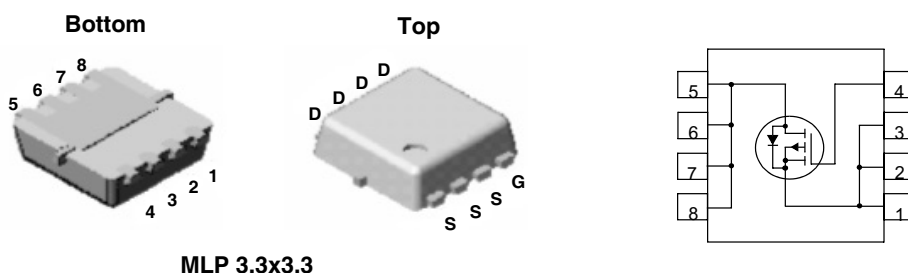


General Description

These P-Channel MOSFET enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Application

- Active Clamp Switch



MLP 3.3x3.3

MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-150	V
V_{GS}	Gate to Source Voltage	± 30	V
I_D	Drain Current - Continuous ($T_C=25^\circ\text{C}$)	-3	A
	- Continuous ($T_C=100^\circ\text{C}$)	-1.8	
	- Pulsed	-12	
P_D	Power Dissipation (Steady State)	25	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$
dv/dt	Peak Diode Recovery dv/dt (Note 2)	-5	V/ns

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	108	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC2523P	FDMC2523P	MLP 3.3X3.3	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	-150			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-138		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -150\text{V}$, $V_{GS} = 0\text{V}$ $T_J = 125^\circ\text{C}$			-1 -10	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0\text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-3	-3.8	-5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -10\text{V}$, $I_D = -1.5\text{A}$ $V_{GS} = -10\text{V}$, $I_D = -1.5\text{A}$, $T_J = 125^\circ\text{C}$		1.1 2.0	1.5 3.6	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -40\text{V}$, $I_D = -1.5\text{A}$ (Note 4)		1.4		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		200	270	pF
C_{oss}	Output Capacitance			60	80	pF
C_{rss}	Reverse Transfer Capacitance			10	15	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		7.5		Ω

Switching Characteristics

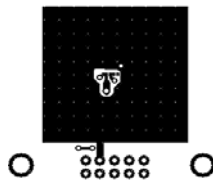
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75\text{V}$, $I_D = -3\text{A}$ $V_{GS} = -10\text{V}$, $R_{GS} = 25\Omega$ (Note 3,4)		15	27	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
t_f	Fall Time			13	24	ns
Q_g	Total Gate Charge	$V_{DS} = -75\text{V}$, $I_D = -3\text{A}$ $V_{GS} = -10\text{V}$ (Note 3,4)		6.2	9	nC
Q_{gs}	Gate to Source Gate Charge			1.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.3		nC

Drain-Source Diode Characteristics

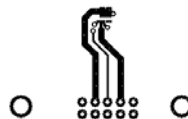
I_S	Maximum Continuous Drain -Source Diode Forward Current			-3	A	
I_{SM}	Maximum Pulse Drain -Source Diode Forward Current			-12	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = -3A$		-1.8	-5	V
t_{rr}	Reverse Recovery Time	$I_F = -3A, di/dt = 100A/\mu s$ (Note 3)		93		ns
Q_{rr}	Reverse Recovery Charge			0.27		nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 52°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 108°C/W when mounted on a minimum pad of 2 oz copper.

Scale 1:1 on letter size paper

- 2: $I_{SD} \leq -3\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
 3: Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$
 4: Essentially independent of operating temperature.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

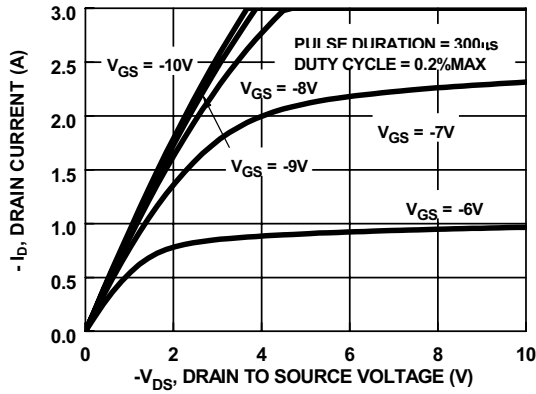


Figure 1. On Region Characteristics

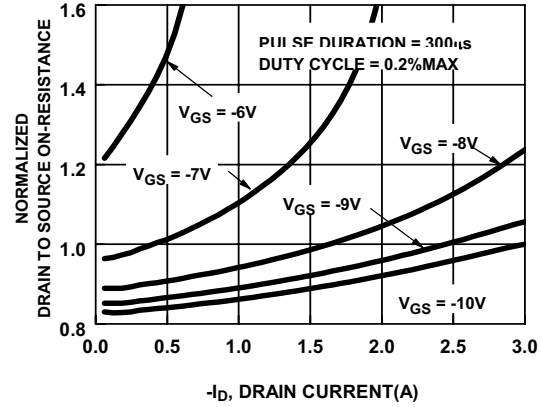


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

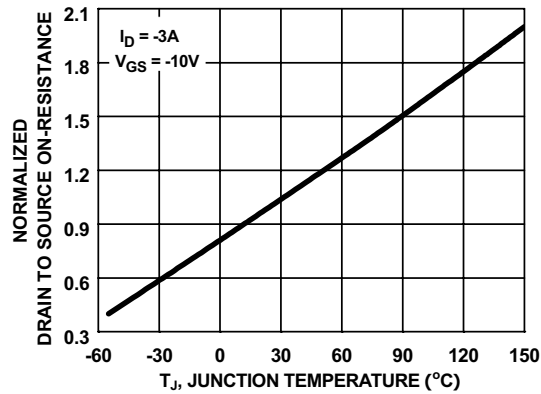


Figure 3. Normalized On Resistance vs Junction Temperature

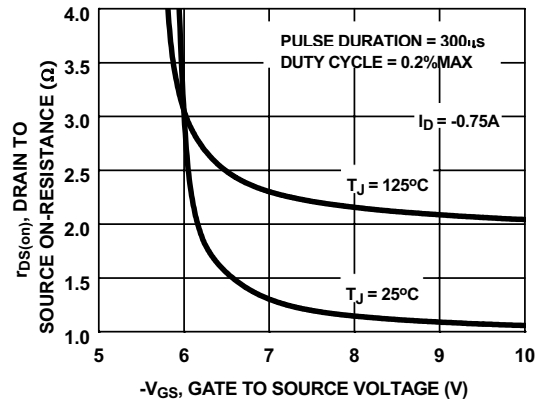


Figure 4. On-Resistance vs Gate to Source Voltage

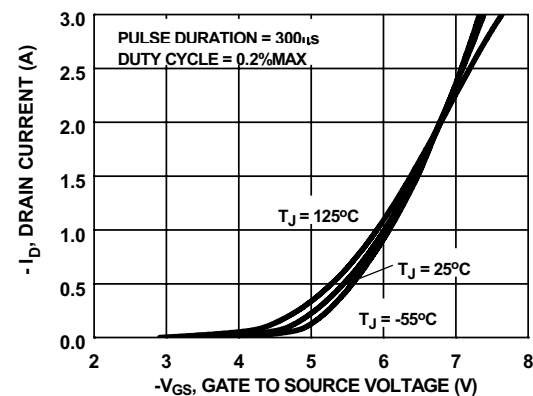


Figure 5. Transfer Characteristics

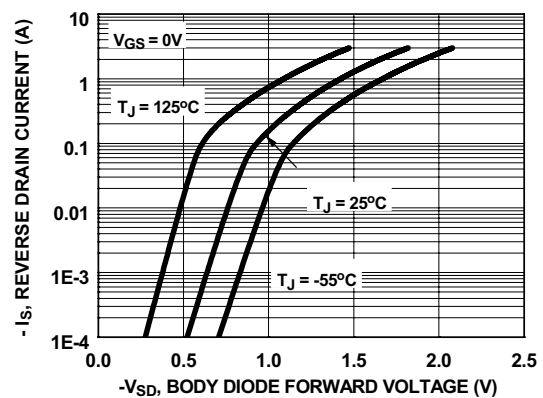


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

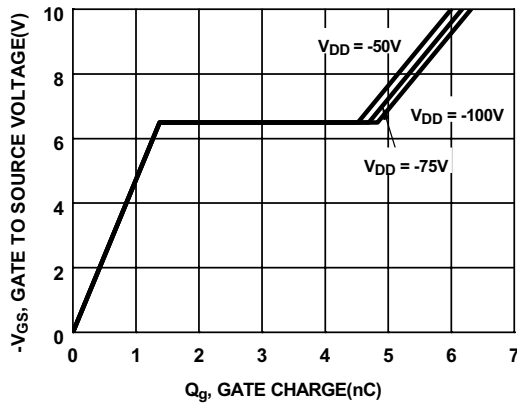


Figure 7. Gate Charge Characteristics

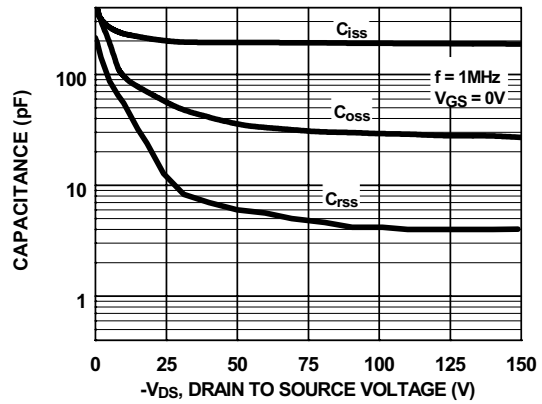


Figure 8. Capacitance vs Drain to Source Voltage

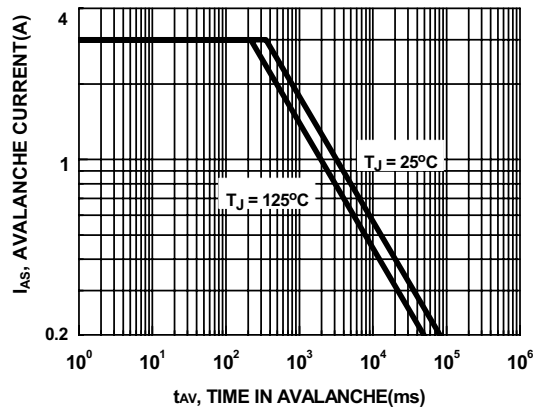


Figure 9. Unclamped Inductive Switching Capability

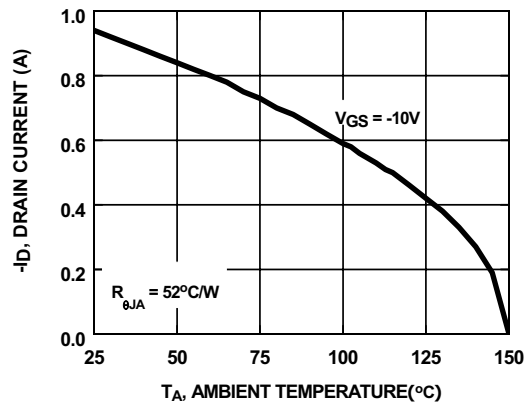


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

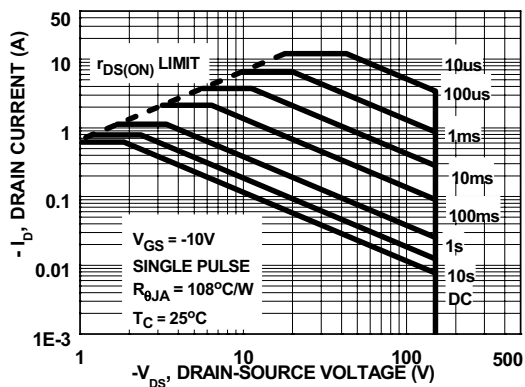


Figure 11. Forward Bias Safe Operating Area

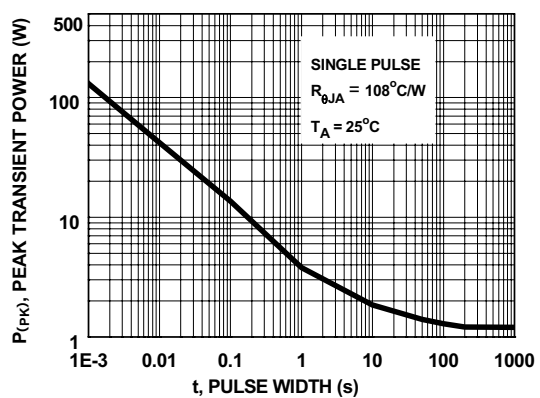
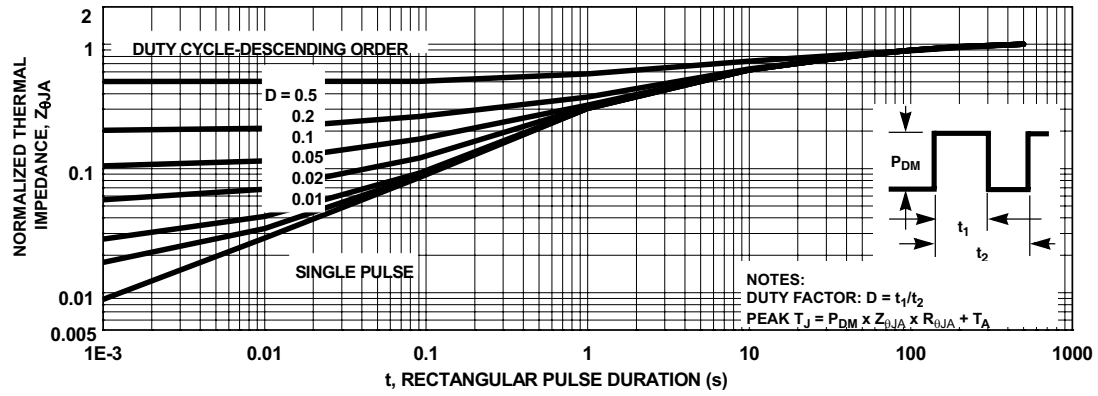
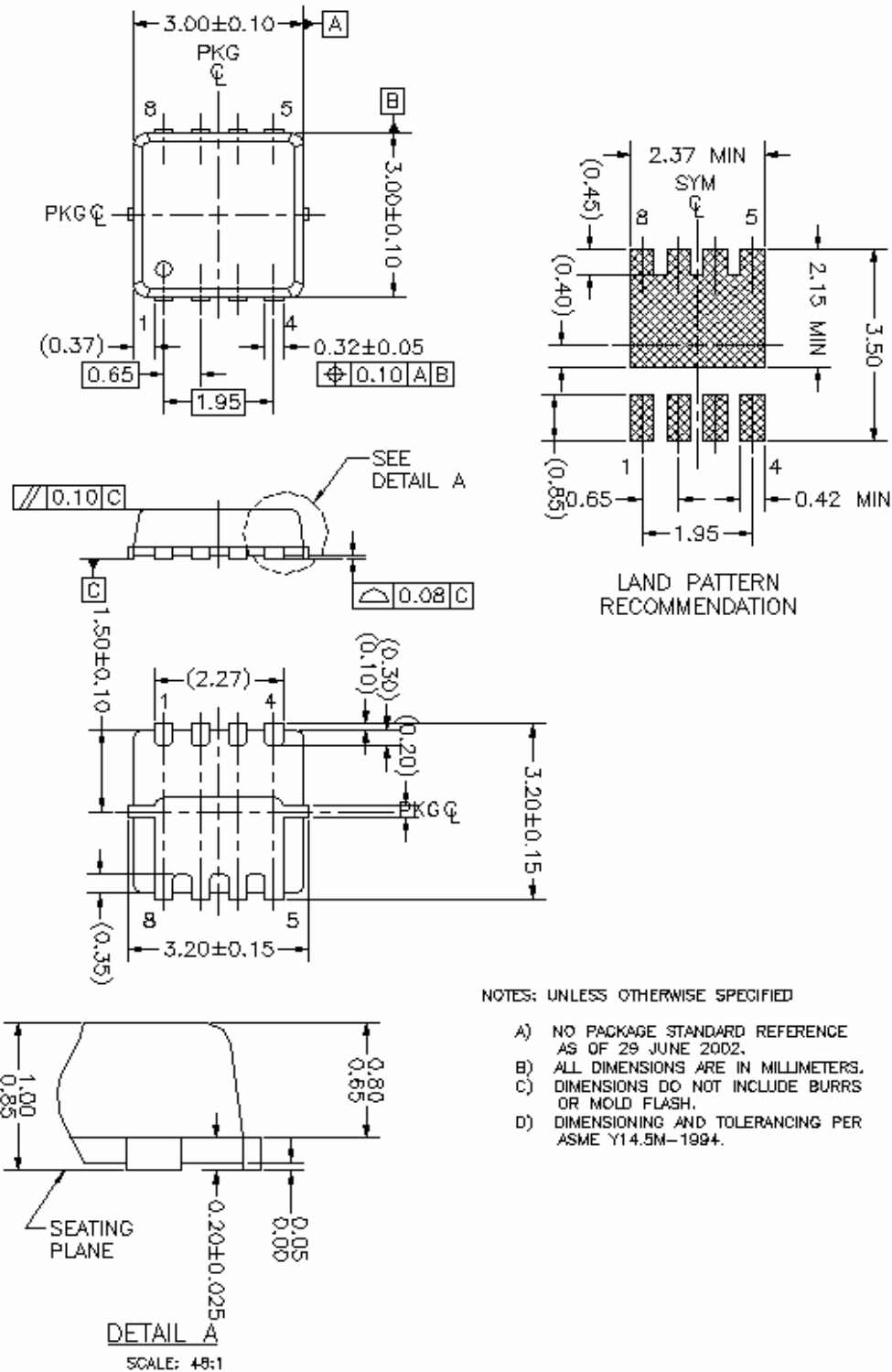


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



Dimensional Outline and Pad Layout



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