5th-Order, Zero-Error, Bessel Lowpass Filter

General Description

The MAX281 is a 5th-order all-pole instrumentation lowpass filter with no DC error. The filter uses an external resistor and capacitor to isolate the integrated circuit from the DC signal path, thus providing DC accuracy.

The external resistor and capacitor together with the on-chip 4th-order switched capacitor filter form a 5th-order Bessel lowpass filter. Bessel lowpass filters provide linear phase (constant group delay) response from DC to beyond the filter cutoff frequency, with some reduction in stopband attenuation.

The filter cutoff frequency is set by a clock which can be either internally generated or externally provided. The clock to cutoff frequency ratio of 101 allows easy removal of clock ripple.

MAX281A provides tighter specfications than the MAX281B for internal clock oscillator frequency and buffer amplifier offset voltage.

MAX280 is available for applications requiring a maximally flat (Butterworth) amplitude response.

Applications

Anti-Aliasing Filters

Data Loggers

Digital Voltmeters

Weigh Scales

Strain Gauges

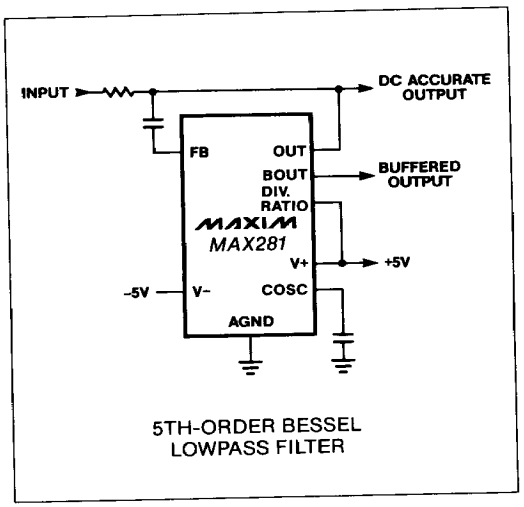
Features

- **Bessel Lowpass Filter with No DC Error**
- **Low Passband Noise**
- **DC to 20kHz Cutoff Frequency**
- **5th-Order All-Pole Bessel Response**
- **Internal or External Clock**
- **Cascadable for Higher Order Rolloff**
- **Buffered Output Available**
- **8-Pin DIP or 16-Pin Wide SO Packages**

Ordering Information

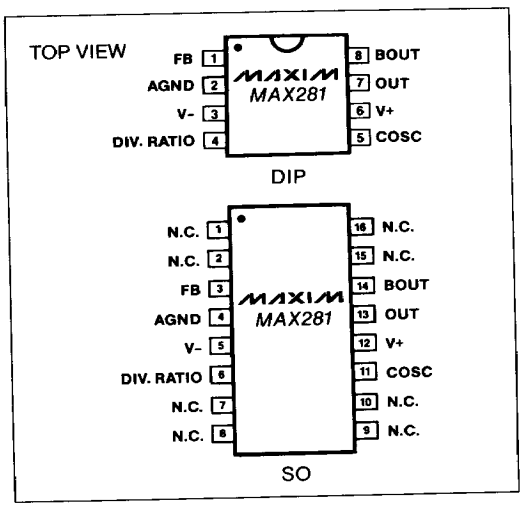
PART	TEMP. RANGE	PIN-PACKAGE
MAX281ACPA	0°C to +70°C	8 Plastic DIP
MAX281BCPA	0°C to +70°C	8 Plastic DIP
MAX281ACWE	0°C to +70°C	16 Wide SO
MAX281BCWE	0°C to +70°C	16 Wide SO
MAX281C/D	0°C to +70°C	Dice
MAX281AEPA	-40°C to +85°C	8 Plastic DIP
MAX281BEPA	-40°C to +85°C	8 Plastic DIP
MAX281AEWE	-40°C to +85°C	16 Wide SO
MAX281BEWE	-40°C to +85°C	16 Wide SO
MAX281AMJA	-55°C to +125°C	8 CERDIP
MAX281BMJA	-55°C to +125°C	8 CERDIP

Typical Operating Circuit



5TH-ORDER BESSEL LOWPASS FILTER

Pin Configurations



MAXIM is a registered trademark of Maxim Integrated Products.

This Material Copyrighted By Its Respective Manufacturer

5th-Order, Zero-Error, Bessel Lowpass Filter

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V–) 17V
Input Voltage at Any Pin .... V- (-0.3V) ≤ V_{IN} ≤ V+ (+0.3V)
Power Dissipation
Plastic DIP (derate at 6.25mW/°C above 70°C) ... 500mW
CERDIP (derate at 8.00mW/°C above 70°C) 640mW
SO (derate at 9.52mW/°C above 70°C) 762mW

Operating Temperature
MAX281_C___ ..... -0°C to +70°C
MAX281_E___ ..... -40°C to +85°C
MAX281_M___ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature Range (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted, AC output measured at OUT pin, Figure 1.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Dual Supply Single Supply			 ±2.375 4.75		 ±8 16	V
Power-Supply Current	COSC (Pin 5 to V-) = 100pF $T_A = T_{MIN}$ to T_{MAX}			5	10	mA
Input Frequency Range				0-20		kHz
Filter Gain at $f_{IN} = 0$ $f_{IN} = 0.5f_C$ (Note 1)	f_{CLK} = 100kHz Pin 4 at V+ C = 0.01µF R = 18.61kΩ	T_A = +25°C		0 -0.9	 -1.2	dB
$f_{IN} = f_C$ $f_{IN} = 2f_C$ $f_{IN} = 4f_C$		$T_A = T_{MIN}$ to T_{MAX}	-2.5 -12 -35	-3.5 -14 -39		
Clock to Cutoff Frequency Ratio f_{CLK}/f_C	f_{CLK} = 100kHz, Pin 4 at V+ C = 0.01µF, R = 25.78kΩ			101		
Filter Gain at f_{IN} = 4fc	f_{CLK} = 400kHz, Pin 4 at V+ C = 0.01µF, R = 4.65kΩ $T_A = T_{MIN}$ to T_{MAX}		-32	-37		dB
f_{CLK}/f_C Tempco	Same as above			10		ppm/°C
Filter Output (Pin 7) DC Swing	Pin 7 buffered with an ext op amp $T_A = T_{MIN}$ to T_{MAX}		±3.5	±3.8		V
Clock Feedthrough				10		mV_{p-p}
INTERNAL BUFFER						
Bias Current	T_A = +25°C $T_A = T_{MIN}$ to T_{MAX}			2 170	50 1000	pA
Offset Voltage	MAX281A MAX281B			0.2 2	2 20	mV
Voltage Swing	20kΩ; $T_A = T_{MIN}$ to T_{MAX}		±3.5	±3.8		V
Short-Circuit Current Source/Sink				30/2		mA
CLOCK (NOTE 2)						
Internal Oscillator Frequency	COSC (Pin 5 to V-) = 100pF	MAX281A MAX281B	31 25	35 35	39 50	kHz
	$T_A = T_{MIN}$ to T_{MAX} COSC (Pin 5 to V-) = 100pF	MAX281A MAX281B	29 15	35 35	43 65	
Max Clock Frequency				4		MHz
COSC Input Sink/Source Current	$T_A = T_{MIN}$ to T_{MAX}			25	80	µA

Note 1: f_C is the corner frequency of the filter.
Note 2: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V+, f_{CLK}/f_C = 101; when pin 4 = GND, f_{CLK}/f_C = 202 when pin 4 = V-, f_{CLK}/f_C = 404.

This Material Copyrighted By Its Respective Manufacturer

5th-Order, Zero-Error, Bessel Lowpass Filter

Pin Description

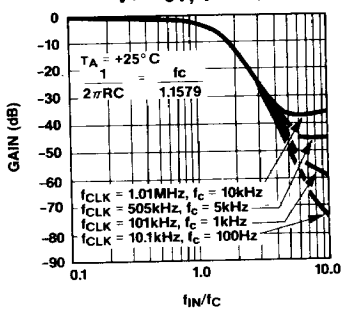
NAME	FUNCTION
FB	External capacitor couples to the chip through this pin.
AGND	Ground. Connect to system ground for dual-supply operation or mid-supply for single operation. This pin should be well bypassed using a large capacitor for single-supply operation.
V-	Negative Supply Voltage
DIVIDER RATIO	Strapped to select clock to cutoff ratio (external clock), or internal divider ratio (internal oscillator).

Voltage at pin 4	EXT fosc/fc	INT divisor
V+	101	1
GND	202	2
V-	404	4

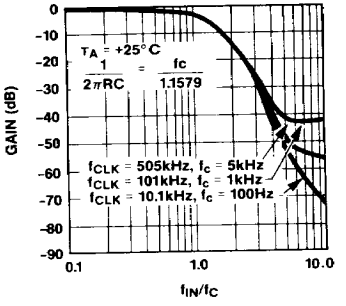
NAME	FUNCTION
COSC	Clock input pin for external clock applications. For internal clock operation, connect an external capacitor between this pin and V-.
V+	Positive Supply Voltage
OUT	Input to on-chip buffer amplifier
BOUT	Output of buffer amplifier

Typical Operating Characteristics

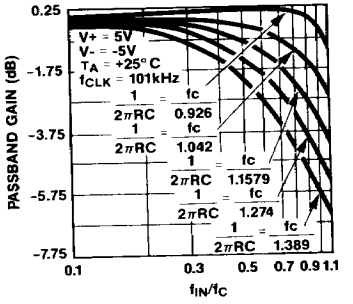
GAIN NORMALIZED TO CUTOFF FREQUENCY
V+ = 5V, V- = -5V



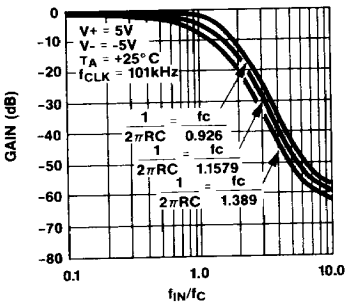
GAIN NORMALIZED TO CUTOFF FREQUENCY
V+ = 5V, V- = -5V



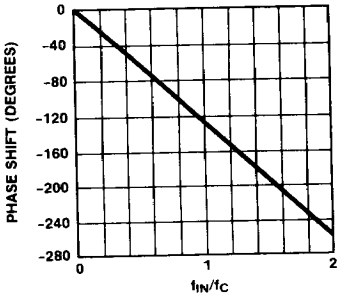
PASSBAND GAIN vs. INPUT FREQUENCY



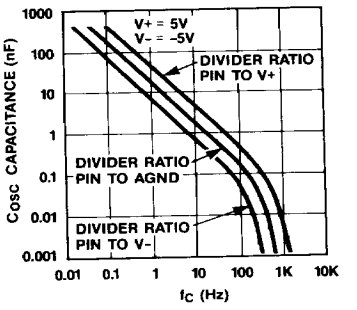
GAIN vs. INPUT FREQUENCY



PHASE SHIFT vs. INPUT FREQUENCY



CUTOFF FREQUENCY vs. COSC

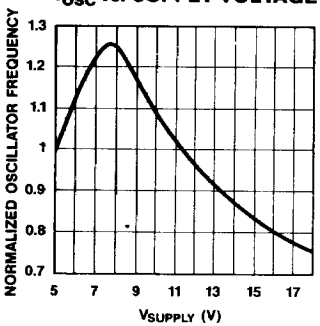


This Material Copyrighted By Its Respective Manufacturer

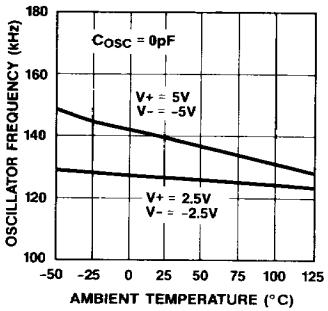
5th-Order, Zero-Error, Bessel Lowpass Filter

Typical Operating Characteristics (continued)

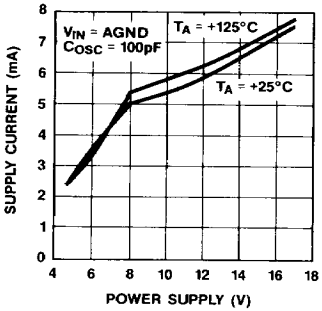
NORMALIZED OSCILLATOR FREQUENCY f_{OSC} vs. SUPPLY VOLTAGE



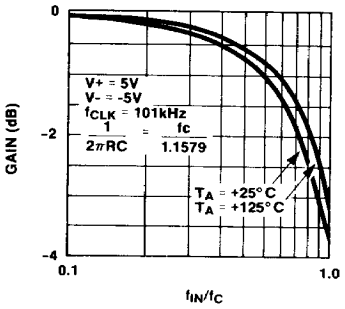
OSCILLATOR FREQUENCY f_{OSC} vs. AMBIENT TEMPERATURE



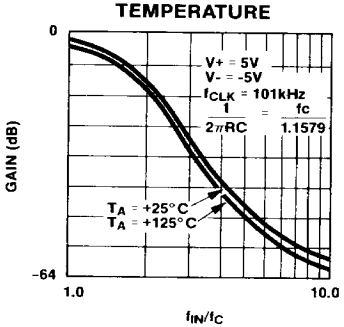
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



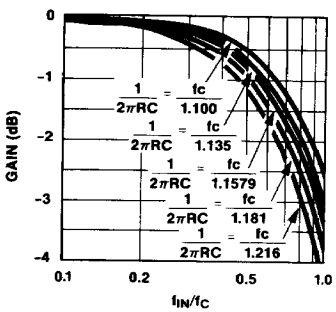
VARIATION OF PASSBAND GAIN WITH TEMPERATURE



VARIATION OF GAIN WITH TEMPERATURE

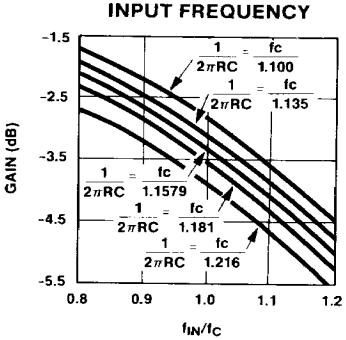


PASSBAND GAIN vs. INPUT FREQUENCY



V+ = 5V
V- = -5V
TA = +25°C
fCLK = 101kHz

GAIN vs. INPUT FREQUENCY



V+ = 5V
V- = -5V
TA = +25°C
fCLK = 101kHz

This Material Copyrighted By Its Respective Manufacturer

Introduction

Figure 1 illustrates the architecture of the circuit. The output voltage is sensed through an internal buffer, then applied to an internal switched capacitor network which drives the bottom plate of an external capacitor to form a 5th-order, lowpass filter. The input and output appear across an external resistor, and the IC part of the overall filter handles only the AC path of the signal. The DC offsets of the buffer and the switched-capacitor network are blocked by the capacitor and do not appear at the zero-offset output pin.

Use of this external resistor and capacitor also automatically provides the required anti-aliasing filtering for the sampled filter. Further, low-frequency noise in the filter IC is attenuated by the external capacitor since any noise at the FB pin goes through a highpass path to the filter output. The filter output pin is unbuffered. This signal can be buffered by the on-chip buffer or by a high-accuracy op amp (such as a chopper stabilized op amp) to obtain a buffered DC accurate system. The on-chip buffer has an offset voltage of 2mV for the MAX281A and 20mV for the MAX281B. The offset voltage for both devices have a typical tempco of 1μV/°C.

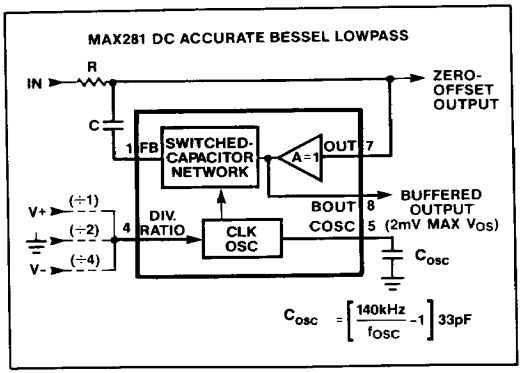


Figure 1. Block Diagram

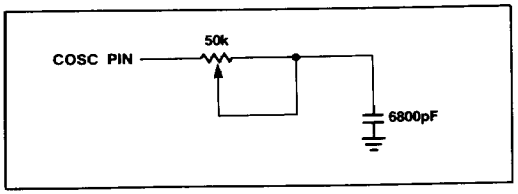


Figure 2. External Oscillator Trim

Detailed Description

Clock Requirements

The MAX281 operates either on its internal oscillator or an externally supplied clock.

Using an Internal Oscillator

The MAX281 contains an internal 140kHz (nominal) oscillator. This frequency can be modified by connecting an external capacitor in parallel with the on-chip 33pF capacitor; from the COSC pin to GND (or to V- if the capacitor is polarized).

When using the internal oscillator, connect the DIVIDER RATIO pin to V+ for 1/1, to GND for a 2/1, and to V- for a 4/1 f_{OSC}/f_{CLK} ratio.

The oscillator frequency can be calculated by:

$$f_{OSC} = 140kHz\ (33pF/(33pF+C_{OSC})\ ) \quad (1)$$

Due to process tolerances, f_{OSC} can vary by ±62.5% in the MAX281B. In the MAX281A, on-chip trimming reduces the f_{OSC} tolerance to ±19.5%. The oscillator frequency can be adjusted by adding a series potentiometer between the capacitor and the COSC pin (Figure 2). The new frequency can be computed as:

$$f'_{OSC} = f_{OSC}/(1-4RC_{OSC}f_{OSC}) \quad (2)$$

where f_{OSC} is the value of the oscillator frequency when R = 0. When an external potentiometer is used, the new value of the oscillator frequency is always higher than the one calculated in (equation 1). To achieve a wide tuning range, calculate (equation 1) the ideal f_{OSC}, C_{OSC} pair, then double the value of C_{OSC} and use a 50k potentiometer to adjust f'_{OSC}. For example, to obtain a 1kHz oscillator frequency, C_{OSC} is 3900pF. By using 6800pF for C_{OSC} and a 50kΩ potentiometer, the clock frequency can be adjusted from 500Hz to 1.56kHz. The internal oscillation frequency can be measured directly at the COSC pin using a low-capacitance probe.

Using an External Clock

Depending upon the connection of the DIVIDER RATIO pin, the internal switched capacitor filter requires a clock 101, 202, or 404 times higher than the desired cutoff frequency. If an external clock is used, the input on the COSC pin must swing close to the power rails (V+,V-). Although standard 74HC00 series CMOS gates do not guarantee CMOS levels with the source and sink currents of the COSC pin, they will in reality drive the COSC pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and current to simultaneously drive several chips. The typical trip levels of the internal Schmitt trigger sensing COSC pin are:

POWER SUPPLY		TRIP LEVEL	
V+ = +2.5V	V- = -2.5V	V_{IH} = 0.9V	V_{IL} = -1.15V
V+ = +5V	V- = -5V	V_{IH} = 1.4V	V_{IL} = -2.1V
V+ = +6V	V- = -6V	V_{IH} = 1.7V	V_{IL} = -2.5V
V+ = +5V	V- = 0V	V_{IH} = 3.4V	V_{IL} = 1.35V
V+ = +10V	V- = 0V	V_{IH} = 6.4V	V_{IL} = 2.9V
V+ = +15V	V- = 0V	V_{IH} = 9.5V	V_{IL} = 4.1V

This Material Copyrighted By Its Respective Manufacturer

5th-Order, Zero-Error, Bessel Lowpass Filter

Choosing External Resistor and Capacitor Values

The external resistor and capacitor are used as part of a feedback loop for the filter and also forms one pole. The internal 4-pole switched-capacitor filter is driven by a clock which also determines the filter cutoff frequency. For a proper Bessel response, the clock and DIVIDER RATIO pin should be set to provide the desired cutoff frequency. Additionally, the resistor and capacitor should be chosen such that:

$$\frac{f_C}{1.1579} = \frac{1}{2\pi RC}$$

where f_C = filter cutoff frequency.

For example to implement a 10Hz cutoff filter, set:

$$1/2\pi RC = 10Hz/1.1579 = 8.6363Hz$$

R is typically ≈ 20kΩ. The minimum value of R depends upon the maximum input signal, and the current sinking capability of the FB pin (typically 1mA). So for a $1V_{p-p}$ signal, the minimum value of the resistor is 1kΩ.

The passband response for values of $1/(2\pi RC)$ around $(f_C/1.1579)$ can be seen on the Passband Gain vs. Input Frequency plots (see Typical Operating Characteristics). For optimum Bessel response, the RC product should be well controlled. Note that an inaccurate RC product can cause excessive peaking at the FB pin (Figure 3), which results in clipping and distortion of the output waveform.

For wide temperature range applications, NPO ceramic capacitors are recommended. Their tempcos are around ±20ppm and values are available to 0.1μF. Other ceramic capacitors are not recommended due to their large tempcos. Mylar, polystyrene and polypropylene capacitors all provide acceptable performance. Solid tantalum capacitors connected back-to-back and disc ceramic capacitors introduce additional passband errors (0.05-0.1dB).

Applications Information

Filter Input Voltage Range

Every node of the filter typically swings within 1V of both supplies. With the appropriate external resistor and capacitor values, the amplitude response of all the internal and external nodes should not exceed a gain of 0dB with the exception of the FB pin. The amplitude response of the FB pin, where some peaking may occur, is shown in Figure 3.

With ±5V supplies, the peak-to-peak input voltage should not exceed 6.5V. If the input voltage goes beyond this value, clipping and distortion of the output waveform may occur; however, the filter will not be damaged. The absolute maximum input voltage to any pin should not exceed the power supplies.

Internal Buffer

The internal output buffer of the FB pin and the OUT pin is part of the AC signal path. Hence, capacitive loading greater than 30pF can cause gain errors in the passband around the cutoff frequency. The internal buffer can also be used as the filter output, however, there will be a few millivolts of output offset.

Filter Attenuation

The rolloff is 30dB/octave. When the clock rate is increased and hence the cutoff frequency is increased, the filter's maximum attenuation decreases as shown in the Typical Operating Characteristics. This decrease is caused by rolloff at higher frequencies of the loop gains of the various internal feedback paths and is not due to any increase in noise floor.

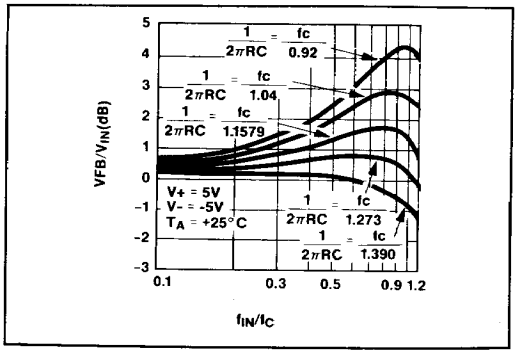


Figure 3. Amplitude Response of FB Pin

Filter Noise

The filter wideband noise is typically $90\mu V_{RMS}$ with ±5V supplies and typically $80\mu V_{RMS}$ for ±2.5V supplies or a +5V single supply. This value is nearly independent of the cutoff frequency. The noise spectral density, unlike conventional active filters, is nearly zero for frequencies below $0.1f_C$. Roughly 2/3 of the entire wideband noise is in the band DC to f_C.

Transient Response

Figure 4 shows the step response of the filter where f_C = 1kHz. This response approximates an ideal 5th-order Bessel filter. The absence of overshoot is characteristic of the Bessel response.

Anti-Aliasing

The internal 4th-order switched-capacitor filter is a sampled device, and as such will alias unless preceded by a band limited signal or a continuous non-sampled filter. The external resistor and capacitor used to form the 5th filter pole also automatically provides this function. Attenuation is greater than 35dB at the Nyquist frequency.

This Material Copyrighted By Its Respective Manufacturer

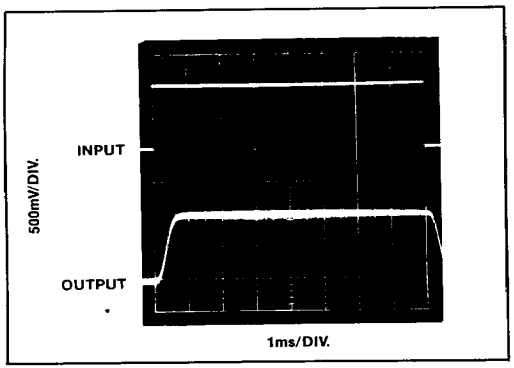


Figure 4. Step Response of MAX281 for f_C = 1kHz

Single-Supply Operation

Figure 5A shows a schematic for single-supply operation. The AGND pin and the OUT pin should be biased at 1/2 supply. The value of the resistors, R1 and R2, should be chosen to conduct 100μA or more. R' DC biases the buffer and C' isolates the buffer from the DC value of the output. Under these conditions, the external resistor and capacitor should be adjusted such that (1/2πRC) = 1.2737. This accounts for the extra loading of the R',C' combination. R' and C' are not required if the input voltage has a DC value around 1/2 supply. If an external capacitor is used to activate the internal oscillator, its bottom plate should be tied to system ground. The AGND pin should also be bypassed by a decoupling capacitor.

Figures 5B and 5C illustrate the passband and stopband frequency response for both single- and dual-supply operation.

Clock Feedthrough

Clock feedthrough can be reduced by using a resistor and capacitor at the buffered output pin provided that this pin is used as an output. An active filter at the DC accurate output can act as a buffer and provide clock feedthrough filtering.

Cascading for Higher Order Filters

Two chips can be cascaded with or without intermediate buffers. Figure 6 shows a buffered arrangement which corrects for loading of the output when the first stage is used to drive the input of the next stage. This introduces a maximum DC error of 2mV over temperature at VOUT.

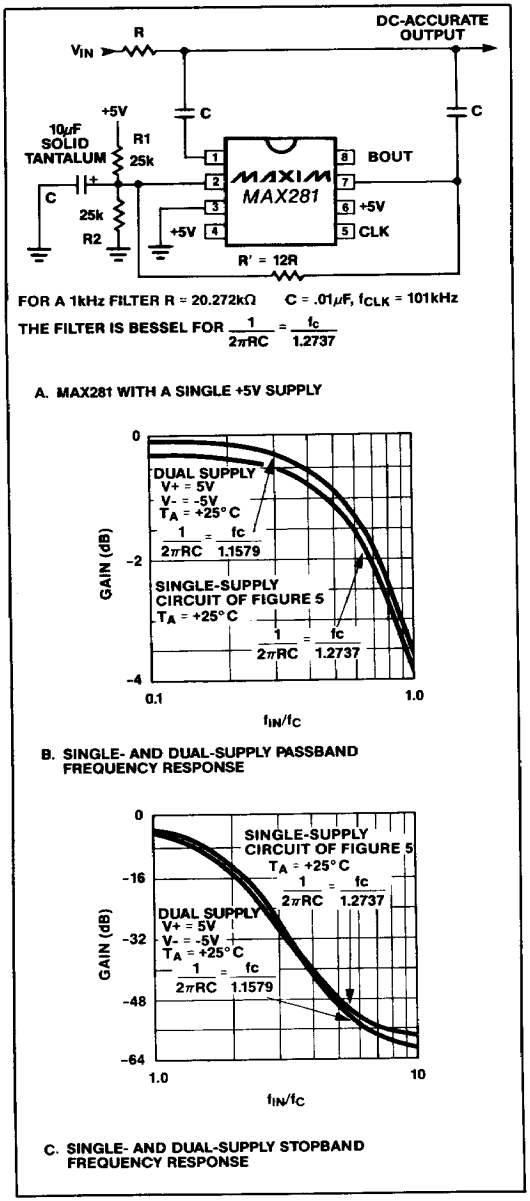


Figure 5. Operation from a Single +5V Supply

This Material Copyrighted By Its Respective Manufacturer

5th-Order, Zero-Error, Bessel Lowpass Filter

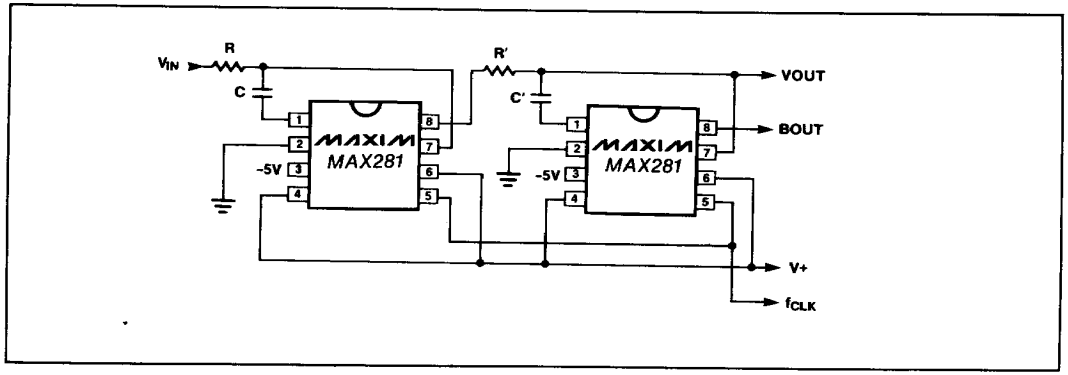


Figure 6. Cascading Two MAX281 filters. The 2nd Stage is Driven by the Buffered Output of the First Stage

Application Circuits

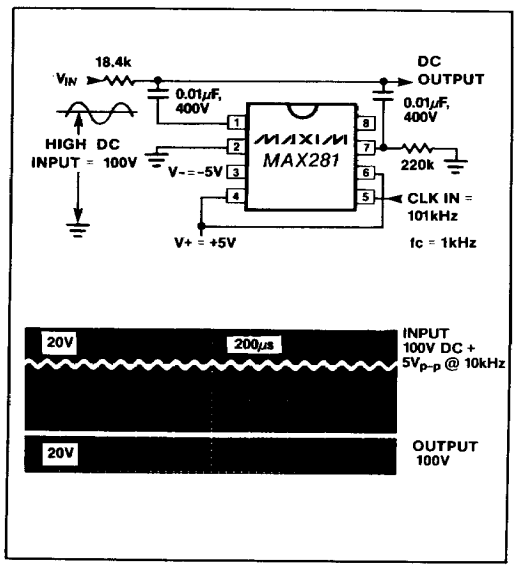
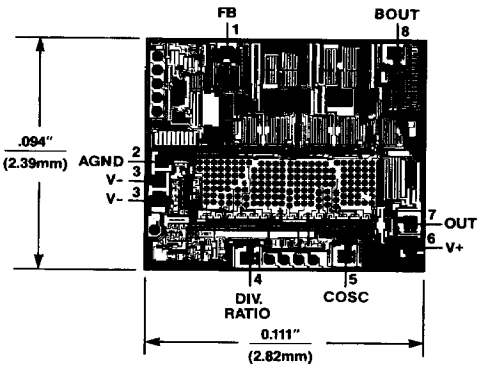


Figure 7. Filtering AC Signals from High DC Voltages

Filtering High DC Voltages

In Figure 7, a MAX281 removes undesired AC components from a DC voltage much higher than the operating voltage of the filter IC. This is possible due to the shunt architecture of these filters and is not generally possible with conventional active filter structures.

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

This Material Copyrighted By Its Respective Manufacturer