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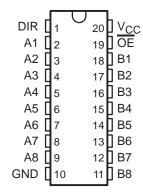
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
  1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Plastic (N) and Ceramic (J) DIPs

### description

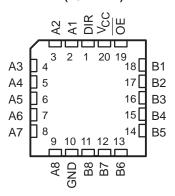
These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT245 . . . J OR W PACKAGE SN74ABT245A . . . DB, DW, N, OR PW PACKAGE (TOP VIEW)



SN54ABT245 . . . FK PACKAGE (TOP VIEW)



The SN74ABT245A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

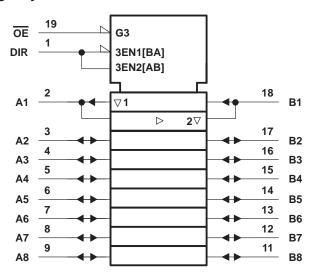
The SN54ABT245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74ABT245A is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

#### **FUNCTION TABLE**

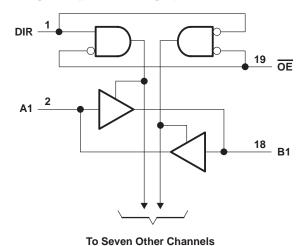
INP	UTS	OPERATION						
OE	DIR							
L	L	B data to A bus						
L	Н	A data to B bus						
Н	X	Isolation						

EPIC-IIB is a trademark of Texas Instruments Incorporated

## logic symbol<sup>†</sup>



## logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage applied to any output in the high state or power-off state,	$V_{\mbox{\scriptsize O}}$ –0.5 V to 5.5 V
Current into any output in the low state, IO: SN54ABT245	96 mA
SN74ABT245A	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 2	): DB package 0.6 W
	DW package 1.6 W
	N package 1.3 W
	PW package 0.7 W
Storage temperature range	65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# recommended operating conditions (see Note 3)

		SN54ABT245		SN74ABT245A		UNIT
		MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	VCC	0	VCC	V
ЮН	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

# **SN54ABT245, SN74ABT245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST COM	T,	A = 25°C	;	SN54ABT245		SN74ABT245A		UNIT		
		TEST CONI	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII		
VIK		$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V	
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5			
\/		$V_{CC} = 5 V$ ,	$I_{OH} = -3 \text{ mA}$	3			3		3		V I	
VOH		V <sub>CC</sub> = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				ľ	
		VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2			
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA			0.55		0.55			· v	
		VCC = 4.5 V	I <sub>OL</sub> = 64 mA			0.55*				0.55		
ļ.,	Control inputs	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	$V_I = V_{CC}$ or GND			±1		±1		±1		
11	A or B ports	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$	$V_I = V_{CC}$ or GND			±20		±100		±20	μΑ	
lozpu		$V_{CC} = 0 \text{ to } 2.1 \text{ V},$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V},$	$\overline{OE} = X$			±50				±50	μА	
lozpd		$V_{CC} = 2.1 \text{ V to } 0,$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V},$	OE = X			±50				±50	μΑ	
I <sub>OZH</sub> ‡		$\frac{\text{V}_{\text{CC}}}{\text{OE}} = 2.1 \text{ V to } 5.5 \text{ V},$	$V_0 = 2.7 V$ ,			10		10		10	μΑ	
I <sub>OZL</sub> ‡		$\frac{\text{V}_{\text{CC}}}{\text{OE}} = 2.1 \text{ V to } 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V,			-10		-10		-10	μΑ	
loff		$V_{CC} = 0$ ,	$V_I$ or $V_O \le 4.5 \text{ V}$			±100				±100	μΑ	
ICEX	Outputs high	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V			50		50		50	μΑ	
IO§		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V	-50	-140	-180	-50	-180	-50	-180	mA	
		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		5	250		250		250	μΑ	
ICC	A or B ports		Outputs low		22	30		30		30	mA	
			Outputs disabled		1	250		250		250	μΑ	
	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled			1.5		1.5		1.5	mA	
			Outputs disabled			50		50		50	μА	
	Control inputs	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND				1.5		1.5		1.5	mA	
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			4						pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			8						pF	

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current. § Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>¶</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

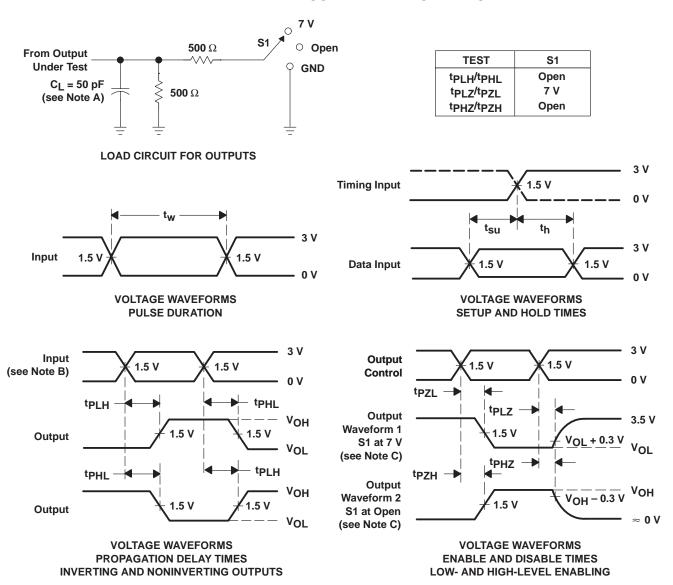
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# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

	FROM (INPUT)	TO (OUTPUT)	SN54ABT245					SN74ABT245A					
PARAMETER			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX			MIN	TYP	MAX			
<sup>t</sup> PLH	A or B	B or A	1	2.6	4.1	1	4.8	1	2	3.2	1	3.6	ns
t <sub>PHL</sub>			1	2.9	4.2	1	4.8	1	2.6	3.5	1	3.9	
<sup>t</sup> PZH	- ŌE	A or B	1.3	3.3	4.8	1	5.9	2	3.5	4.5	2	5.6	ns
t <sub>PZL</sub>		AOIB	2.3	4.3	5.8	2	7.5	1.9	4	5.3	1.9	6.2	115
<sup>t</sup> PHZ	ŌĒ	A or B	1.7†	4.7	6.2	1.7	7.4	2.2	4.4	5.4	2.2	5.9	ns
tPLZ		OE	AUIB	1.7†	4.3	5.8	1.7	6.5	1.5	3	4	1.5	4.5

<sup>†</sup>This data sheet limit may vary among suppliers.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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