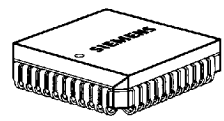
SIEMENS

Stand Alone
Full CAN Controller

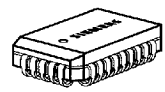
SAE 81C90/91

Preliminary Data

- Full CAN controller for data rate up to 1 Mbaud
- Complies with CAN specification V2.0 part A (part B passive)
- Up to 16 messages simultaneous (each with maximum data length)
- Message identifier reprogrammable "on the fly"
- Several transmit jobs can be sent with a single command
- Transmit check
- Basic CAN feature
- Time stamp for eight messages
- Two host interfaces (parallel and serial)
- User-configurable outputs for different bus concepts
- Programmable clock output
- Two 8 bit I/O-Port extension (P-LCC-44-1 package only)



P-LCC-44-1



P-LCC-28-1

The device comes in two versions:

SAE 81C90 in a P-LCC-44-1 package with two 8-bit I/O ports, and

SAE 81C91 in a P-LCC-28-1 package without I/O ports. **Ordering Information**

Type	Ordering Code	Package	Function
SAE 81C91	Q67121-F0001	P-LCC-28-1	Stand Alone Full CAN Controller Temperature range – 40 to + 110 °C
SAE 81C90	Q67121-H9038	P-LCC-44-1	Stand Alone Full CAN Controller Temperature range – 40 to + 110 °C

Introduction

The Siemens Stand Alone Full CAN (SFCAN) circuit incorporates all the parts for completely autonomous transmission and reception of messages using the CAN protocol. The flexible, programmable interface allows hookup to different implementations of the physical layer. The link to a host controller can be made either by a multiplexed 8-bit address/data bus or by a high-speed, serial synchronous interface.

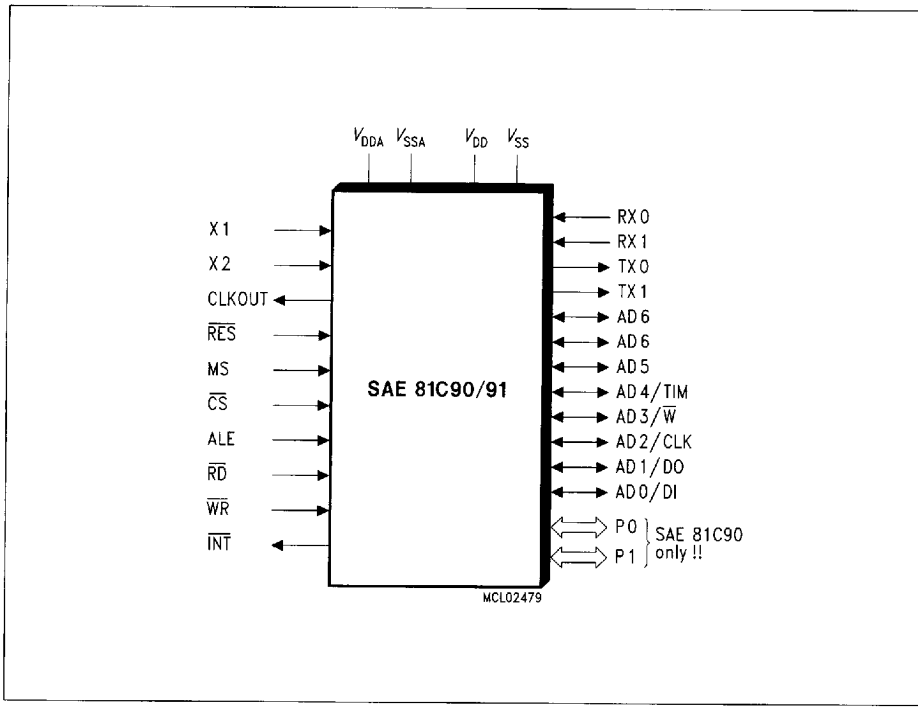


Figure 1
Logic Symbol

Pin Configurations
(top view)

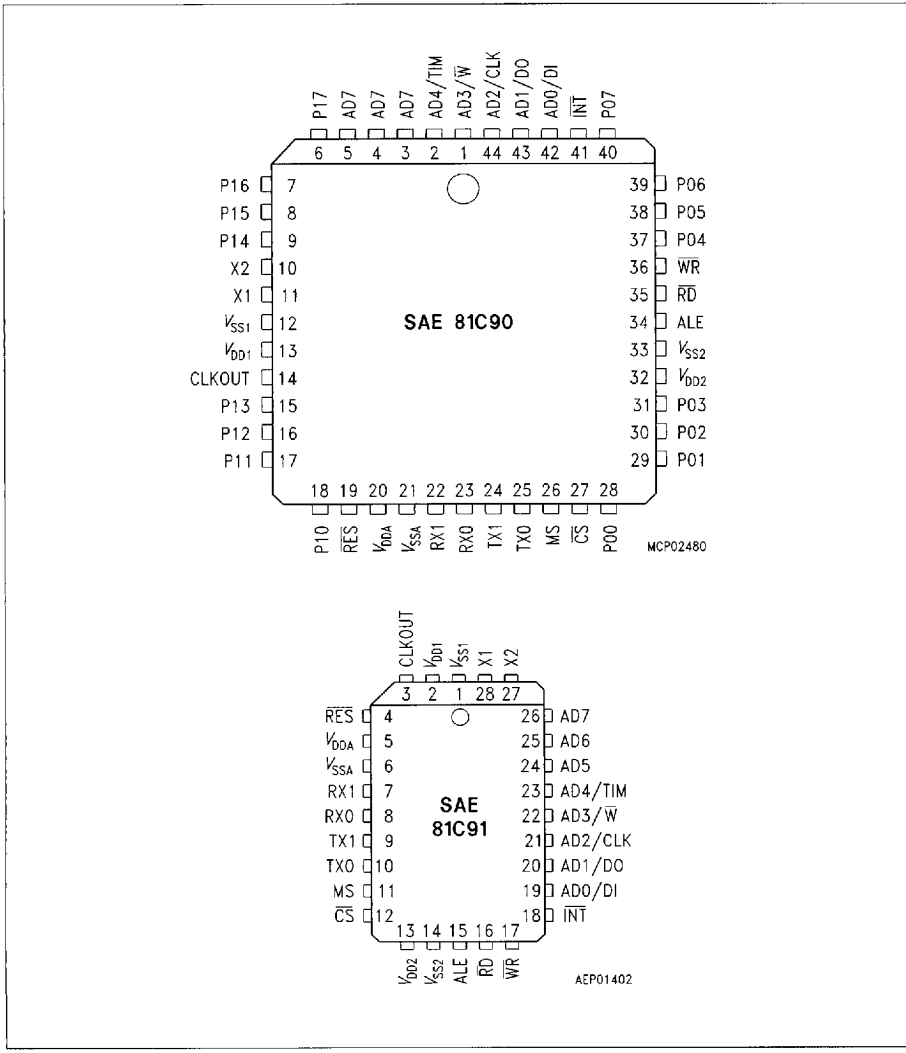


Figure 2

Pin Definitions and Functions

Symbol	Pin Number		Input (I) Output (O)	Function
	P-LCC-48	P-LCC-28		
X1	11	28	I	Crystal oscillator. Must be unconnected for external clock input.
X2	10	27	I	Crystal oscillator. Used for external clock input.
CLKOUT	14	3	O	Clock output
$\overline{RES}$	19	4	I	Reset. (Schmitt trigger characteristic)
AD0/DI	42	19	I/O	PI: Address / Data bus / SI: Data input
AD1/DO	43	20	I/O	PI: Address / Data bus / SI: Data output
AD2/CLK	44	21	I/O	PI: Address / Data bus / SI: Clock input
AD3/$\overline{W}$	1	22	I/O	PI: Address / Data bus / SI: Write select
AD4/TIM	2	23	I/O	PI: Address / Data bus / SI: TIM = 0: Timing A; TIM = 1: Timing B
AD5	3	24	I/O	PI: Address/Data bus
AD6	4	25	I/O	PI: Address/Data bus
AD7	5	26	I/O	PI: Address/Data bus
$\overline{RD}$	35	16	I	PI: Read / SI: no Function
$\overline{WR}$	36	17	I	PI: Write / SI: no Function
ALE	34	15	I	PI: Address Latch Enable / SI:no Function
$\overline{CS}$	27	12	I	Chip Select
$\overline{INT}$	41	18	O	Interrupt
MS	26	11	I	Mode Select (PI ↔ SI)
P00 ... P03, P04 ... P07	28, 29, 30, 31, 37, 38, 39, 40	– –	I/O –	Port 0 These pins provide internal pullup resistors of about 10 ... 200 kΩ.
P10 ... P13, P14 ... P17	18, 17, 16, 15, 9, 8, 7, 6	– –	I/O –	Port 1 These pins provide internal pullup resistors of about 10 ... 200 kΩ.
TX0	25	10	O	Transmitter output 0
TX1	24	9	O	Transmitter output 1
RX0	23	8	I	Comparator input 0 / Digital input [1]
RX1	22	7	I	Comparator input 1 [1]

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		Input (I) Output (O)	Function
	P-LCC-48	P-LCC-28		
V_{DDA}	20	5	I	Analogue power supply for comparator (may be unconnected using the digital mode)
V_{SSA}	21	6	I	Analogue power ground for comparator (must always be connected)
V_{DD1}	13	2	I	Digital power supply
V_{DD2}	32	13	I	Digital power supply
V_{SS1}	12	1	I	Digital power ground
V_{SS2}	33	14	I	Digital power ground

1) If the bus lines work according to the ISO specification, additional circuitry is necessary for Interconnection of the input comparator to the bus lines

Functional Description

The Siemens stand-alone Full-CAN (SFCAN) circuit is a large-scale-integrated peripheral device that executes the entire protocol of an automobile or industrial network.

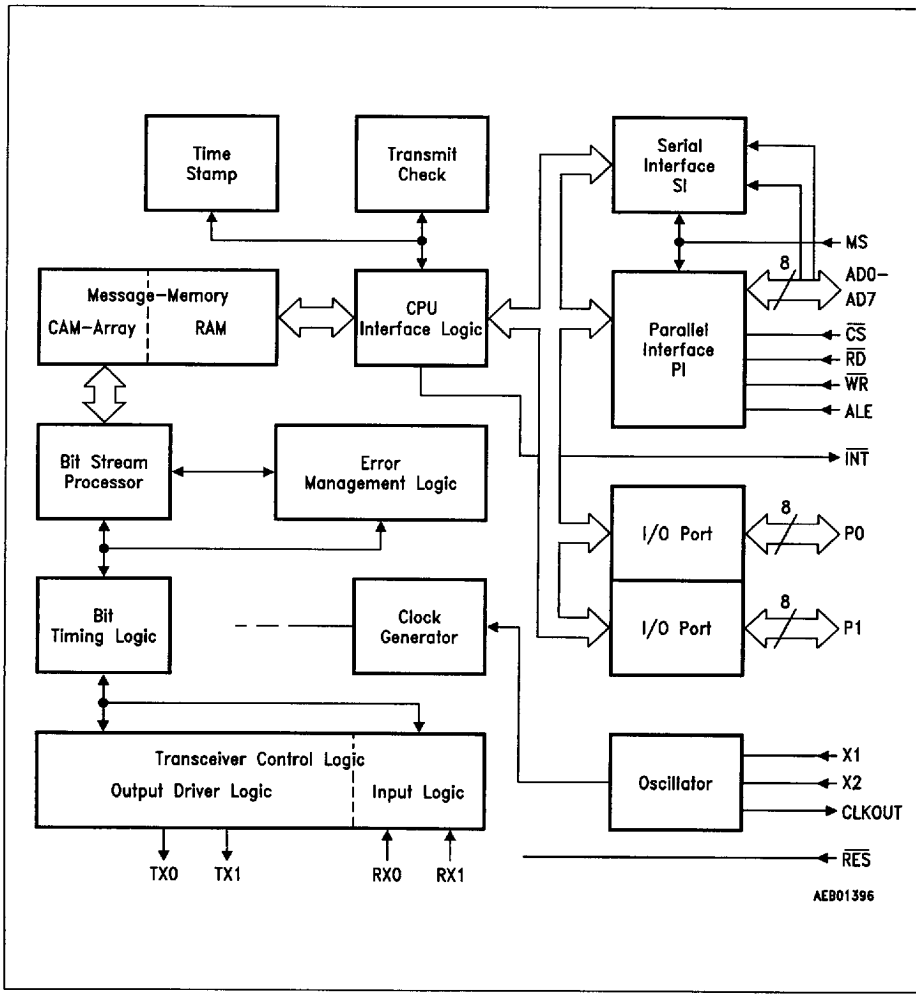


Figure 3
Block Diagram

Bus communication is based on the controller-area-network (CAN) protocol. With features like short message length, guaranteed reaction time for messages of appropriate priority, which is defined by the message identifiers. Also included are powerful error detection and treatment capabilities plus ease of operation. The CAN protocol is especially designed for the requirements of automobile and industrial electronic networks.

The SFCAN circuit incorporates all the parts for completely independent transmission and reception of messages using the CAN protocol. The flexible, programmable interface allows connection to different implementations of the physical layer. The link to a host controller can be made either by a multiplexed 8-bit address/data bus or by a high-speed, serial synchronous interface.

Message Memory

The SFCAN circuit filters incoming messages with an associative memory (CAM = content-addressable memory). For this the identifier and RTR bits of the required message must be written to the appropriate memory location.

The identifier of each incoming message is compared with the identifiers stored in the CAM. Upon a match the received data bytes are written into the RAM buffer of the matching message. At the same time the corresponding receive-ready bit is set and a receive interrupt is generated, if it is enabled. If no match is detected, the received message is rejected.

Identifiers can be reprogrammed at any time, although it is possible that data of the old or new identifier may be lost during reprogramming.

An incoming transmit request will only be satisfied automatically by the hardware if the RTR bit of the particular identifier is set in CAM.

To ensure data consistency when reading or writing several data bytes, these data are buffered in a 64-bit shadow register (see **Figure 4** 'CAM, Message Memory and Time-Stamp Registers' below).

Writing must start with the most-significant data byte. When data byte 0 is written, the contents of the shadow register are transferred in parallel into the RAM of the respective message. For read operations data are transferred into the shadow register automatically by interpreting the address of the byte that is being read. In this way, for example, reading address 83_H ensures that the data of locations 80_H through 87_H go into the shadow register. But transfer is only made if a date of another message has been read out before. Upon reading the highest data byte of a message (e.g. address 87_H) the shadow register is newly loaded in any case.

Note: For these reasons it is absolutely essential to ensure that the writing of data is not interrupted by a read operation and vice versa, a read operation should not be interrupted by a write.

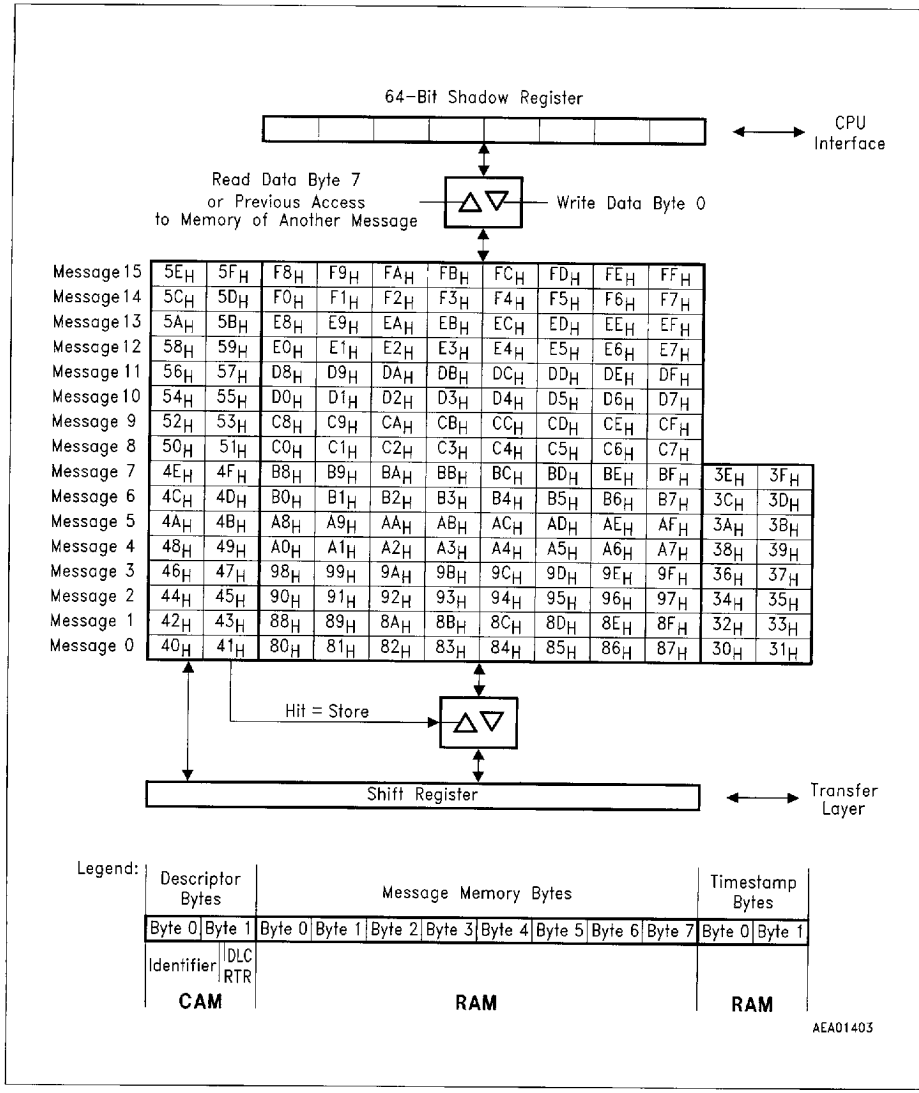


Figure 4
CAM, Message Memory and Time-Stamp Registers

Bit Stream Processor (BSP)

The bit-stream processor controls the entire protocol, differentiates between the frames types and detects frame errors.

Error Management Logic (EML)

The error-management logic receives error messages from the BSP and, in turn, sends back information about error state to the BSP and CIL.

Bit Timing Logic (BTL)

The bit-timing logic determines the timing of the bits and synchronizes with the edges of the bit stream on the CAN bus.

Transceiver Control Logic (TCL)

The transceiver-control logic consists of programmable output driver, input comparator and input multiplexer.

Clock Generator (CG)

The clock generator consists of an oscillator and a programmable divider. The oscillator can be fed from an external quartz crystal, ceramic resonator or an external timing source. The permissible crystal frequency is 1 to 20 MHz, and the external clock may be between 0 and 20 MHz. A programmable frequency, dependent on the crystal clock, is available with the CLKOUT pin, e.g. for the clocking of a host controller.

CPU Interface Logic (CIL)

The CPU interface logic controls the access of the host via the parallel or serial interface, interprets the commands and outputs status and interrupt information.

Transmit Check

The CAN protocol ensures a very high integrity for the data transferred over the bus. The on-chip path from the data stored in parallel to the serial bit stream is not protected by the protocol. To eliminate any possible uncertainties at this point too, the SFCAN circuit incorporates a transmit-check unit. This unit reads back a transmitted message via the normal receive path from the bus interface and compares the data with those written into the message memory by the host controller. If any inconsistency of the data is detected, the current message will be invalidated by an error frame.

The transmit-check error counter TCEC is then incremented by 1. If this counter reaches 4 an error interrupt (bit TCI in the INT register) is generated, provided that this has not been masked (bit ETCI in the IMSK register). This count will also produce the Bus Off status.

The TCEC is set to 0 after a reset and can be read and also written for test purposes at any time.

Note: The transmit-check is an additional feature of the Siemens Full CAN Chip and is not part of the CAN protocol.

Time Stamp

It is impossible to determine from the received data in the message memory when they were received. So the host controller is unable to derive any information about the actuality or the repetition rate of the data.

To enable an indication of the time of reception for at least some of the messages, a 16-bit timer is implemented on the SFCAN circuit. The content of this gets written into the time-stamp registers of the particular message when it is received (for the messages 0 through 7). There are two time-stamp bytes for each of the messages 0 through 7, and these hold the value of the 16-bit timer.

The actuality of a message is determined by subtracting the old time-stamp of a message, stored in the host controller, from the new one, with respect to the timer overflow bit.

Overflow of the timer can be detected by bit TSOV in the CTRL register. This bit does not trigger an interrupt and has to be reset by the host controller. Depending on the setting of bits TSP0 and TSP1 in the CTRL register, the counter is fed with 1/32, 1/64, 1/128 or 1/256 of the bus clock. The momentary timer status can be read and set at any time. The timer starts at 0 after a reset and cannot be stopped.

I/O-Ports

There are two parallel I/O ports in the SAE 81C90, each with eight pins. These ports are configured pin by pin as input or output, depending on the contents of the port-direction register.

The output data for the port pins can be written (latched) into the port-latch register. Reading this register reproduces the contents of the latch. The levels on the port pins can be read from the port-pin register.

For the SAE 81C91 in its P-LCC-28-1 package, the pads of the I/O ports are not bonded and therefore unavailable to the user.

Control Registers

The SFCAN circuit is controlled by registers. These can be accessed by the addresses listed below. If not otherwise noted in the detailed description they are readable and writable.

Address Assignments: Control Registers

Register Name	Address	Function	Reset Value	Read Write [1]
BL1	00_H	Bit-length register 1	00_H	r/w,l
BL2	01_H	Bit-length register 2	00_H	r/w,l
OC	02_H	Output-control register	00_H	r/w,l
BRP	03_H	Baud-rate prescaler	00_H	wo,l
RR1	04_H	Receive-ready register 1	00_H	r/w
RR2	05_H	Receive-ready register 2	00_H	r/w
RIM1	06_H	Receive-interrupt-mask register 1	00_H	r/w
RIM2	07_H	Receive-interrupt-mask register 2	00_H	r/w
TRS1	08_H	Transmit-request-set register 1	00_H	r/w
TRS2	09_H	Transmit-request-set register 2	00_H	r/w
IMSK	$0A_H$	Interrupt-mask register	00_H	r/w
MOD	10_H	Mode/status register	00_H	r/w
INT	11_H	Interrupt register	00_H	r/w
CTRL	12_H	Control register	00_H	r/w
CC	14_H	Clock-control register	01_H	wo
TCEC	15_H	Transmit-check error counter	00_H	r/w
TCD	16_H	Transmit-check data register	XX	ro
TRR1	18_H	Transmit-request-reset register 1	00_H	wo
TRR2	19_H	Transmit-request-reset register 2	00_H	wo
RRP1	$1A_H$	Remote-request-pending register 1	00_H	ro
RRP2	$1B_H$	Remote-request-pending register 2	00_H	ro
TSCH	$1C_H$	Time-Stamp counter high byte	00_H	r/w
TSCL	$1D_H$	Time-Stamp counter low byte	00_H	r/w
P0PDR	28_H	Port 0 port-direction register	00_H	r/w
P0PR	29_H	Port 0 pin register	00_H	ro
P0LR	$2A_H$	Port 0 latch register	00_H	r/w
P1PDR	$2C_H$	Port 1 port-direction register	00_H	r/w
P1PR	$2D_H$	Port 1 pin register	00_H	ro
P1LR	$2E_H$	Port 1 latch register	00_H	r/w

[1] ro: readonly, r/w read and write access, l: access only with bit IM set, wo: write only

Addresses not listed above are not available and must not be written in initialization mode.

Message-Memory Layout

Time Stamp registers

Address	Function	
30_H	High Byte	Time-Stamp 0
31_H	Low Byte	
32_H	High Byte	Time-Stamp 1
33_H	Low Byte	
:	:	:
$3C_H$	High Byte	Time-Stamp 6
$3D_H$	Low Byte	
$3E_H$	High Byte	Time-Stamp 7
$3F_H$	Low Byte	

Descriptor Registers

Address	Function	
40_H	Byte 0	Descriptor 0
41_H	Byte 1	
42_H	Byte 0	Descriptor 1
43_H	Byte 1	
:	:	:
$5C_H$	Byte 0	Descriptor 14
$5D_H$	Byte 1	
$5E_H$	Byte 0	Descriptor 15
$5F_H$	Byte 1	

Data Registers

Address	Function	
80_H	Byte 0	Message 0
81_H	Byte 1	
82_H	Byte 2	
83_H	Byte 3	
84_H	Byte 4	
85_H	Byte 5	
86_H	Byte 6	
87_H	Byte 7	
88_H	Byte 0	Message 1
89_H	Byte 1	
$8A_H$	Byte 2	
$8B_H$	Byte 3	
$8C_H$	Byte 4	
$8D_H$	Byte 5	
$8E_H$	Byte 6	
$8F_H$	Byte 7	
:	: :	
$F8_H$	Byte 0	Message 15
$F9_H$	Byte 1	
FA_H	Byte 2	
FB_H	Byte 3	
FC_H	Byte 4	
FD_H	Byte 5	
FE_H	Byte 6	
FF_H	Byte 7	

Descriptor Registers

7	6	5	4	3	2	1	0
ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3

7	6	5	4	3	2	1	0
ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0

These two registers contain the eleven bits of the message identifier (ID.0 through ID.10), the remote-transmission-request bit (RTR) and the data length code (DLC.0 through DLC.3) of a message.

Note: Bitfield DLC allows data length codes of 0...8 bytes (DLC=0000...1000). All other bit combinations are not permitted.
For the transmission of remote frames (RTR = 1) the data-length-code must be set like the DLC-bits of the corresponding data frame.

Time-Stamp Registers

7	6	5	4	3	2	1	0
TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8

7	6	5	4	3	2	1	0
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

The two registers contain the time-stamp of the corresponding message. Both registers can only be read.

Mode/Status-Register MOD

7	6	5	4	3	2	1	0
ADE	**RS**	**TC**	**TWL**	**RWL**	**BS**	**RES**	**IM**

The register can be read and written except otherwise noted; the reset value is 00_H.

Symbol	Function
IM	**Init Mode** IM = 1: Setting this bit to 1 enables the initialization mode: write access to the configuration registers BL1, BL2, OC, BRP is enabled. If the bit stays set, the chip enters the normal mode, with enabled access to the configuration registers. If this bit is set in conjunction with bit RES a hard software reset is activated. IM = 0: Normal mode.
RES	**Reset Request** RES = 1: The chip enters the reset state: – if bit IM = 0 a soft reset takes place. – if bit IM = 1 a hard reset takes place further details see below. RES = 0: Normal mode.
BS	**Bus State (read only)** BS = 1: Bus Off state, the IC does not participate in bus activities. BS = 0: Normal mode.
RWL	**Receiver Warning Level (read only)** RWL = 1: Receive-error counter larger or equal 96. RWL = 0: Receive-error counter smaller 96.
TWL	**Transmit Warning Level (read only)** TWL = 1: Transmit-error counter larger or equal 96. TWL = 0: Transmit-error counter smaller 96.
TC	**Transmission Complete (read only)** TC = 1: The last transmission request was executed successfully. TC = 0: The last transmission request is not yet executed successfully.
RS	**Receive State (read only)** RS = 1: Currently the SAE81C90/91 is in receive mode. RS = 0: No receive.
ADE	**Auto Decrement Enable** ADE = 1: With every read or write access using the serial synchronous interface SI the address is decremented by one automatically. So one can access data continuously without the need of writing a new address. ADE = 0: No automatic address decrement.

Notes on Bit TC

Scanning this bit is particularly useful if only one transmission is active. If there are several transmission jobs at the same time, it is better to scan the transmit-request register, because bit TC may possibly only be set very briefly between acknowledgment of the previous message and the start of the next one.

Notes on Bit RES and IM and reset modes

There are three different reset modes implemented in the SAE 81C90/91:

hardware reset (activated by low level on pin $\overline{\text{RES}}$)

hard software reset (activated by setting both bits RES and IM to 1)

soft software reset (activated by setting bit RES to 1 and bit IM to 0)

The only difference between hardware and hard software reset affect bits RES and IM, that are not changed by software reset.

With soft software reset the registers RR1, RR2, TRS1, TRS2, RRP1 and RRP2 are set to 0, all busactivities are stopped, the error counters are not set to 0, the Bus Off state is cancelled only after 128 idle phases (according to the CAN protocol 1 idle phase = 11 recessive bits in sequence). Simply spoken a soft software reset interrupts and cancels all bus activities and - if necessary - recovers from Bus Off state.

Notes on Bit RS

Bit RS directly reflects the internal status.
RS is '0' during transmission or when the SAE 81C90/91 is idle.
RS is '1' during reception or during the synchronization after a reset (duration: 1 idle phase).

Control Register CTRL

7	6	5	4	3	2	1	0
RX	**TST**	**TSP1**	**TSP0**	**TSOV**	**SME**	**TCE**	**MM**

The register can be read and written; the reset value is 00_H.

Symbol	Function
MM	**Monitor Mode** MM = 1: The memory location of message 0 receives all identifiers that are not accepted by other memory locations (corresponds to a Basic CAN receive register). MM = 0: The above memory location responds like all others.
TCE	**Transmit Check Enable** TCE = 1: If the transmit check detects an error, the message is invalidated by an error frame and the error counter TCEC is incremented by 1. If the counter reaches 4, the Bus Off status is initiated and, if enabled, an interrupt (TCI) is generated. TCE = 0: If the transmit check detects an error, there is no intervention.
SME	**Sleep Mode Enable** SME = 1: The sleep mode is enabled: the crystal oscillator is deactivated, all other activities are inhibited. The wake up is done by a reset signal or by an active signal at the $\overline{CS}$ pin or by an input edge going from recessive to dominant at pin Rx0 or Rx1. SME = 0: Normal operation.
TSOV	**Time Stamp Overflow** TSOV = 1:There was at least one overflow of the time-stamp timer. TSOV = 0:There has been no overflow.
TSP0 **TSP1**	**Time Stamp Prescaler** TSP1 TSP0 Clock of time-stamp timer 0 0 f_{BL} / 32 0 1 f_{BL} / 64 1 0 f_{BL} / 128 1 1 f_{BL} / 256 (For f_{BL} see baud-rate prescaler BRP).
TST	**Time Stamp Test** TST = 1: The time-stamp prescaler is deactivated. Only for test, bit IM (MOD.0) must be set to 1. TST = 0: The prescaler is activated.
RX	**Input Monitor RX** This bit monitors the actual state of the digital input pin RX0.

Interrupt Register INT

7	6	5	4	3	2	1	0
TCI	EPI	BOI	WUPI	RFI	WLI	TI	RI

Register bits can be reset by writing 0 to the respective bit, writing 1 has no effect.

Symbol	Function
RI	**Receive Interrupt** After a valid message has been received and filed, this bit is set and an interrupt generated. This bit will remain set until all bits of the registers RR1 and RR2 are reset.
TI	**Transmit Interrupt** This bit is set and an interrupt generated as soon as a transmit request has been processed.
WLI	**Warning Level Interrupt** If at least one of the two error counters is greater than or equals 96, this bit is set and an interrupt generated.
RFI	**Remote Frame Interrupt** This interrupt is generated after reception of a remote frame.
WUPI	**Wake Up Interrupt** After a wake-up this bit is set and an interrupt generated.
BOI	**Bus Off Interrupt** This bit is set and an interrupt generated when the Bus Off status is entered.
EPI	**Error Passive Interrupt** If at least one of the two error counters is greater than or equals 128, this bit is set and an interrupt generated.
TCI	**Transmit Check Interrupt** If the transmit-check error counter reaches 4, this bit is set and an interrupt generated.

All bits of this register must be reset by software.

Note: An interrupt is only generated, if the respective IMSK bit is set. The bits in this register are set independent of the IMSK-Register.

Bit-Length Register 1 BL1

7	6	5	4	3	2	1	0
SAM	**TS2.2**	**TS2.1**	**TS2.0**	**TS1.3**	**TS1.2**	**TS1.1**	**TS1.0**

The register can always be read but only written when bit IM (MOD.0) is set; the reset value is 00_H.

Symbol	Function
TS1.3 - TS1.0	**Length of segment 1** (TSEG1). TSEG1 = (TS1 + 1) × t_{SCL}
TS2.2 - TS2.0	**Length of segment 2** (TSEG2). TSEG2 = (TS2 + 1) × t_{SCL}
SAM	**Sample Rate** SAM = 1: Input signal is sampled three times per bit. SAM = 0: Input signal is sampled once per bit. Note: Bit SAM should only be set to 1 using very low baud rates.

For t_{SCL} see baud-rate prescaler BRP.

Bit-Length Register 2 BL2

7	6	5	4	3	2	1	0
IPOL	**DI**	–	–	–	**SM**	**SJW.1**	**SJW.0**

The register can always be read but only written when bit IM (MOD.0) is set; the reset value is 00_H.

Symbol	Function
SJW.1 - SJW.0	**Maximum Synchronization Jump Width.** SJWidth = (SJW + 1) × t_{SCL}
SM	**Speed Mode** Determines which edges are used for synchronization. SM = 1: Both edges are used. SM = 0: Recessive to dominant is used. Note: According to the CAN specification this bit should not be set to 1.
–	**Reserved**, must be 0 (read value is not defined when IM is set).
–	**Reserved**, must be 0 (read value is not defined when IM is set).
–	**Reserved**, must be 0 (read value is not defined when IM is set).
DI	**Digital Input** DI = 1: The input signal on pin RX0 is evaluated digitally. The input comparator is inactive. Pin RX1 should be on V_{SS} DI = 0: The input signal is applied to the input comparator.
IPOL	**Input Polarity** IPOL = 1: The input level is inverted. IPOL = 0: The input level remains unaltered.

For t_{SCL} see baud-rate prescaler BRP.

Interrupt-Mask Register IMSK

7	6	5	4	3	2	1	0
ETCI	EEPI	EBOI	EWUPI	ERFI	EWLI	ETI	ERI

The register can be read and written; the reset value is 00_H.

Symbol	Function
ERI	**Enable Receive Interrupt** ERI = 1: Receive interrupts are enabled. ERI = 0: No receive interrupt enabled.
ETI	**Enable Transmit Interrupt** ETI = 1: Completed transmit jobs generate interrupts. ETI = 0: No transmit interrupt enabled.
EWLI	**Enable Warning Level Interrupt** EWLI = 1: There is an interrupt when the warning level is reached. EWLI = 0: No warning level interrupt enabled.
ERFI	**Enable Remote Frame Interrupt** ERFI = 1: A receive interrupt is generated after receiving a remote frame. ERFI = 0: No remote frame interrupt enabled.
EWUPI	**Enable Wake Up Interrupt** EWUPI = 1: Wake-up is enabled as interrupt. EWUPI = 0: No wake up interrupt enabled.
EBOI	**Enable Bus Off Interrupt** EBOI = 1: Bus off is enabled as interrupt. EBOI = 0: No bus off interrupt enabled.
EEPI	**Enable Error Passive Interrupt** EEPI = 1: Error passive is enabled as interrupt. EEPI = 0: No error passive interrupt enabled.
ETCI	**Enable Transmit Check Error Interrupt** ETCI = 1: Transmit-check error is enabled as interrupt. ETCI = 0: No transmit check interrupt enabled.

Note: The above bits determine if an event activates the INT pin. They don't influence the INT register.

Baud Rate Prescaler BRP

7	6	5	4	3	2	1	0
–	–	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0

The register is not readable and can only be written when bit IM (MOD.0) is set.
The reset value is 00_H.

Symbol	Function
BRP5 - BRP0	**Baud Rate Prescaler** This register determines the system clock. $t_{SCL} = (BRP + 1) \times 2t_{OSC}$
–	**Reserved**, must be 0
–	**Reserved**, must be 0

$t_{OSC} = 1 / f_{crystal}$

The bit length t_{BL} is computed as follows:

$t_{BL} = T_{SEG1} + T_{SEG2} + 1\ t_{SCL}$

The baudrate BR is:

$BR = f_{crystal} / (2 \times (BRP + 1) \times (TS1 + TS2 + 3))$

Note: BRP = BRP0...BRP5 see Baud Rate Prescaler
TS1 = TS1.0...TS1.3 see Bit Length Register 1
TS2 = TS2.0...TS2.2 see Bit Length Register 1

Output-Control Register OC

7	6	5	4	3	2	1	0
OCTP.1	OCTN.1	OCP.1	OCTP.0	OCTN.0	OCP.0	OCM.1	OCM.0

The register can always be read but only written when bit IM (MOD.0) is set; the reset value is 00_H.

Output Modes

OCM.1	OCM.0	Output Mode
0	X	**Normal Mode**: TX0 = Bit Sequence, TX1 = Bit Sequence
1	0	**Test Mode**: TX0 = Bit Sequence, TX1 = RX0
1	1	**Clock Mode**: TX0 = Bit Sequence, TX1 = Bit Clock

Output Programming

OCTP.x	OCTN.x	OCP.x	Data	TxP	TxN	TXx-Level
0	0	0	0 = dominant	OFF	OFF	float
0	0	0	1 = recessive	OFF	OFF	float
0	0	1	0	OFF	OFF	float
0	0	1	1	OFF	OFF	float
0	1	0	0	OFF	ON	LOW
0	1	0	1	OFF	OFF	float
0	1	1	0	OFF	OFF	float
0	1	1	1	OFF	ON	LOW
1	0	0	0	OFF	OFF	float
1	0	0	1	ON	OFF	HIGH
1	0	1	0	ON	OFF	HIGH
1	0	1	1	OFF	OFF	float
1	1	0	0	OFF	ON	LOW
1	1	0	1	ON	OFF	HIGH
1	1	1	0	ON	OFF	HIGH
1	1	1	1	OFF	ON	LOW

TxP is the output transistor switching to V_{DD}, TxN switches to V_{SS}.
TXx is the output level at the transmit pin.

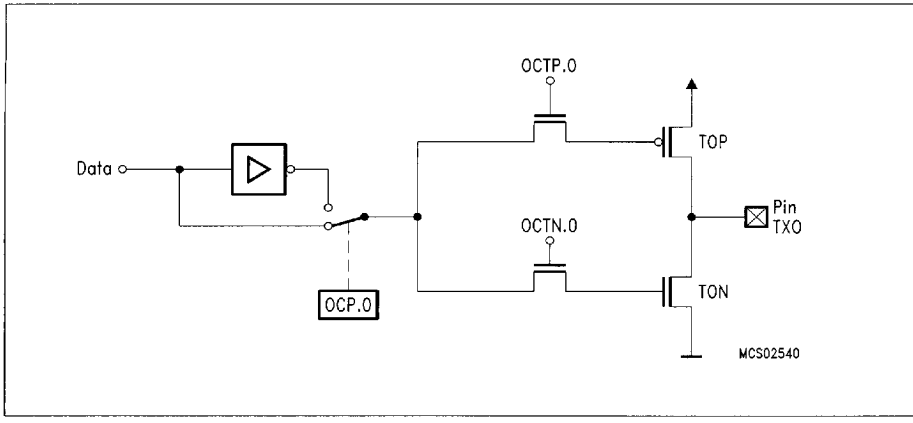


Figure 5
Output Control Circuitry

Receive-Ready Registers RR1 and RR2

7	6	5	4	3	2	1	0
RR7	**RR6**	**RR5**	**RR4**	**RR3**	**RR2**	**RR1**	**RR0**

7	6	5	4	3	2	1	0
RR15	**RR14**	**RR13**	**RR12**	**RR11**	**RR10**	**RR9**	**RR8**

The register bits can be reset by writing 0 to the respective bit, writing 1 has no effect; the reset value is 00_H. Bit RRx is set when a message has arrived and been written into the memory location of message x. Setting this bit by hardware can generate a receive interrupt, which can be blocked by bit RIMx in the receive-interrupt-mask register.
Bits RRx must be reset by software.

Receive-Interrupt-Mask Registers RIM1 and RIM2

7	6	5	4	3	2	1	0
RIM7	RIM6	RIM5	RIM4	RIM3	RIM2	RIM1	RIM0

7	6	5	4	3	2	1	0
RIM15	RIM14	RIM13	RIM12	RIM11	RIM10	RIM9	RIM8

These registers can be read and written; the reset value is 00_H.

Setting bit RIMx enables a receive interrupt to be generated if the receive-ready bit RRx has been set, i.e. a message has arrived and was written into the memory location of message x.

Bit ERI in the interrupt-mask register IM blocks all receive interrupts, even if bits RIMx are set.

Transmit-Request Registers TR1 and TR2

The transmit-request registers are each divided in the addresses for setting and resetting of the transmission request. In this manner it is prevented that when writing these registers bits become set again which meanwhile were reset because of a completed transmission.

Transmit-Request-Set Registers TRS1 and TRS2

7	6	5	4	3	2	1	0
TRS7	TRS6	TRS5	TRS4	TRS3	TRS2	TRS1	TRS0

7	6	5	4	3	2	1	0
TRS15	TRS14	TRS13	TRS12	TRS11	TRS10	TRS9	TRS8

These registers can be read. Writing 1 to a bit takes effect, writing 0 has no effect; the reset value is 00_H.

Setting bit TRx causes the particular message x to be transmitted. The bit is reset by hardware after transmission. Several bits can be set simultaneously. In this way all messages whose request bits are set are transmitted in turn, starting with the memory location with the highest number.

Transmit-Request-Reset Registers TRR1 and TRR2

7	6	5	4	3	2	1	0
TRR7	TRR6	TRR5	TRR4	TRR3	TRR2	TRR1	TRR0

7	6	5	4	3	2	1	0
TRR15	TRR14	TRR13	TRR12	TRR11	TRR10	TRR9	TRR8

These registers can not be read and only writing 1 to a bit takes effect.

Setting bit TRRx causes a transmission request, initiated by the corresponding bit TRSx, to be cancelled, provided that it is not currently processed. Bit TRSx is set to 0 by this action.

Remote-Request-Pending Register RRP1

7	6	5	4	3	2	1	0
RRP7	RRP6	RRP5	RRP4	RRP3	RRP2	RRP1	RRP0

Remote-Request-Pending Register RRP2

7	6	5	4	3	2	1	0
RRP15	RRP14	RRP13	RRP12	RRP11	RRP10	RRP9	RRP8

These registers can only be read; the reset value 00_H.

If bit RRPx by is set a remote frame was received for the particular message x, and is not yet answered by the transmission of the corresponding message.

Port-Latch Registers P0LR and P1LR

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Port-Pin Registers P0PR and P1PR

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Port-Direction Registers P0PDR and P1PDR

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Except for the port-pin registers which can only be read all registers can be read and written; the reset value of the port registers is 00_H.

After a reset, the ports are switched as inputs. The state of the pin can be read via the port register. Setting a bit of the port-direction register to 1 causes the associated port pin to be switched as an output. The output data can then be written (latched) into the port register. The latch can be read from the port-latch register, the levels on the port pins from the port-pin register.

In parallel to the standard CMOS structure there is an additional internal pull up resistor of about 10 ... 200 kΩ at each port pin.

Clock-Control Register CC

7	6	5	4	3	2	1	0
–	–	–	–	CC3	CC2	CC1	CC0

This register can only be written (special procedure see below); the reset value is 01_H.

The clock control register determines the output frequency at pin CLK.

CC3	CC2	CC1	CC0	Output frequency
0	0	0	0	f_{osc}
0	0	0	1	$f_{osc}/2$
0	0	1	0	$f_{osc}/4$
0	0	1	1	$f_{osc}/6$
0	1	0	0	$f_{osc}/8$
0	1	0	1	$f_{osc}/10$
0	1	1	0	$f_{osc}/12$
0	1	1	1	$f_{osc}/14$
1	X	X	X	switched off (Low level)

Bits 4 through 7 must be 0 except for the case described below:

Writing to this register requires a special protocol in order to avoid erroneous writing:

- Step 1: Write 80_H to CC
- Step 2: Write desired value to CC

Transmit-Check Error Counter TCEC

7	6	5	4	3	2	1	0
–	–	–	–	–	TCEC2	TCEC1	TCEC0

This register can be read and written; the reset value is 00_H.

This register counts the errors detected by the transmit check. When a count of 4 is reached (TCEC2 = 1) an interrupt is generated if enabled. Furthermore if bit TCE (CTRL.1) is set to 1 the Bus Off status is initiated.

Bits 3 through 7 must be 0.

Transmit-Check Data Register TCD

7	6	5	4	3	2	1	0

This register can only be read; the reset value is undefined.

This register, when a transmit-check error appears, contains the data byte that led to the error. By reading the contents of the register one can see which byte was actually being sent. This way an error analysis can be attempted.

Time-Stamp Counter TSCL and TSCH

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8

Via these registers the time-stamp counter can be read and written, the reset value is 00_H.

Bit Timing

A regular bit period is composed of the following three segments:

- synchronization segment
- timing segment 1
- timing segment 2.

The sampling point is between timing segment 1 and timing segment 2.

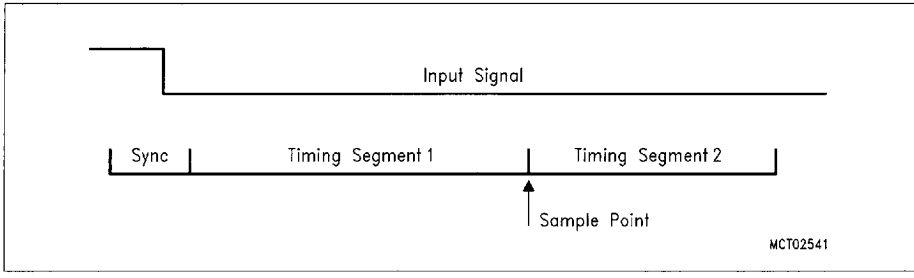


Figure 6
Bit Time Segments

Synchronization

The edge of the input signal is expected during the sync segment (duration = 1 system clock cycle = 1 t_{SCL}).

Timing Segment 1

Timing segment 1 determines the sampling point within a bit period. This point is always at the end of segment 1. The segment is programmable from 1 to 16 t_{SCL} (see bit-length register BL1).

Timing Segment 2

Timing segment 2 provides extra time for internal processing after the sampling point. The segment is programmable from 1 to 8 t_{SCL} (see bit-length register BL1).

Synchronization Jump Width

To compensate for phase shifts between the oscillator frequencies of the different bus stations, each CAN controller must be able to synchronize to the relevant signal edge of the incoming signal. The synchronization jump width (SJW) determines the maximum number of system clock pulses by which the bit period can be lengthened or shortened for resynchronization. The synchronization jump width is programmable from 1 to 4 t_{SCL} (see bit-length register BL2).

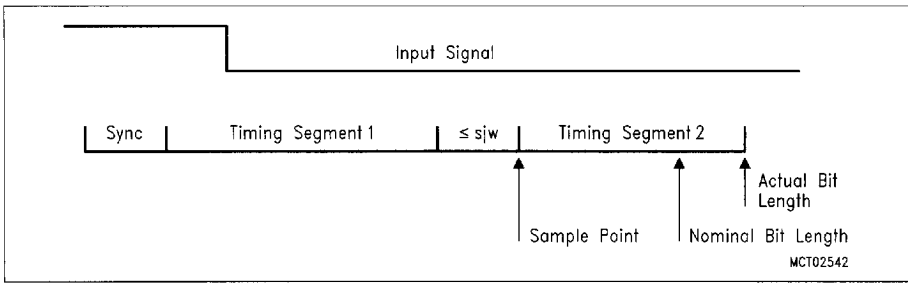


Figure 7
Lengthening a Bit Period

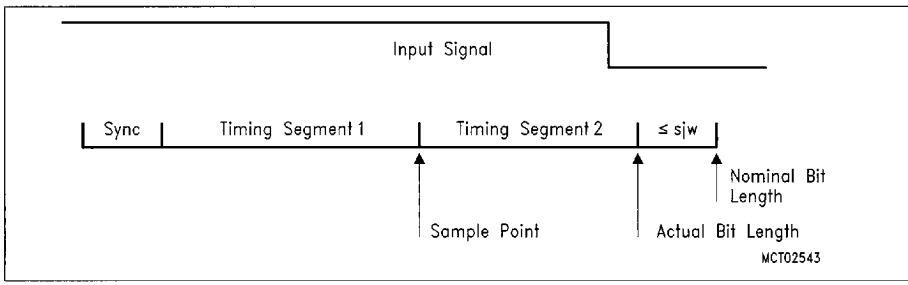


Figure 8
Shortening a Bit Period

Delay Times

The total delay is calculated from the following single delays:

- 2 × physical bus t_{Bus} (max. 100 ns acc. to CAN specification)
- 2 × input comparator t_{Comp} (depends on application circuit)
- 2 × output driver t_{Driver} (depends on application circuit)
- 1 × input to output of CAN controller t_{InOut} (max. 1 t_{SCL} + 80 ns)

$$t_{Delay} = 2 \times (t_{Bus} + t_{Comp} + t_{Driver}) + t_{InOut}$$

Recommendations

On the premise of the stated conditions, there are the following essential requirements to be maintained:

$t_{TSEG1} \geq t_{SEG2}$
$t_{TSEG1} \geq t_{Delay}$
$t_{TSEG2} > t_{SJW}$
$t_{TSEG2} \geq 3 \times t_{SCL} + SJW$ if bit SAM = 1.

Host Interfaces

There are two different host interfaces implemented in the SAE 81C90/91.

Data and addresses on a multiplexed 8-bit bus, compatible with Siemens microcontrollers (C5xx, C16x), can be transferred via the parallel interface (PI). Using the serial synchronous interface (SI), any host controller with a serial three-lead interface can be connected with.

The interface is selected by hardware through the wiring of the MS (Mode Select) pin. This pin may not be switched during operation. If there is a High level on the MS pin, the SI and thus pins DI, DO, CLK, $\overline{W}$ and TIM are activated, while pins AD5 through AD7, $\overline{RD}$, $\overline{WR}$ and ALE are inactive. A Low level on the MS pin switches to the PI and thus activates pins AD0 through AD7, $\overline{RD}$, $\overline{WR}$ and ALE.

Parallel Interface PI

The parallel interface uses a multiplexed 8-bit address/data bus. First the address of the required register is applied to the pins AD0 through AD7. A falling edge on pin ALE means that this address is transferred to an on-chip latch. After this, data can either be written into the selected register (pin $\overline{WR}$ = 0) or read from it (pin $\overline{RD}$ = 0) via the address/data bus. Pin $\overline{CS}$ must be 0 for the entire duration of the $\overline{RD}$/$\overline{WR}$ active time so that the circuit is activated.

Serial Synchronous Interface SI

If the SI is used the unused pins of PI must be set to inactive levels ($\overline{RD}$, $\overline{WR}$ to V_{DD} and ALE, AD5, AD6, AD7 to V_{SS}).

Communication on the SI is accomplished according to the following procedure:

Each access to the stand-alone Full-CAN circuit has to be started by activating the device ($\overline{CS}$ = 0). After the beginning of access, an address must be written first and then data can be read or written. The required function is determined by pin $\overline{W}$ ($\overline{W}$ = 1: read; $\overline{W}$ = 0: write). If the automatic decrementing of the address is activated (bit ADE in the MOD register), any number of data bytes can be accessed in succession. Finally the device has to be deactivated.

Procedure:

- Activate device ($\overline{CS}$ = 0)
- Set pin $\overline{W}$ to 1 for read, to 0 for write
- Write in address of first data byte
- Read out/write in one or more data bytes
- Deactivate device ($\overline{CS}$ = 1)

The most-significant bit is always output as the first bit of an address or a data byte.
Data from pin DI are transferred into the internal shift register with the **rising** edge of the clock. The active clock edge of pin DO is selectable via the pin TIM. If this pin is 0 the data are output from the shift register to pin DO with the **rising** clock edge (Timing A). If the pin TIM is 1, the output of data is done with the **falling** edge (Timing B).

The timing for reading and writing of two data bytes with automatic decrementing activated is illustrated below.

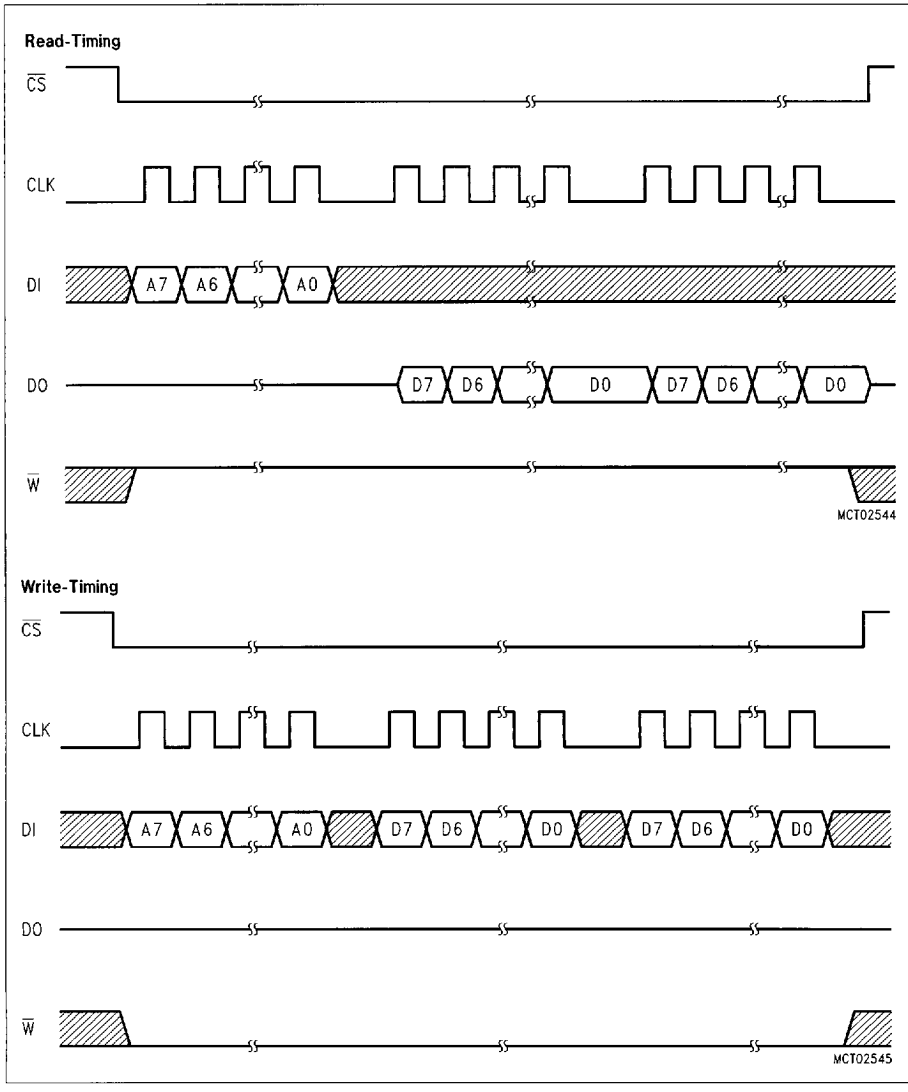


Figure 9
Serial Interface Timing (for 2 Data Bytes)

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	– 40 to + 110 °C
Storage temperature (T_{ST})	– 50 to + 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 to + 6.0 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to V_{CC} + 0.5 V
Input current on any pin during overload condition	– 10 to + 10 mA
Absolute sum of all input currents during overload condition	|100 mA|
Power dissipation	0.5 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the SAE 81C90/91 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column "Symbol":

DC (**D**evice **C**haracteristics):
The logic of the SAE 81C90/91 will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the SAE 81C90/91.

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = – 40 to + 110 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (all except XTAL1 and XTAL2)	V_{IL} SR	0	0.3 V_{CC}	V	–
Input low voltage (XTAL1 and XTAL2)	V_{ILX} SR	0	0.5	V	–
Input high voltage (all except XTAL1 and XTAL2)	V_{IH} SR	0.7 V_{CC}	V_{CC}	V	–
Input high voltage (XTAL1 and XTAL2)	V_{IHX} SR	V_{CC} – 1.0	V_{CC}	V	–
Comparator input voltage	V_{CI} SR	0.5	V_{CC} + 0.5	V	–
Common mode voltage [1]	V_{ICOM} SR	1.5	V_{CC} – 1.5	V	–
Hysteresis [1]	V_{HYS} DC	–	100 [2]	mV	–
Offset voltage [1]	V_{OFF} DC	–	100 [2]	mV	–
Output low voltage (all except CLKOUT, TX0, TX1)	V_{OL} DC	–	0.2 V_{CC}	V	I_{OL} = 1.6 mA
Output low voltage (CLKOUT)	V_{OLC} DC	–	0.4	V	I_{OL1} = 10 mA
Output high voltage (all except CLKOUT, TX0, TX1)	V_{OH} DC	0.8 V_{CC}	V_{CC}	V	I_{OH} = – 1.6 mA
Output high voltage (CLKOUT)	V_{OHC} DC	V_{CC} – 0.8	V_{CC}	V	I_{OH} = – 10 mA
Input leakage current	I_I DC	–	± 1	µA	0 V < V_{IN} < V_{CC} [3]
Source output current (TX0, TX1)	I_{SRC} DC	5	–	mA	V_O = V_{CC} – 1 V
Sink output current (TX0, TX1)	I_{SNK} DC	5	–	mA	V_O = 1 V
Low end capacitance [4]	C_L DC	27	47	pF	
Pin capacitance [1]	C_I DC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current	I_{CC}	–	30	mA	

Notes

1) Not 100 % tested, guaranteed by design characterization.

2) This value is a typical value!

3) This specification does not apply to the port pins (P00 ... P07, P10 ...P17) due to the implemented pullups!

4) In oscillator mode the size of the low-end capacitance must correspond to the specification of the crystal manufacturer.

AC Characteristics (General Timing)
V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = – 40 to + 110 °C

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Oscillator period	t_{OSC}	SR	50	–	ns	
Clock input high time	t_H	SR	23.5	–	ns	
Clock input low time	t_L	SR	23.5	–	ns	
Reset pulse width	t_{RES}	SR	2	–	t_{OSC}	
Output rise time [1]	t_{QR}	DC	–	40	ns	C_L = 70 pF
Output fall time [1]	t_{QF}	DC	–	40	ns	C_L = 70 pF
CLKOUT rise time [1]	t_{QRC}	DC	–	20	ns	C_L = 50 pF
CLKOUT fall time [1]	t_{QFC}	DC	–	20	ns	C_L = 50 pF

[1] Not 100 % tested, guaranteed by design characterization.

AC Characteristics (SI Timing)
V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = – 40 to +110 °C; C_L = 50 pF

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Chip Select Setup	t_{CSS}	SR	10		ns	
Clock High Time	t_{CH}	SR	1.5 t_{OSC} + 10		ns	
Clock Low Time	t_{CL}	SR	1.5 t_{OSC} + 10		ns	
Clock Period	t_C	SR	4 t_{OSC}		ns	
DI Setup	t_{DIS}	SR	10		ns	
DI Hold	t_{DIH}	SR	0		ns	
Address to Data Out	t_{ADO}	DC	3 t_{OSC}		ns	
Output Delay	t_{OD}	DC		25	ns	
Data Float after $\overline{CS}$ high	t_{DF}	DC		25	ns	
Chip Select Hold	t_{CSH}	SR	1 t_{OSC}		ns	
Write to Clock	t_{WC}		0		ns	
$\overline{W}$ to $\overline{CS}$ high	t_{WCS}	SR	0		ns	
Address to Data In	t_{ADI}	DC	0		ns	

AC Characteristics (PI Timing)
V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = – 40 to + 110 °C; C_L = 50 pF

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Read-Cycle time	t_{CYR}	DC	4 t_{OSC}		ns	
Write-Cycle time	t_{CYW}	DC	4 t_{OSC}		ns	
ALE pulse width	t_{LHLL}	DC	30		ns	
Address setup to ALE low	t_{AVLL}	SR	20		ns	
Address hold after ALE low	t_{LLAX}	SR	20		ns	
$\overline{RD}$ pulse width	t_{RLRH}	SR	2 t_{OSC} + 30		ns	
$\overline{WR}$ pulse width	t_{WLWH}	SR	2 t_{OSC} + 30		ns	
ALE low to $\overline{WR}$ active	t_{LLWL}	SR	20		ns	
ALE low to $\overline{RD}$ active	t_{LLRL}	SR	20		ns	
Data float after $\overline{RD}$ high	t_{RFDX}	DC	0	20	ns	
$\overline{RD}$ low to data valid	t_{RLDV}	DC		2 t_{OSC} + 20	ns	
Data setup before $\overline{WR}$ high	t_{DVWH}	SR	30		ns	
Data hold after $\overline{WR}$ high	t_{WHDX}	SR	30		ns	
$\overline{CS}$ low to $\overline{RD}$ low	t_{CLRL} /	SR	0		ns	
$\overline{CS}$ low to $\overline{WR}$ low	t_{CLWL}	SR	0		ns	
$\overline{WR}$ high to next ALE low	t_{WHLL}	SR	1.5 t_{OSC}		ns	

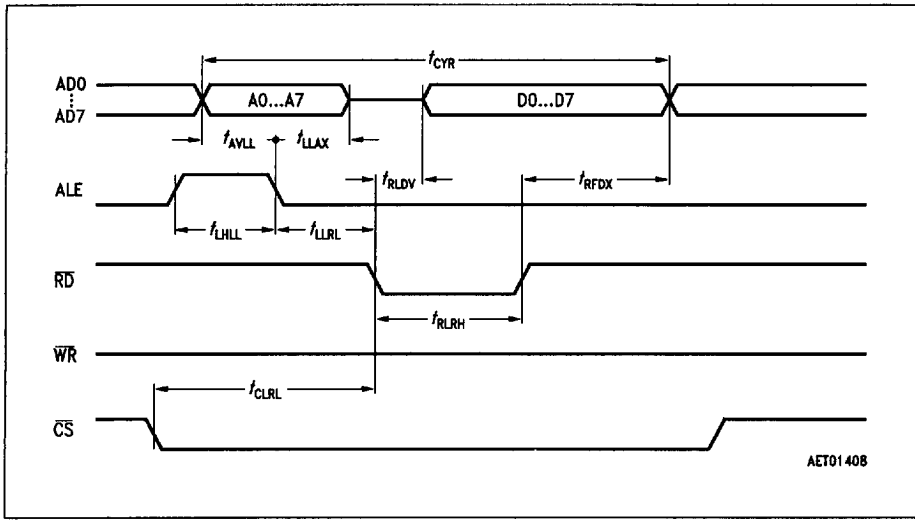


Figure 10
PI Timing: Read-Cycle-Timing

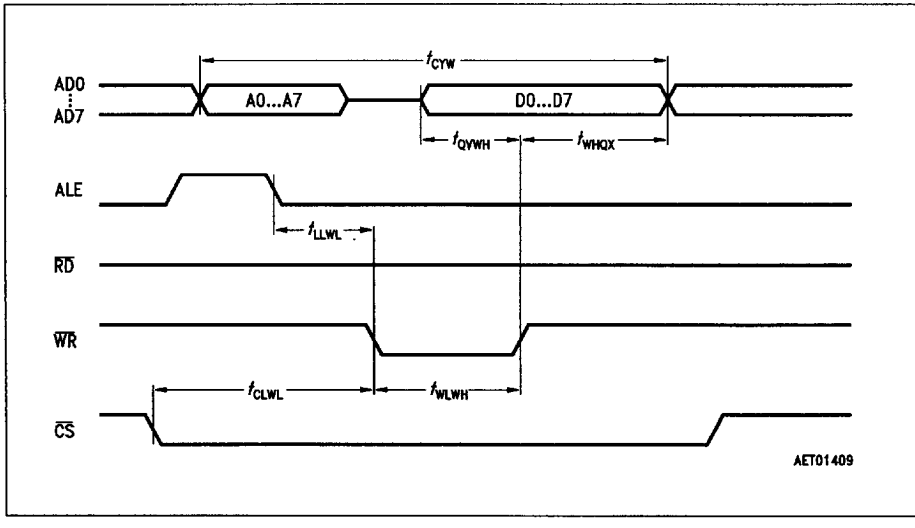


Figure 11
PI Timing: Write-Cycle-Timing

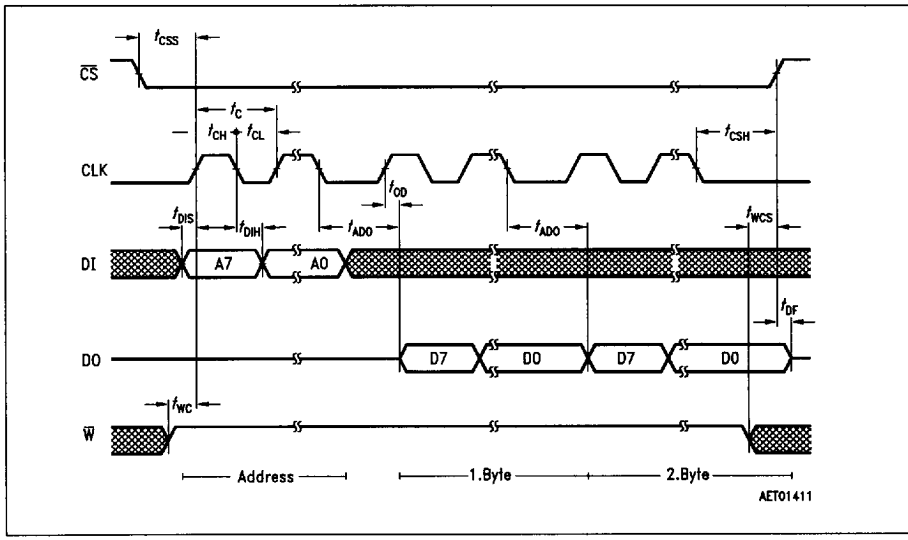


Figure 12
SI-Read-Timing (Timing A: Pin TIM = 0)

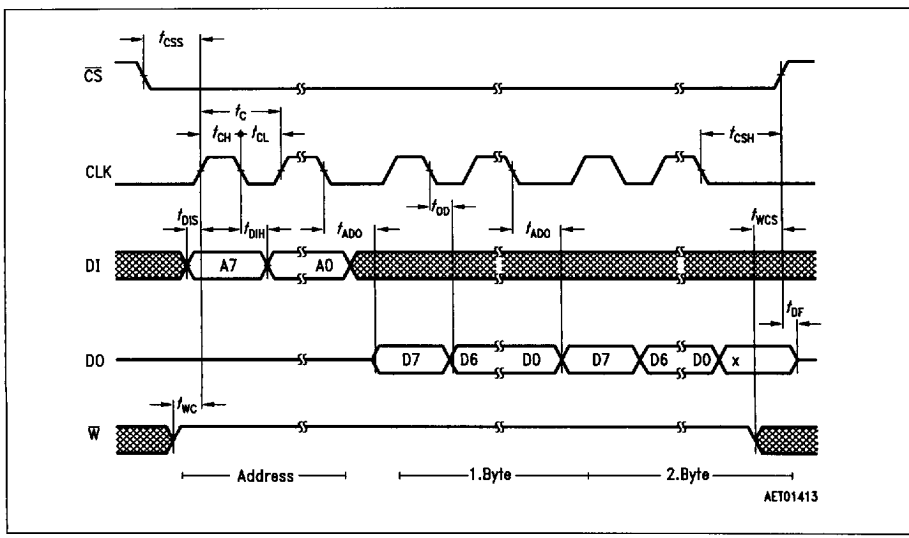


Figure 13
SI-Read-Timing (Timing B: Pin TIM = 1)

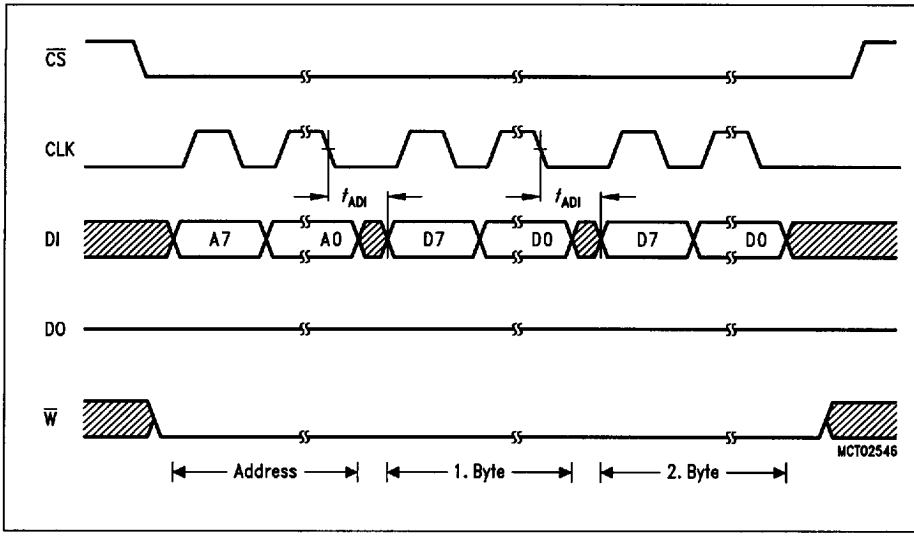


Figure 14
SI-Write-Timing

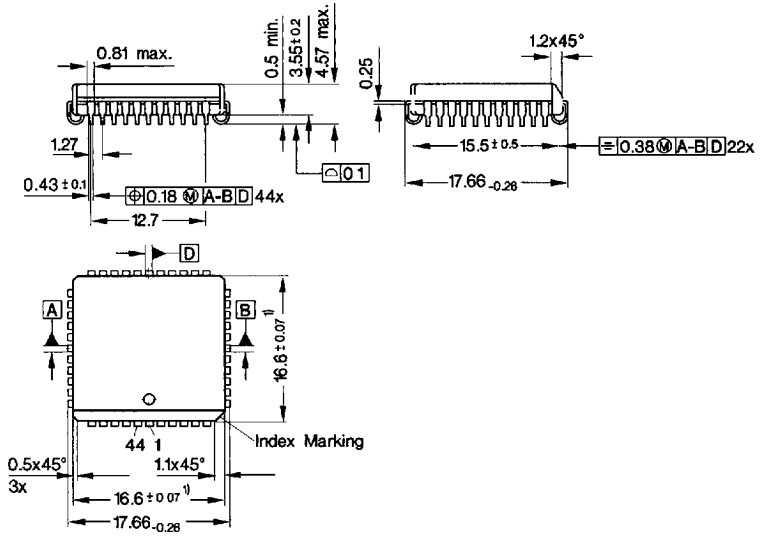
Package Outlines

The SAE 81C90/91 is available in two different packages:

- in a P-LCC-44-1 package named as SAE 81C90 and
- in a P-LCC-28-1 package named as SAE 81C91.

Note: In the last package the pads of the I/O-ports are not bonded and so they are not available.

Plastic-Package, P-LCC-44-1 (SMD)
(Plastic Leaded Chip Carrier)



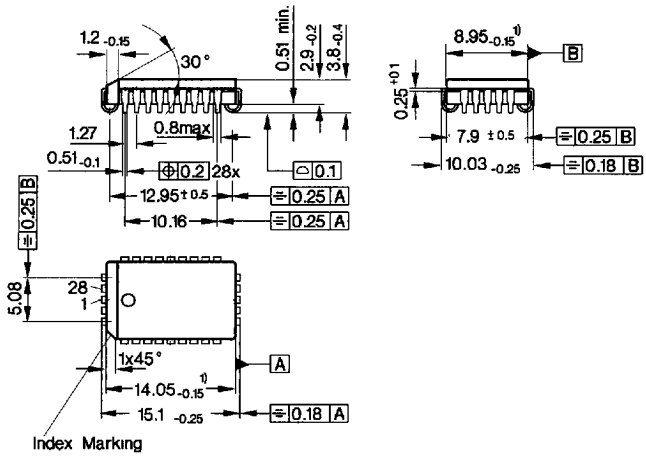
1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05102

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-LCC-28-1 (SMD)
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05018

B158-H6869-X-X-7600

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

8235605 0079784 250