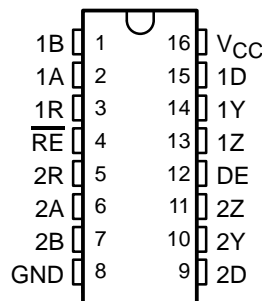


SN75ALS1177, SN75ALS1178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

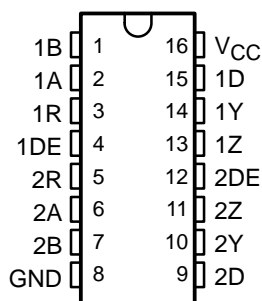
SLLS154B – MARCH 1993 – REVISED FEBRUARY 2001

- Meet or Exceed Standards TIA/EIA-422-B and TIA/EIA-485-A
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirement
50 mA Max
- Driver Positive- and Negative-Current Limiting
- Driver Common-Mode Output Voltage Range of -7 V to 12 V
- Thermal Shutdown Protection
- Driver 3-State Outputs Active-High Enable
- Receiver Common-Mode Input Voltage Range of -12 V to 12 V
- Receiver Input Sensitivity . . . $\pm 200\text{ mV}$
- Receiver Hysteresis . . . 50 mV Typ
- Receiver High Input Impedance . . . $12\text{ k}\Omega$ Min
- Receiver 3-State Outputs Active-Low Enable for SN75ALS1177 Only
- Operate From Single 5-V Supply

SN75ALS1177 . . . N OR NS PACKAGE
(TOP VIEW)



SN75ALS1178 . . . N OR NS PACKAGE
(TOP VIEW)



description

The SN75ALS1177 and SN75ALS1178 dual differential drivers and receivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet standards TIA/EIA-422-B and TIA/EIA-485-A.

The SN75ALS1177 combines dual 3-state differential line drivers and dual 3-state differential input line receivers, both of which operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which can be externally connected together to function as direction control. The SN75ALS1178 drivers each have an individual active-high enable. Fail-safe design ensures that when the receiver inputs are open, the receiver outputs are always high.

The SN75ALS1177 and SN75ALS1178 are characterized for operation from 0°C to 70°C .

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES	
	PLASTIC DIP (N)	PLASTIC SMALL OUTLINE (NS)
0°C to 70°C	SN75ALS1177N	SN75ALS1177NSR
	SN75ALS1178N	SN75ALS1178NSR

The NS package is only available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS1177NSR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN75ALS1177, SN75ALS1178

DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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Function Tables

SN75ALS1177, SN75ALS1178
(each driver)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN75ALS1177
(each receiver)

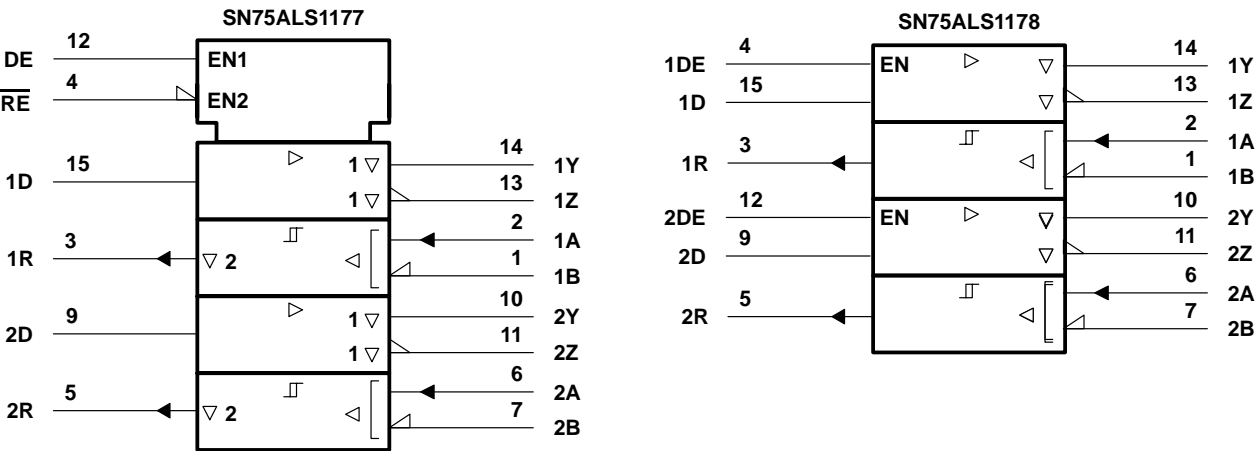
DIFFERENTIAL A–B	ENABLE $\overline{\text{RE}}$	OUTPUT Y
$V_{\text{ID}} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{\text{ID}} < 0.2 \text{ V}$	L	?
$V_{\text{ID}} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

SN75ALS1178
(each receiver)

DIFFERENTIAL A–B	OUTPUT Y
$V_{\text{ID}} \geq 0.2 \text{ V}$	H
$-0.2 \text{ V} < V_{\text{ID}} < 0.2 \text{ V}$?
$V_{\text{ID}} \leq -0.2 \text{ V}$	L
Open	H

H = High level, L = Low level,
? = Indeterminate, X = Irrelevant,
Z = High impedance (off)

logic symbol†

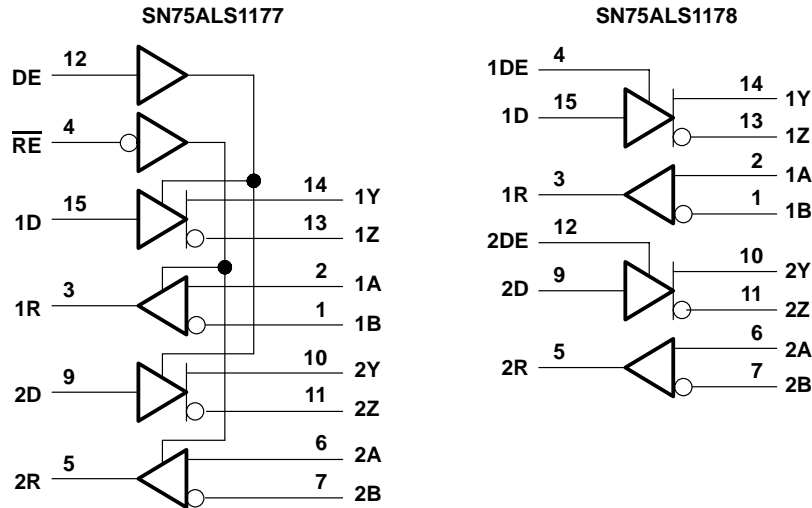


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

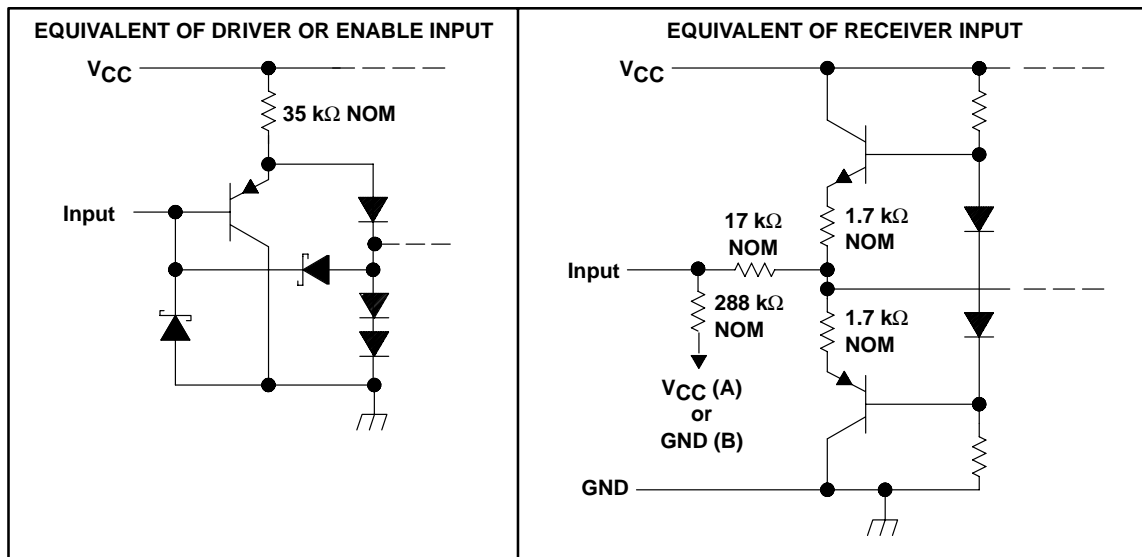
SN75ALS1177, SN75ALS1178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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logic diagram (positive logic)



equivalent schematics

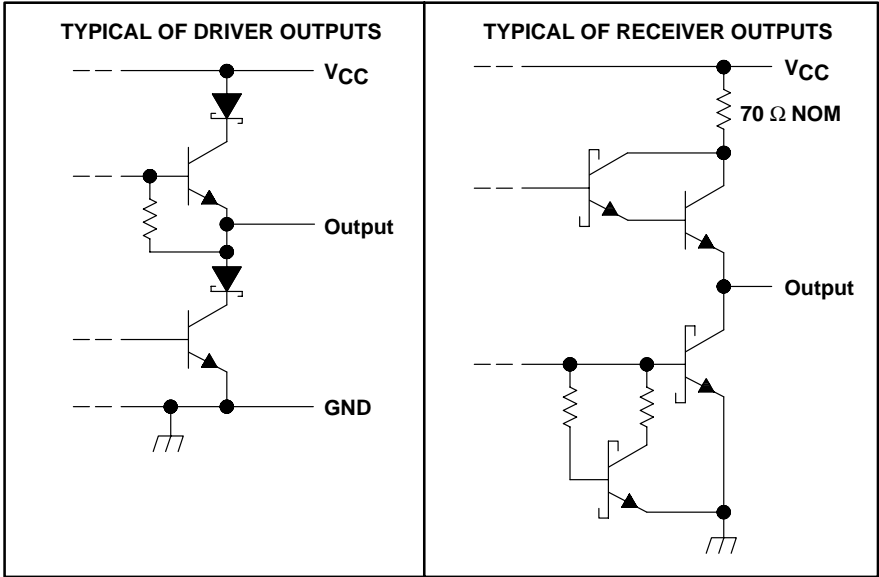


SN75ALS1177, SN75ALS1178

DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (DE, \overline{RE} , and D inputs)	7 V
Output voltage range, V_O (driver)	–9 V to 14 V
Input voltage range, receiver	–14 V to 14 V
Receiver differential-input voltage range (see Note 2)	–14 V to 14 V
Receiver low-level output current	50 mA
Package thermal impedance, θ_{JA} (see Note 3): N package	67°C/W
NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN75ALS1177, SN75ALS1178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{ID}	Differential input voltage	Receiver		±12	V
V _{OC}	Common-mode output voltage	Driver		–7 [†]	12
V _{IC}	Common-mode input voltage	Receiver		±12	V
V _{IH}	High-level input voltage	DE, \overline{RE} , D		2	V
V _{IL}	Low-level input voltage	DE, \overline{RE} , D		0.8	V
I _{OH}	High-level output current	Driver		–60	mA
		Receiver		–400	μA
I _{OL}	Low-level output current	Driver		60	mA
		Receiver		8	
T _A	Operating free-air temperature	0		70	°C

[†] The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage level only.



SN75ALS1177, SN75ALS1178

DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -33 \text{ mA}$		3.3		V
V_{OL} Low-level output voltage	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 33 \text{ mA}$		1.1		V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$V_{CC} = 5 \text{ V}$, $R_L = 100 \Omega$, See Figure 1	$\frac{1}{2} V_{OD1}$ or $2\frac{1}{2}$			V
	$R_L = 54 \Omega$, See Figure 1	1.5	2.5	5	
$ V_{OD3} $ Differential output voltage	See Note 4	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage (see Note 5)	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage	$R_L = 54 \Omega$ or 100Ω , See Figure 1	-1§		3	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage (see Note 5)	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
$I_{O(OFF)}$ Output current with power off	$V_{CC} = 0$, $V_O = -7 \text{ V}$ to 12 V			± 100	μA
I_{OZ} High-impedance-state output current	$V_O = -7 \text{ V}$ to 12 V			± 100	μA
I_{IH} High-level input current	$V_{IH} = 2.7 \text{ V}$			100	μA
I_{IL} Low-level input current	$V_{IL} = 0.4 \text{ V}$			-100	μA
I_{OS} Short-circuit output current	$V_O = -7 \text{ V}$			-250	mA
	$V_O = V_{CC}$			250	
	$V_O = 12 \text{ V}$			250	
	$V_O = 0 \text{ V}$			150	
I_{CC} Supply current (total package)	No load	Outputs enabled		35	mA
		Outputs disabled		20	

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $\frac{1}{2} V_{OD1}$ or 2 V , whichever is greater.

§ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 4. See TIA/EIA-485-A Figure 3.5, test termination measurement 2.

5. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

switching characteristics at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, high- to low-level output	$R_L = 60 \Omega$, $C_{L1} = C_{L2} = 100 \text{ pF}$, See Figure 3	9	15	22	ns
t_{PHL} Propagation delay time, low- to high-level output	$R_L = 60 \Omega$, $C_{L1} = C_{L2} = 100 \text{ pF}$, See Figure 3	9	15	22	ns
t_{sk} Output-to-output skew	$R_L = 60 \Omega$, $C_{L1} = C_{L2} = 100 \text{ pF}$, See Figure 3	0	2	8	ns
t_{PZH} Output enable time to high level	$C_L = 100 \text{ pF}$, See Figure 4	30	35	50	ns
t_{PZL} Output enable time to low level	$C_L = 100 \text{ pF}$, See Figure 5	5	15	25	ns
t_{PHZ} Output disable time from high level	$C_L = 15 \text{ pF}$, See Figure 4	7	15	30	ns
t_{PLZ} Output disable time from low level	$C_L = 15 \text{ pF}$, See Figure 5	7	15	30	ns



SN75ALS1177, SN75ALS1178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7\text{ V}$, $I_O = -0.4\text{ mA}$			0.2	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5\text{ V}$, $I_O = 8\text{ mA}$	-0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
V_{IK}	Enable input clamp voltage	SN75ALS1177 $I_I = -18\text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200\text{ mV}$, $I_{OH} = -400\text{ }\mu\text{A}$, See Figure 2		2.7		V
V_{OL}	Low-level output voltage	$V_{ID} = 200\text{ mV}$, $I_{OL} = 8\text{ mA}$, See Figure 2			0.45	V
I_{OZ}	High-impedance-state output current	SN75ALS1177 $V_O = 0.4\text{ V to } 2.4\text{ V}$			± 20	μA
I_I	Line input current (see Note 6)	Other input at 0 V				
		$V_I = 12\text{ V}$			1	mA
		$V_I = -7\text{ V}$			-0.8	mA
I_{IH}	High-level input current, \overline{RE}	SN75ALS1177 $V_{IH} = 2.7\text{ V}$			20	μA
I_{IL}	Low-level input current, \overline{RE}	SN75ALS1177 $V_{IL} = 0.4\text{ V}$			-100	μA
r_i	Input resistance			12		$\text{k}\Omega$
I_{OS}	Short-circuit output current	$V_O = 0\text{ V}$, See Note 7	-15		-85	mA
I_{CC}	Supply current (total package)	No load, Outputs enabled		35	50	mA

† All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 6. Refer to TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.

7. Not more than one output should be shorted at a time.

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 15\text{ pF}$, See Figure 6	15	25	37	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 15\text{ pF}$, See Figure 6	15	25	37	ns
t_{PZH}	Output enable time to high level	SN75ALS1177 $C_L = 100\text{ pF}$, See Figure 7	10	20	30	ns
t_{PZL}	Output enable time to low level	SN75ALS1177 $C_L = 100\text{ pF}$, See Figure 7	10	20	30	ns
t_{PHZ}	Output disable time from high level	SN75ALS1177 $C_L = 15\text{ pF}$, See Figure 7	3.5	12	16	ns
t_{PLZ}	Output disable time from low level	SN75ALS1177 $C_L = 15\text{ pF}$, See Figure 7	5	12	16	ns

SN75ALS1177, SN75ALS1178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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PARAMETER MEASUREMENT INFORMATION

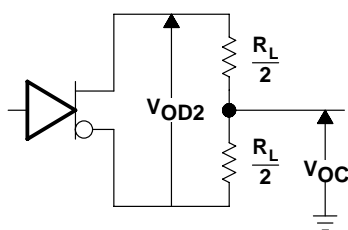


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

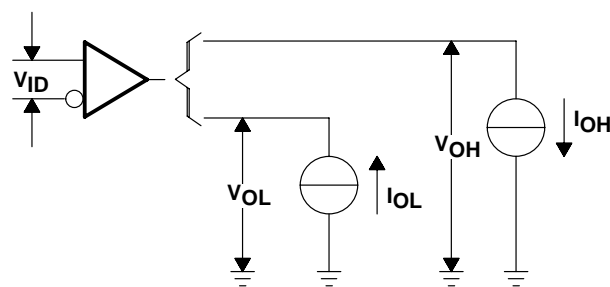
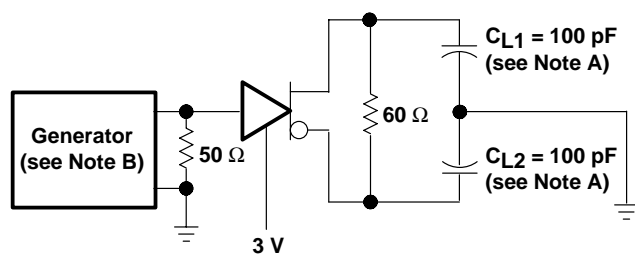
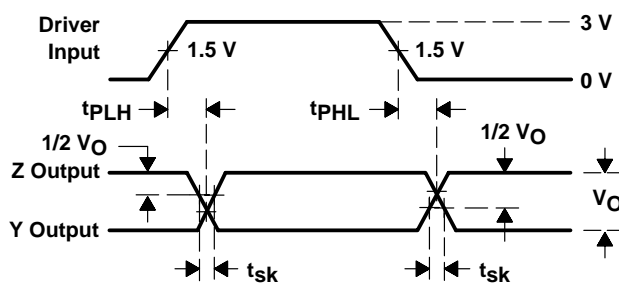


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}



DRIVER TEST CIRCUIT

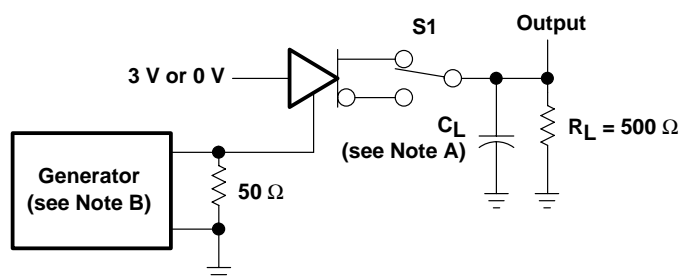


DRIVER VOLTAGE WAVEFORMS

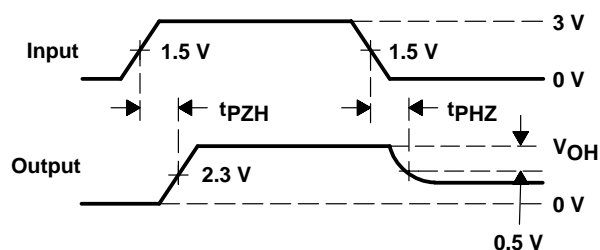
NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 3. Driver Propagation Delay Times



DRIVER TEST CIRCUIT



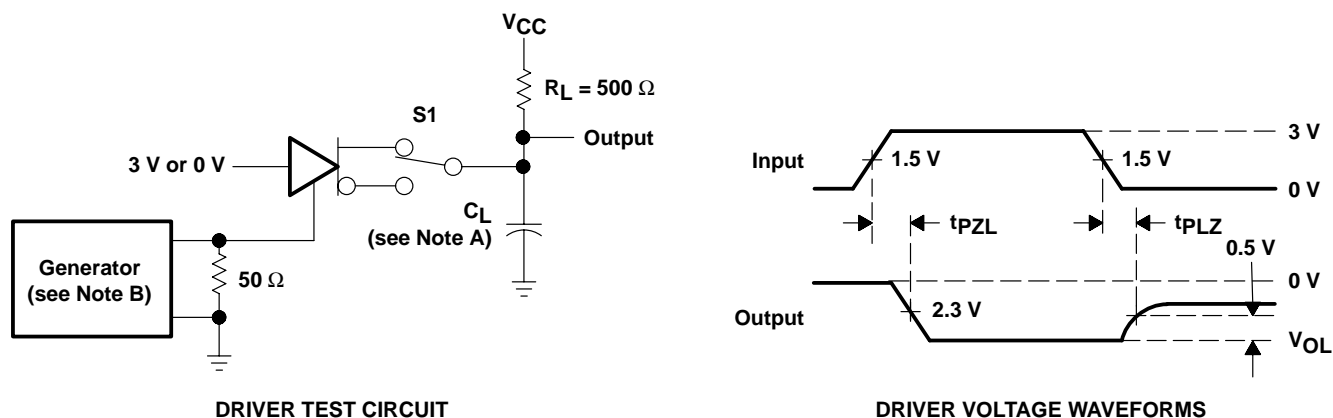
DRIVER VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

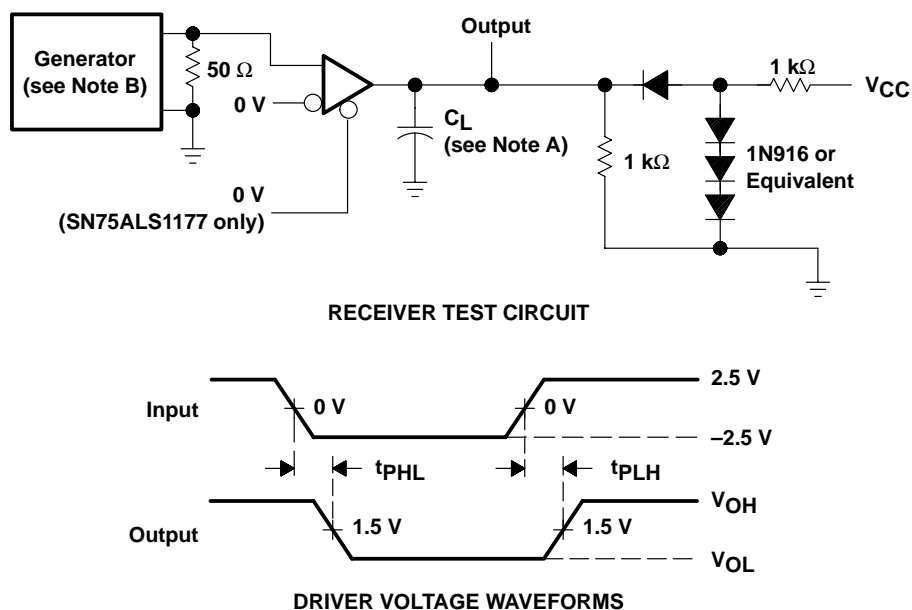
Figure 4. Driver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 5. Driver Enable and Disable Times



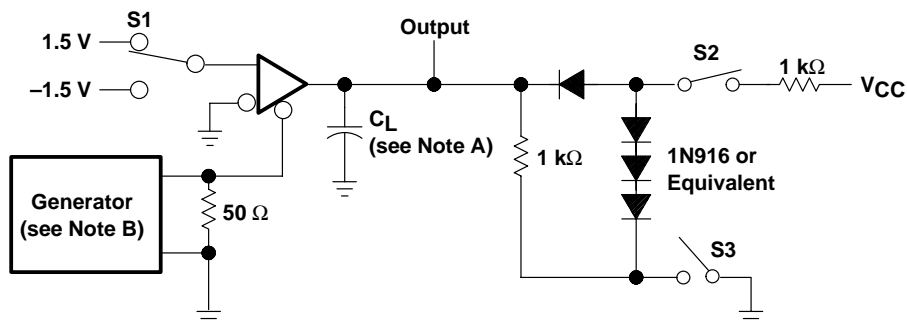
- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 6. Receiver Propagation Delay Times

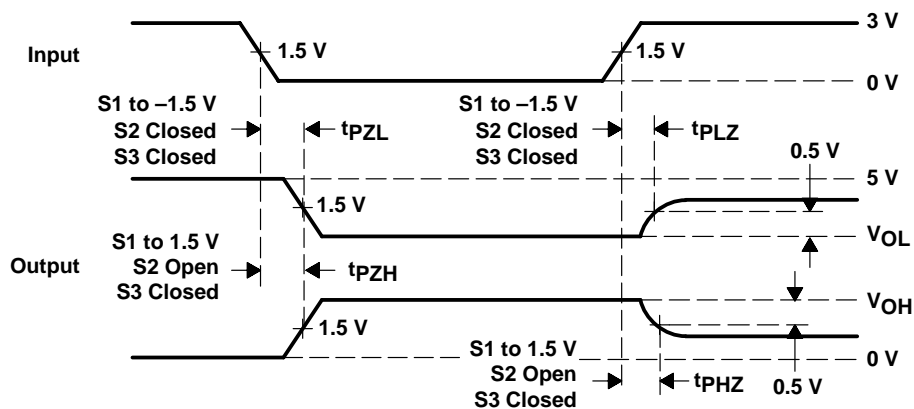
SN75ALS1177, SN75ALS1178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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PARAMETER MEASUREMENT INFORMATION



RECEIVER TEST CIRCUIT



RECEIVER VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 7. Receiver Output Enable and Disable Times

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75ALS1177N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS1177NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS1177NSLE	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI
SN75ALS1177NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS1177NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS1178N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS1178NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS1178NSLE	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI
SN75ALS1178NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS1178NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

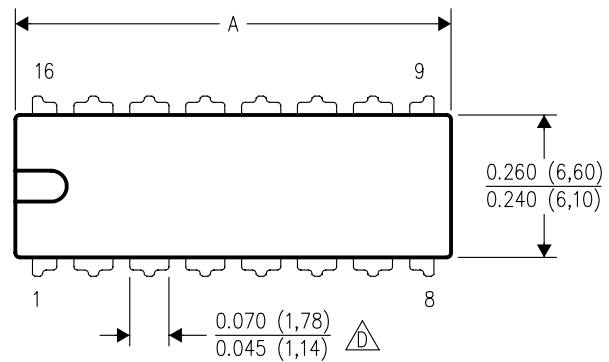
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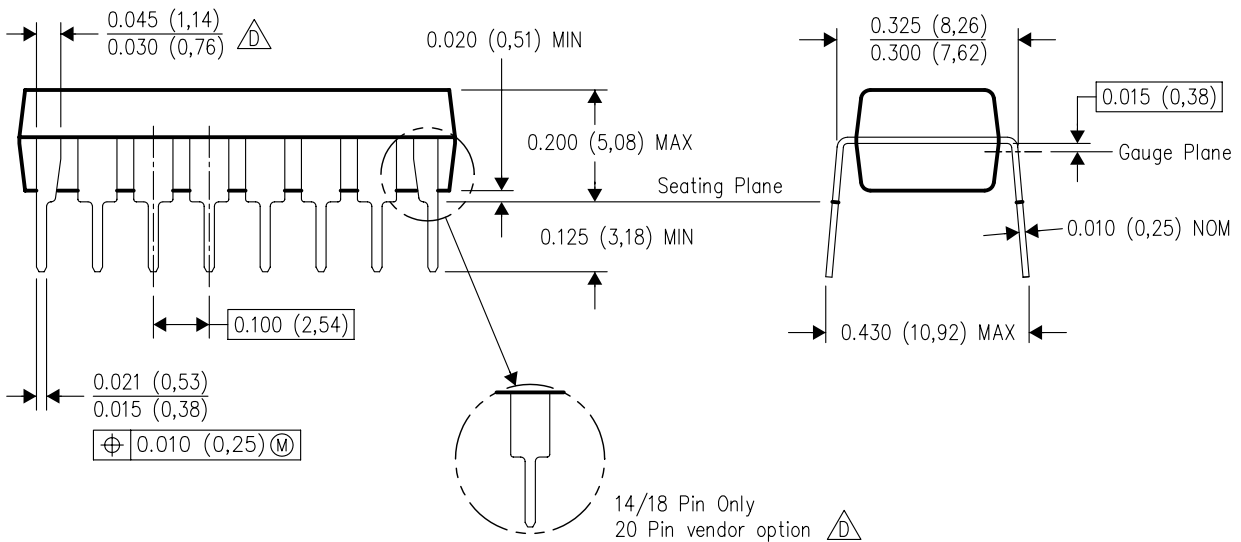
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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