

FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of up to**
–40°C to 85°C, –40°C to 125°C and –55°C to 125°C
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** ⁽¹⁾
- **Member of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

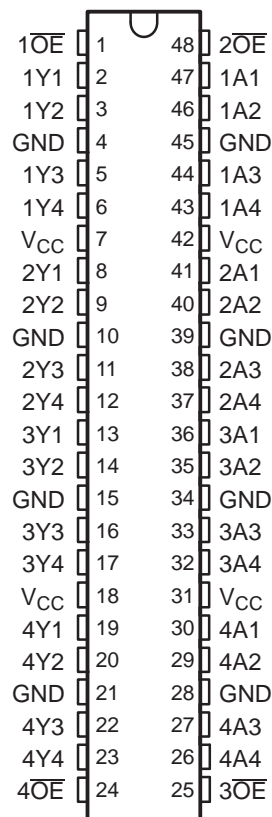
(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION/ORDERING INFORMATION

The SN74LVTH16244A is a 16-bit buffer and line driver designed for low-voltage (3.3 V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. This device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74LVTH16244A-EP

3.3-V ABT 16-BIT BUFFER/DRIVER

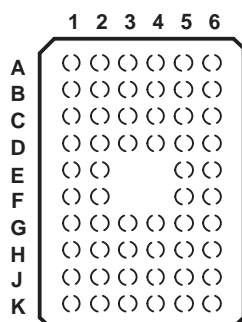
WITH 3-STATE OUTPUTS

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When V_{CC} is between 0 V and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
A	$1\overline{OE}$	NC	NC	NC	NC	$2\overline{OE}$
B	1Y2	1Y1	GND	GND	1A1	1A2
C	1Y4	1Y3	V_{CC}	V_{CC}	1A3	1A4
D	2Y2	2Y1	GND	GND	2A1	2A2
E	2Y4	2Y3			2A3	2A4
F	3Y1	3Y2			3A2	3A1
G	3Y3	3Y4	GND	GND	3A4	3A3
H	4Y1	4Y2	V_{CC}	V_{CC}	4A2	4A1
J	4Y3	4Y4	GND	GND	4A4	4A3
K	$4\overline{OE}$	NC	NC	NC	NC	$3\overline{OE}$

(1) NC - No internal connection

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SSOP – DL	Tape and reel	CLVTH16244AQLREP	LH16244AEP
	TSSOP – DGG	Tape and reel	CLVTH16244AQDGGREP	LH16244AEP
–40°C to 85°C	TVSOP – DGV	Tape and reel	CLVTH16244AIDGVREP	LL244AEP
	VFBGA – GQL	Tape and reel	CLVTH162244AIGQLREP	LL244AEP
	VFBGA – ZQL (Pb-free)		CLVTH16244AIZQLREP	
–55°C to 125°C	TSSOP – DGG	Tape and reel	CLVTH16244AMDGGREP	H16244AMEP

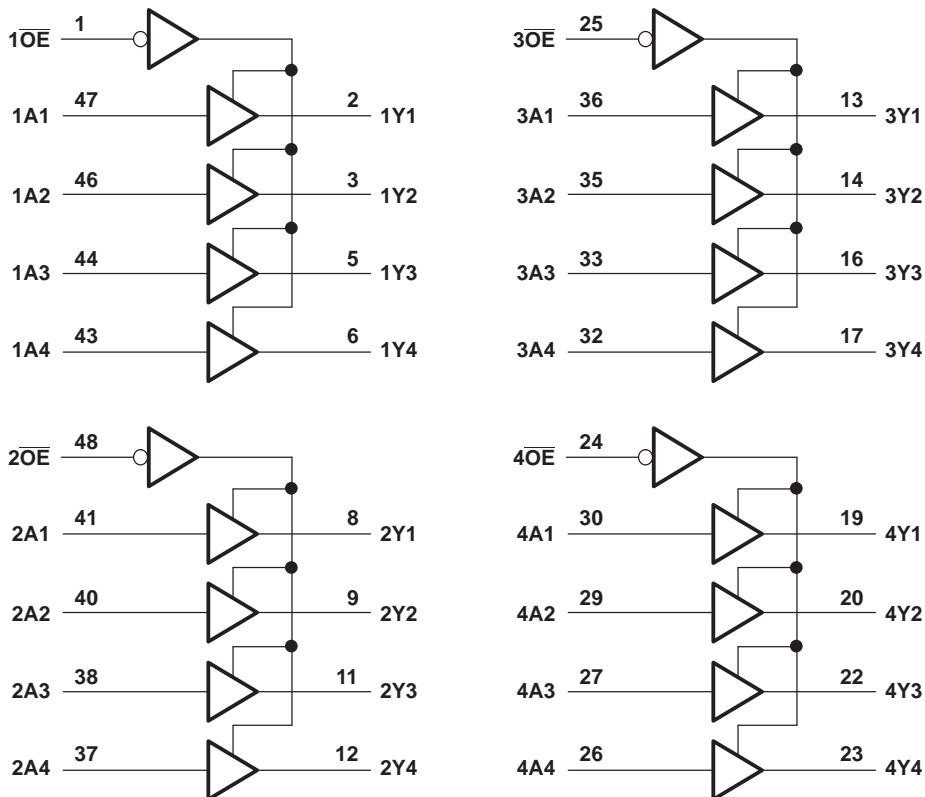
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

SN74LVTH16244A-EP

3.3-V ABT 16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range ⁽²⁾		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5	7	V
V_O	Voltage range applied to any output in the high state ⁽²⁾		–0.5	$V_{CC} + 0.5$	V
I_O	Current into any output in the low state	SN74LVTH16244AQ		96	mA
		SN74LVTH16244AI		128	
I_O	Current into any output in the high state ⁽³⁾	SN74LVTH16244AQ		48	mA
		SN74LVTH16244AI		64	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		70	°C/W
		DGV package		58	
		DL package		63	
		GQL/ZQL package		42	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current	SN74LVTH16244AQ		–24	mA
		SN74LVTH16244AI		–32	
		SN74LVTH16244AM		–24	
I_{OL}	Low-level output current	SN74LVTH16244AQ		24	mA
		SN74LVTH16244AI		64	
		SN74LVTH16244AM		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		μs/V
T_A	Operating free-air temperature	SN74LVTH16244AQ	–40	125	°C
		SN74LVTH16244AI	–40	85	
		SN74LVTH16244AM	–55	125	

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

over recommended operating free-air temperature range (unless otherwise noted)

- (1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.
- (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
- (3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN74LVTH16244A-EP

3.3-V ABT 16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

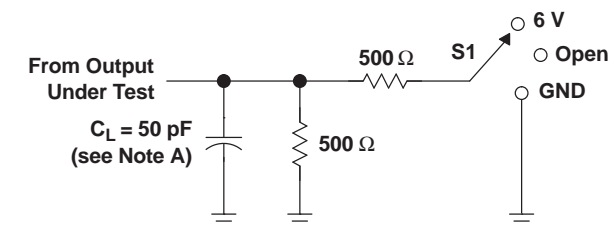
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
C _O	V _O = 3 V or 0 V			9		pF

Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Figure 1](#))

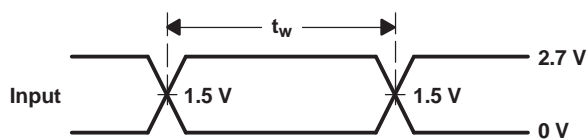
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVTH16244AQ/M				SN74LVTH16244AI				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN		MAX
t _{PLH}	A	Y	1.1	4.4	4.6		1.2	2.5	3.2	3.7		ns
t _{PHL}			1.1	3.6	3.9		1.2	2	3.2	3.7		
t _{PZH}	OE	Y	1.1	4.6	5.4		1.2	2.6	4	5		ns
t _{PZL}			1.1	5.4	6.2		1.2	2.7	4	5		
t _{PHZ}	OE	Y	1.6	5.7	6.2		2.2	3.3	4.5	5		ns
t _{PLZ}			1.2	5	4.7		2	3.1	4.2	4.4		
t _{sk(o)}									0.5			ns

PARAMETER MEASUREMENT INFORMATION

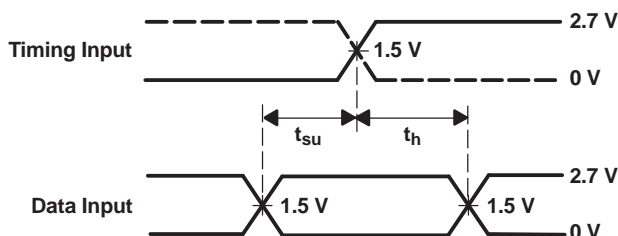


LOAD CIRCUIT

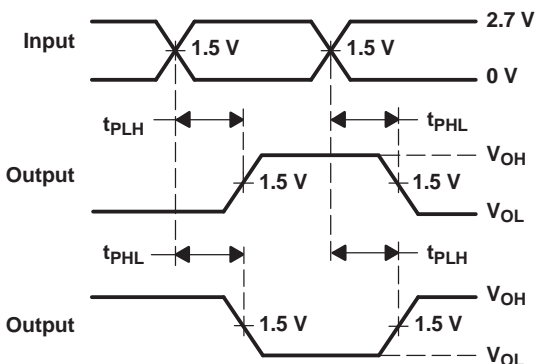
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



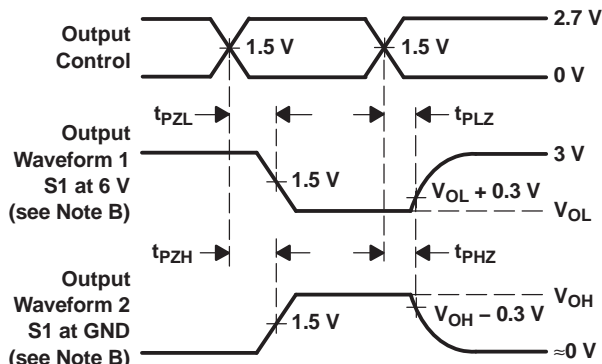
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8W244AMDGGREPG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	H16244AMEP
CLVTH16244AIDGVREP	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LL244AEP
CLVTH16244AMDGGREP	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	H16244AMEP
CLVTH16244AQDGGREP	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LH16244AEP
CLVTH16244AQDLREP	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LH16244AEP
V62/04601-01XE	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LH16244AEP
V62/04601-01YE	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LH16244AEP
V62/04601-02ZE	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LL244AEP
V62/04601-03YE	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	H16244AMEP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVTH16244A-EP :

- Catalog : [SN74LVTH16244A](#)
- Military : [SN54LVTH16244A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVTH16244AIDGVREP	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
CLVTH16244AMDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CLVTH16244AQDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CLVTH16244AQDLREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

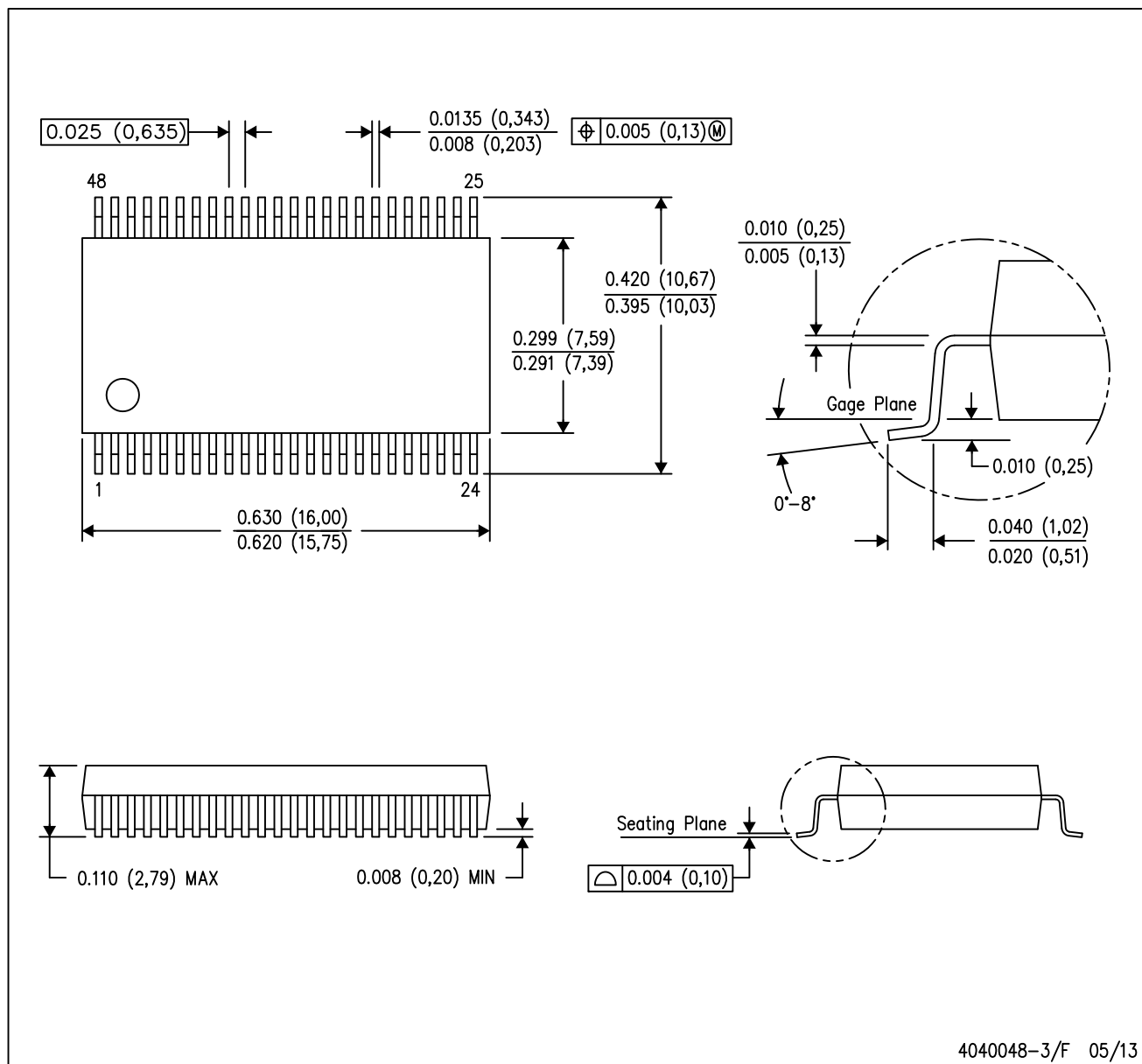


*All dimensions are nominal

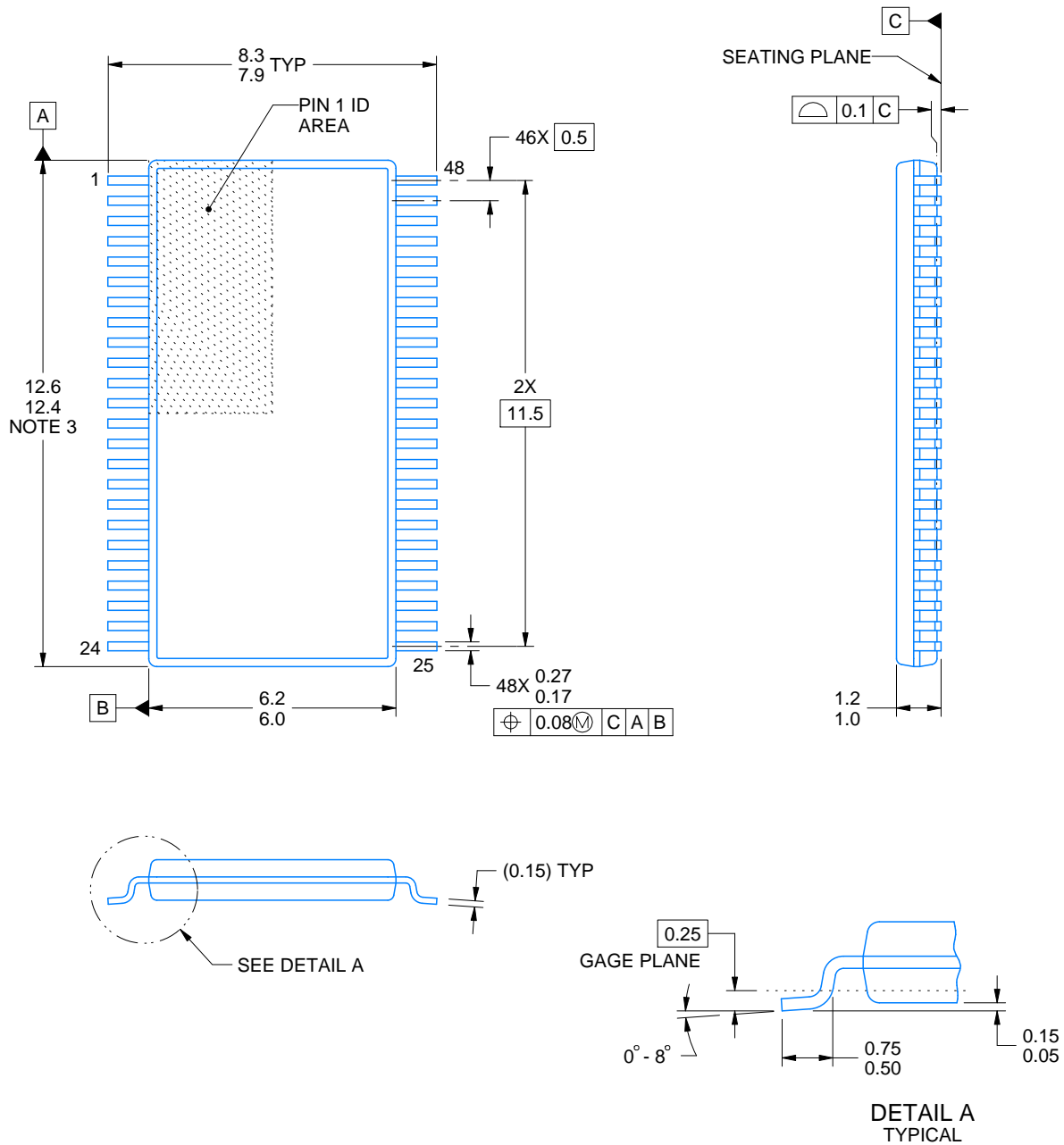
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVTH16244AIDGVREP	TVSOP	DGV	48	2000	353.0	353.0	32.0
CLVTH16244AMDGGREP	TSSOP	DGG	48	2000	356.0	356.0	45.0
CLVTH16244AQDGGREP	TSSOP	DGG	48	2000	356.0	356.0	45.0
CLVTH16244AQDLREP	SSOP	DL	48	1000	356.0	356.0	53.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



4214859/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

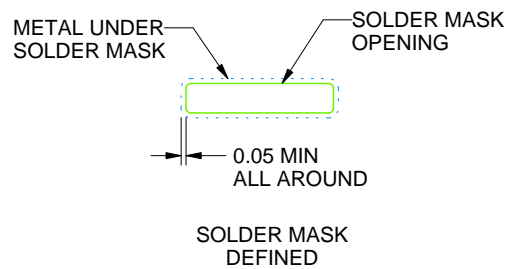
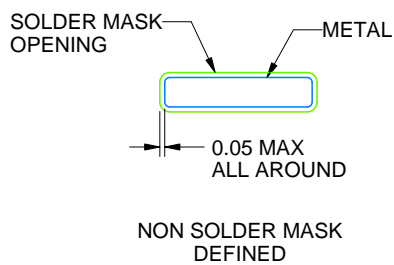
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

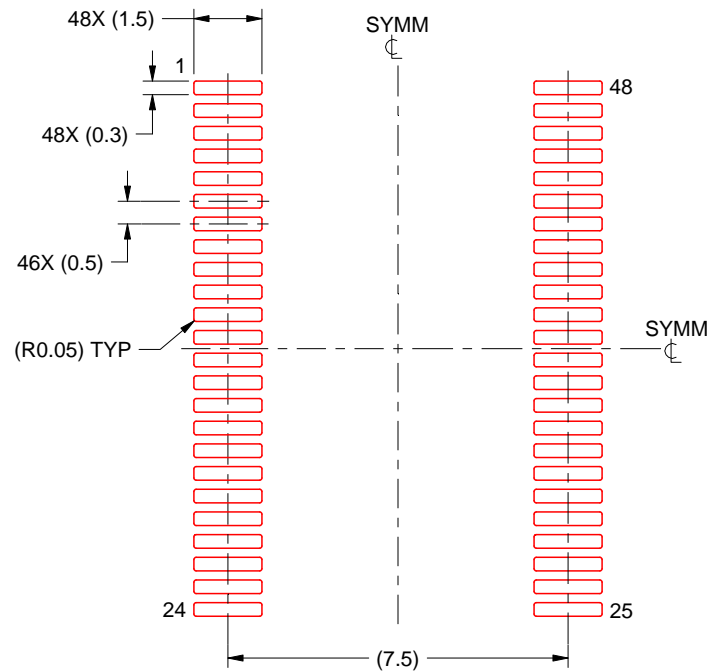
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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