

74LVC1T45; 74LVCH1T45

Dual supply translating transceiver; 3-state

Rev. 6 — 6 August 2012

Product data sheet

1. General description

The 74LVC1T45; 74LVCH1T45 are single bit, dual supply transceivers with 3-state outputs that enable bidirectional level translation. They feature two 1-bit input-output ports (A and B), a direction control input (DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins A and DIR are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The devices are fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the 74LVCH1T45 holds unused or floating data inputs at a valid logic level.

2. Features and benefits

- Wide supply voltage range:
 - ◆ $V_{CC(A)}$: 1.2 V to 5.5 V
 - ◆ $V_{CC(B)}$: 1.2 V to 5.5 V
- High noise immunity
- Complies with JEDEC standards:
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8C (2.7 V to 3.6 V)
 - ◆ JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - ◆ HBM JESD22-A114F Class 3A exceeds 4000 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Maximum data rates:
 - ◆ 420 Mbps (3.3 V to 5.0 V translation)
 - ◆ 210 Mbps (translate to 3.3 V))
 - ◆ 140 Mbps (translate to 2.5 V)
 - ◆ 75 Mbps (translate to 1.8 V)
 - ◆ 60 Mbps (translate to 1.5 V)
- Suspend mode



- Latch-up performance exceeds 100 mA per JESD 78 Class II
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- Inputs accept voltages up to 5.5 V
- Low power consumption: 16 μ A maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1T45GW	-40 °C to $+125$ °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVCH1T45GW				
74LVC1T45GM	-40 °C to $+125$ °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm	SOT886
74LVCH1T45GM				
74LVC1T45GF	-40 °C to $+125$ °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1 \times 0.5$ mm	SOT891
74LVCH1T45GF				
74LVC1T45GN	-40 °C to $+125$ °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115
74LVCH1T45GN				
74LVC1T45GS	-40 °C to $+125$ °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202
74LVCH1T45GS				

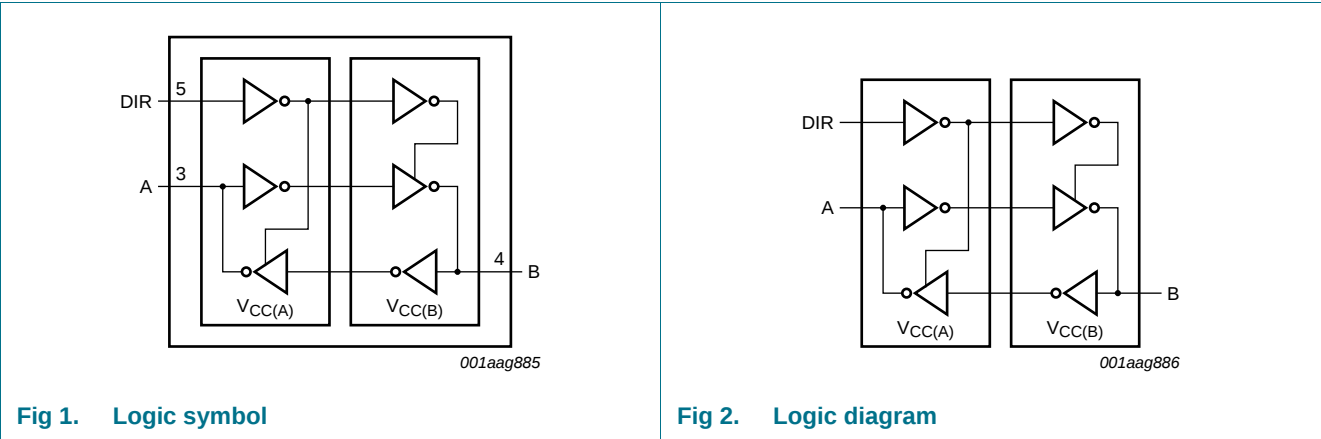
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1T45GW	V5
74LVCH1T45GW	X5
74LVC1T45GM	V5
74LVCH1T45GM	X5
74LVC1T45GF	V5
74LVCH1T45GF	X5
74LVC1T45GN	V5
74LVCH1T45GN	X5
74LVC1T45GS	V5
74LVCH1T45GS	X5

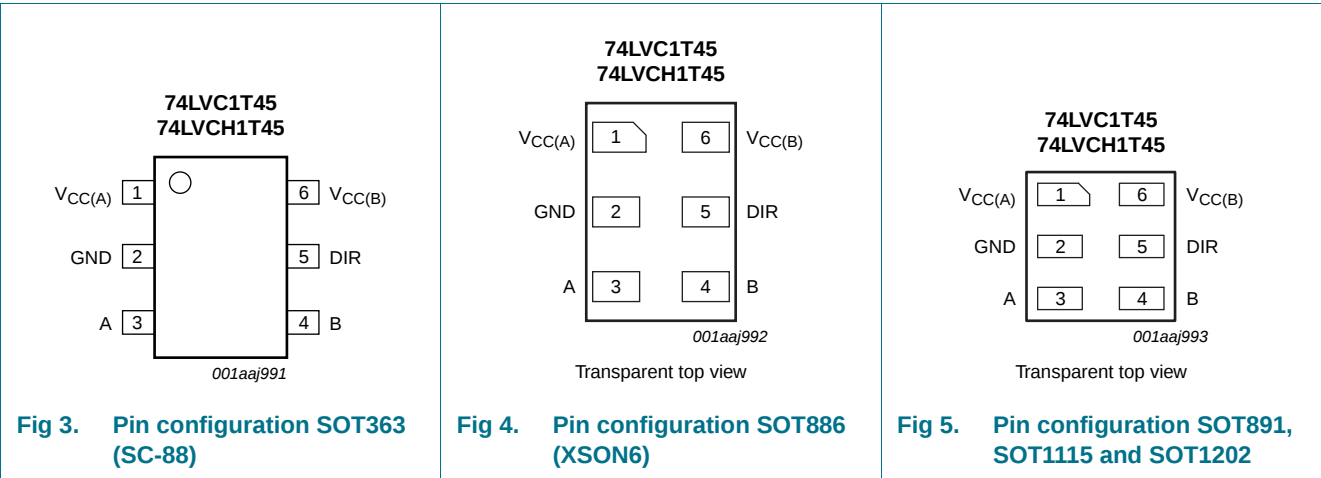
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V _{CC} (A)	1	supply voltage port A and DIR
GND	2	ground (0 V)
A	3	data input or output
B	4	data input or output
DIR	5	direction control
V _{CC} (B)	6	supply voltage port B

7. Functional description

Table 4. Function table^[1]

Supply voltage	Input	Input/output ^[2]	
$V_{CC(A)}$, $V_{CC(B)}$	DIR	A	B
1.2 V to 5.5 V	L	A = B	input
1.2 V to 5.5 V	H	input	B = A
GND ^[3]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The input circuit of the data I/O is always active.

[3] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		^[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode	^{[1][2][3]} -0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	^[1] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CCO}	^[2] -	± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[4] -	250	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] $V_{CCO} + 0.5$ V should not exceed 6.5 V.

[4] For SC-88 package: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	5.5	V
$V_{CC(B)}$	supply voltage B		1.2	5.5	V
V_I	input voltage		0	5.5	V

Table 6. Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Max	Unit
V _O	output voltage	Active mode	[1] 0	V _{CCO}	V
		Suspend or 3-state mode	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CCI} = 1.2 V	[2] -	20	ns/V
		V _{CCI} = 1.4 V to 1.95 V	-	20	ns/V
		V _{CCI} = 2.3 V to 2.7 V	-	20	ns/V
		V _{CCI} = 3 V to 3.6 V	-	10	ns/V
		V _{CCI} = 4.5 V to 5.5 V	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

10. Static characteristics

Table 7. Typical static characteristics at T_{amb} = 25 °C

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -3 mA; V _{CCO} = 1.2 V	[1] -	1.09	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 3 mA; V _{CCO} = 1.2 V	[1] -	0.07	-	V
I _I	input leakage current	DIR input; V _I = 0 V to 5.5 V; V _{CCI} = 1.2 V to 5.5 V	[2] -	-	±1	μA
I _{BHL}	bus hold LOW current	A or B port; V _I = 0.42 V; V _{CCI} = 1.2 V	[2] -	19	-	μA
I _{BHH}	bus hold HIGH current	A or B port; V _I = 0.78 V; V _{CCI} = 1.2 V	[2] -	-19	-	μA
I _{BHLO}	bus hold LOW overdrive current	A or B port; V _{CCI} = 1.2 V	[2][3] -	19	-	μA
I _{BHHO}	bus hold HIGH overdrive current	A or B port; V _{CCI} = 1.2 V	[2][3] -	-19	-	μA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CCO} = 1.2 V to 5.5 V	[1] -	-	±1	μA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 5.5 V; V _{CC(A)} = 0 V; V _{CC(B)} = 1.2 V to 5.5 V	-	-	±1	μA
		B port; V _I or V _O = 0 V to 5.5 V; V _{CC(B)} = 0 V; V _{CC(A)} = 1.2 V to 5.5 V	-	-	±1	μA
C _I	input capacitance	DIR input; V _I = 0 V or 3.3 V; V _{CC(A)} = V _{CC(B)} = 3.3 V	-	2.2	-	pF
C _{I/O}	input/output capacitance	A and B port; suspend mode; V _O = 3.3 V or 0 V; V _{CC(A)} = V _{CC(B)} = 3.3 V	-	6.0	-	pF

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input [1]					
		$V_{CCI} = 1.2\text{ V}$	$0.8V_{CCI}$	-	$0.8V_{CCI}$	-	V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	1.7	-	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	2.0	-	V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CCI}$	-	$0.7V_{CCI}$	-	V
		DIR input					
		$V_{CCI} = 1.2\text{ V}$	$0.8V_{CC(A)}$	-	$0.8V_{CC(A)}$	-	V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	1.7	-	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	2.0	-	V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC(A)}$	-	$0.7V_{CC(A)}$	-	V
V_{IL}	LOW-level input voltage	data input [1]					
		$V_{CCI} = 1.2\text{ V}$	-	$0.2V_{CCI}$	-	$0.2V_{CCI}$	V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	-	0.7	-	0.7	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	-	0.8	-	0.8	V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	-	$0.3V_{CCI}$	-	$0.3V_{CCI}$	V
		DIR input					
		$V_{CCI} = 1.2\text{ V}$	-	$0.2V_{CC(A)}$	-	$0.2V_{CC(A)}$	V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	-	0.7	-	0.7	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	-	0.8	-	0.8	V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	-	$0.3V_{CC(A)}$	-	$0.3V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$					
		$I_O = -100\text{ }\mu\text{A}$; $V_{CCO} = 1.2\text{ V to }4.5\text{ V}$ [2]	$V_{CCO} - 0.1$	-	$V_{CCO} - 0.1$	-	V
		$I_O = -6\text{ mA}$; $V_{CCO} = 1.4\text{ V}$	1.0	-	1.0	-	V
		$I_O = -8\text{ mA}$; $V_{CCO} = 1.65\text{ V}$	1.2	-	1.2	-	V
		$I_O = -12\text{ mA}$; $V_{CCO} = 2.3\text{ V}$	1.9	-	1.9	-	V
		$I_O = -24\text{ mA}$; $V_{CCO} = 3.0\text{ V}$	2.4	-	2.4	-	V
		$I_O = -32\text{ mA}$; $V_{CCO} = 4.5\text{ V}$	3.8	-	3.8	-	V

Table 8. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IL} [2]					
		I _O = 100 µA; V _{CCO} = 1.2 V to 4.5 V	-	0.1	-	0.1	V
		I _O = 6 mA; V _{CCO} = 1.4 V	-	0.3	-	0.3	V
		I _O = 8 mA; V _{CCO} = 1.65 V	-	0.45	-	0.45	V
		I _O = 12 mA; V _{CCO} = 2.3 V	-	0.3	-	0.3	V
		I _O = 24 mA; V _{CCO} = 3.0 V	-	0.55	-	0.55	V
		I _O = 32 mA; V _{CCO} = 4.5 V	-	0.55	-	0.55	V
I _I	input leakage current	DIR input; V _I = 0 V to 5.5 V; V _{CCI} = 1.2 V to 5.5 V	-	±2	-	±10	µA
I _{BHL}	bus hold LOW current	A or B port [1]					
		V _I = 0.49 V; V _{CCI} = 1.4 V	15	-	10	-	µA
		V _I = 0.58 V; V _{CCI} = 1.65 V	25	-	20	-	µA
		V _I = 0.70 V; V _{CCI} = 2.3 V	45	-	45	-	µA
		V _I = 0.80 V; V _{CCI} = 3.0 V	100	-	80	-	µA
		V _I = 1.35 V; V _{CCI} = 4.5 V	100	-	100	-	µA
I _{BHH}	bus hold HIGH current	A or B port [1]					
		V _I = 0.91 V; V _{CCI} = 1.4 V	-15	-	-10	-	µA
		V _I = 1.07 V; V _{CCI} = 1.65 V	-25	-	-20	-	µA
		V _I = 1.60 V; V _{CCI} = 2.3 V	-45	-	-45	-	µA
		V _I = 2.00 V; V _{CCI} = 3.0 V	-100	-	-80	-	µA
		V _I = 3.15 V; V _{CCI} = 4.5 V	-100	-	-100	-	µA
I _{BHLO}	bus hold LOW overdrive current	A or B port [1][3]					
		V _{CCI} = 1.6 V	125	-	125	-	µA
		V _{CCI} = 1.95 V	200	-	200	-	µA
		V _{CCI} = 2.7 V	300	-	300	-	µA
		V _{CCI} = 3.6 V	500	-	500	-	µA
		V _{CCI} = 5.5 V	900	-	900	-	µA
I _{BHHO}	bus hold HIGH overdrive current	A or B port [1][3]					
		V _{CCI} = 1.6 V	-125	-	-125	-	µA
		V _{CCI} = 1.95 V	-200	-	-200	-	µA
		V _{CCI} = 2.7 V	-300	-	-300	-	µA
		V _{CCI} = 3.6 V	-500	-	-500	-	µA
		V _{CCI} = 5.5 V	-900	-	-900	-	µA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CCO} = 1.2 V to 5.5 V [2]	-	±2	-	±10	µA

Table 8. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0$ V to 5.5 V; $V_{CC(A)} = 0$ V; $V_{CC(B)} = 1.2$ V to 5.5 V	-	± 2	-	± 10	μA
		B port; V_I or $V_O = 0$ V to 5.5 V; $V_{CC(B)} = 0$ V; $V_{CC(A)} = 1.2$ V to 5.5 V	-	± 2	-	± 10	μA
I_{CC}	supply current	A port; $V_I = 0$ V or V_{CCI} ; $I_O = 0$ A [1]					
		$V_{CC(A)}, V_{CC(B)} = 1.2$ V to 5.5 V	-	8	-	8	μA
		$V_{CC(A)}, V_{CC(B)} = 1.65$ V to 5.5 V	-	3	-	3	μA
		$V_{CC(A)} = 5.5$ V; $V_{CC(B)} = 0$ V	-	2	-	2	μA
		$V_{CC(A)} = 0$ V; $V_{CC(B)} = 5.5$ V	-2	-	-2	-	μA
		B port; $V_I = 0$ V or V_{CCI} ; $I_O = 0$ A					
		$V_{CC(A)}, V_{CC(B)} = 1.2$ V to 5.5 V	-	8	-	8	μA
		$V_{CC(A)}, V_{CC(B)} = 1.65$ V to 5.5 V	-	3	-	3	μA
		$V_{CC(B)} = 5.5$ V; $V_{CC(A)} = 0$ V	-	2	-	2	μA
		$V_{CC(B)} = 0$ V; $V_{CC(A)} = 5.5$ V	-2	-	-2	-	μA
		A plus B port ($I_{CC(A)} + I_{CC(B)}$); $I_O = 0$ A; $V_I = 0$ V or V_{CCI}					
		$V_{CC(A)}, V_{CC(B)} = 1.2$ V to 5.5 V	-	16	-	16	μA
		$V_{CC(A)}, V_{CC(B)} = 1.65$ V to 5.5 V	-	4	-	4	μA
ΔI_{CC}	additional supply current	$V_{CC(A)}, V_{CC(B)} = 3.0$ V to 5.5 V					
		A port; A port at $V_{CC(A)} - 0.6$ V; DIR at $V_{CC(A)}$; B port = open [4]	-	50	-	75	μA
		DIR input; DIR at $V_{CC(A)} - 0.6$ V; A port at $V_{CC(A)}$ or GND; B port = open	-	50	-	75	μA
		B port; B port at $V_{CC(B)} - 0.6$ V; DIR at GND; A port = open [4]	-	50	-	75	μA

[1] V_{CCI} is the supply voltage associated with the data input port.[2] V_{CCO} is the supply voltage associated with the output port.[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHIO} when the input is in the range V_{IL} to V_{IH} .

[4] For non bus hold parts only (74LVC1T45).

11. Dynamic characteristics

Table 9. Typical dynamic characteristics at $V_{CC(A)} = 1.2\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for waveforms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{PLH}	LOW to HIGH propagation delay	A to B	10.6	8.1	7.0	5.8	5.3	5.1	ns
		B to A	10.6	9.5	9.0	8.5	8.3	8.2	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	10.1	7.1	6.0	5.3	5.2	5.4	ns
		B to A	10.1	8.6	8.1	7.8	7.6	7.6	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	9.4	9.4	9.4	9.4	9.4	9.4	ns
		DIR to B	12.0	9.4	9.0	7.8	8.4	7.9	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	7.1	7.1	7.1	7.1	7.1	7.1	ns
		DIR to B	9.5	7.8	7.7	6.9	7.6	7.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	20.1	17.3	16.7	15.4	15.9	15.2	ns
		DIR to B [1]	17.7	15.2	14.1	12.9	12.4	12.2	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	22.1	18.0	17.1	15.6	16.0	15.5	ns
		DIR to B [1]	19.5	16.5	15.4	14.7	14.6	14.8	ns

[1] t_{PZH} and t_{PZL} are calculated values using the formula shown in [Section 14.4 "Enable times"](#)

Table 10. Typical dynamic characteristics at $V_{CC(B)} = 1.2\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for waveforms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{PLH}	LOW to HIGH propagation delay	A to B	10.6	9.5	9.0	8.5	8.3	8.2	ns
		B to A	10.6	8.1	7.0	5.8	5.3	5.1	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	10.1	8.6	8.1	7.8	7.6	7.6	ns
		B to A	10.1	7.1	6.0	5.3	5.2	5.4	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	9.4	6.5	5.7	4.1	4.1	3.0	ns
		DIR to B	12.0	6.1	5.4	4.6	4.3	4.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	7.1	4.9	4.5	3.2	3.4	2.5	ns
		DIR to B	9.5	7.3	6.6	5.9	5.7	5.6	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	20.1	15.4	13.6	11.7	11.0	10.7	ns
		DIR to B [1]	17.7	14.4	13.5	11.7	11.7	10.7	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	22.1	13.2	11.4	9.9	9.5	9.4	ns
		DIR to B [1]	19.5	15.1	13.8	11.9	11.7	10.6	ns

[1] t_{PZH} and t_{PZL} are calculated values using the formula shown in [Section 14.4 "Enable times"](#)

Table 11. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$ [1][2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$				Unit
			1.8 V	2.5 V	3.3 V	5.5 V	
C_{PD}	power dissipation capacitance	A port: (direction A to B); B port: (direction B to A)	2	3	3	4	pF
		A port: (direction B to A); B port: (direction A to B)	15	16	16	18	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = load capacitance in pF; V_{CC} = supply voltage in V; N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.[2] $f_i = 10\text{ MHz}$; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\text{ }\Omega$.**Table 12. Dynamic characteristics for temperature range $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$** Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	

 $V_{CC(A)} = 1.4\text{ V to }1.6\text{ V}$

t_{PLH}	LOW to HIGH propagation delay	A to B	2.8	21.3	2.4	17.6	2.0	13.5	1.7	11.8	1.6	10.5	ns
		B to A	2.8	21.3	2.6	19.1	2.3	14.9	2.3	12.4	2.2	12.0	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	2.6	19.3	2.2	15.3	1.8	11.8	1.7	10.9	1.7	10.8	ns
		B to A	2.6	19.3	2.4	17.3	2.3	13.2	2.2	11.3	2.3	11.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	3.0	18.7	3.0	18.7	3.0	18.7	3.0	18.7	3.0	18.7	ns
		DIR to B	3.5	24.8	3.5	23.6	3.0	11.0	3.3	11.3	2.8	10.3	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	2.4	11.4	2.4	11.4	2.4	11.4	2.4	11.4	2.4	11.4	ns
		DIR to B	2.8	18.3	3.0	17.2	2.5	9.4	3.0	10.1	2.5	9.4	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	-	39.6	-	36.3	-	24.3	-	22.5	-	21.4	ns
		DIR to B [1]	-	32.7	-	29.0	-	24.9	-	23.2	-	21.9	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	-	44.1	-	40.9	-	24.2	-	22.6	-	21.3	ns
		DIR to B [1]	-	38.0	-	34.0	-	30.5	-	29.6	-	29.5	ns

 $V_{CC(A)} = 1.65\text{ V to }1.95\text{ V}$

t_{PLH}	LOW to HIGH propagation delay	A to B	2.6	19.1	2.2	17.7	2.2	9.3	1.7	7.2	1.4	6.8	ns
		B to A	2.4	17.6	2.2	17.7	2.3	16.0	2.1	15.5	1.9	15.1	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	2.4	17.3	2.0	14.3	1.6	8.5	1.8	7.1	1.7	7.0	ns
		B to A	2.2	15.3	2.0	14.3	2.1	12.9	2.0	12.6	1.8	12.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	2.9	17.1	2.9	17.1	2.9	17.1	2.9	17.1	2.9	17.1	ns
		DIR to B	3.2	24.1	3.2	21.9	2.7	11.5	3.0	10.3	2.5	8.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	2.4	10.5	2.4	10.5	2.4	10.5	2.4	10.5	2.4	10.5	ns
		DIR to B	2.5	17.6	2.6	16.0	2.2	9.2	2.7	8.4	2.4	6.4	ns

Table 12. Dynamic characteristics for temperature range –40 °C to +85 °C ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V _{CC(B)}											Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	-	35.2	-	33.7	-	25.2	-	23.9	-	21.8	ns	
		DIR to B [1]	-	29.6	-	28.2	-	19.8	-	17.7	-	17.3	ns	
t _{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	-	39.4	-	36.2	-	24.4	-	22.9	-	20.4	ns	
		DIR to B [1]	-	34.4	-	31.4	-	25.6	-	24.2	-	24.1	ns	
V _{CC(A)} = 2.3 V to 2.7 V														
t _{PLH}	LOW to HIGH propagation delay	A to B	2.3	17.9	2.3	16.0	1.5	8.5	1.3	6.2	1.1	4.8	ns	
		B to A	2.0	13.5	2.2	9.3	1.5	8.5	1.4	8.0	1.0	7.5	ns	
t _{PHL}	HIGH to LOW propagation delay	A to B	2.3	15.8	2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	ns	
		B to A	1.8	11.8	1.9	8.5	1.4	7.5	1.3	7.0	0.9	6.2	ns	
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	2.1	8.1	2.1	8.1	2.1	8.1	2.1	8.1	2.1	8.1	ns	
		DIR to B	3.0	22.5	3.0	21.4	2.5	11.0	2.8	9.3	2.3	6.9	ns	
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	1.7	5.8	1.7	5.8	1.7	5.8	1.7	5.8	1.7	5.8	ns	
		DIR to B	2.3	14.6	2.5	13.2	2.0	9.0	2.5	8.4	1.8	5.3	ns	
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	-	28.1	-	22.5	-	17.5	-	16.4	-	12.8	ns	
		DIR to B [1]	-	23.7	-	21.8	-	14.3	-	12.0	-	10.6	ns	
t _{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	-	34.3	-	29.9	-	18.5	-	16.3	-	13.1	ns	
		DIR to B [1]	-	23.9	-	21.0	-	15.6	-	13.5	-	12.7	ns	
V _{CC(A)} = 3.0 V to 3.6 V														
t _{PLH}	LOW to HIGH propagation delay	A to B	2.3	17.1	2.1	15.5	1.4	8.0	0.8	5.6	0.7	4.4	ns	
		B to A	1.7	11.8	1.7	7.2	1.3	6.2	0.7	5.6	0.6	5.4	ns	
t _{PHL}	HIGH to LOW propagation delay	A to B	2.2	15.6	2.0	12.6	1.3	7.0	0.8	5.0	0.7	4.0	ns	
		B to A	1.7	10.9	1.8	7.1	1.3	5.4	0.8	5.0	0.7	4.5	ns	
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	2.3	7.3	2.3	7.3	2.3	7.3	2.3	7.3	2.7	7.3	ns	
		DIR to B	2.9	18.0	2.9	16.5	2.3	10.1	2.7	8.6	2.2	6.3	ns	
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	2.0	5.6	2.0	5.6	2.0	5.6	2.0	5.6	2.0	5.6	ns	
		DIR to B	2.3	13.6	2.4	12.5	1.9	7.8	2.3	7.1	1.7	4.9	ns	
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	-	25.4	-	19.7	-	14.0	-	12.7	-	10.3	ns	
		DIR to B [1]	-	22.7	-	21.1	-	13.6	-	11.2	-	10.0	ns	
t _{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	-	28.9	-	23.6	-	15.5	-	13.6	-	10.8	ns	
		DIR to B [1]	-	22.9	-	19.9	-	14.3	-	12.3	-	11.3	ns	
V _{CC(A)} = 4.5 V to 5.5 V														
t _{PLH}	LOW to HIGH propagation delay	A to B	2.2	16.6	1.9	15.1	1.0	7.5	0.7	5.4	0.5	3.9	ns	
		B to A	1.6	10.5	1.4	6.8	1.0	4.8	0.7	4.4	0.5	3.9	ns	
t _{PHL}	HIGH to LOW propagation delay	A to B	2.3	15.3	1.8	12.2	1.0	6.2	0.7	4.5	0.5	3.5	ns	
		B to A	1.7	10.8	1.7	7.0	0.9	4.6	0.7	4.0	0.5	3.5	ns	
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	1.7	5.4	1.7	5.4	1.7	5.4	1.7	5.4	1.7	5.4	ns	
		DIR to B	2.9	17.3	2.9	16.1	2.3	9.7	2.7	8.0	2.5	5.7	ns	

Table 12. Dynamic characteristics for temperature range –40 °C to +85 °C ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	1.4	3.7	1.4	3.7	1.3	3.7	1.0	3.7	0.9	3.7	ns
		DIR to B	2.3	13.1	2.4	12.1	1.9	7.4	2.3	7.0	1.8	4.5	ns
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	-	23.6	-	18.9	-	12.2	-	11.4	-	8.4	ns
		DIR to B [1]	-	20.3	-	18.8	-	11.2	-	9.1	-	7.6	ns
t _{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	-	28.1	-	23.1	-	14.3	-	12.0	-	9.2	ns
		DIR to B [1]	-	20.7	-	17.6	-	11.6	-	9.9	-	8.9	ns

[1] t_{PZH} and t_{PZL} are calculated values using the formula shown in [Section 14.4 "Enable times"](#)**Table 13. Dynamic characteristics for temperature range –40 °C to +125 °C**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	

V_{CC(A)} = 1.4 V to 1.6 V

t _{PLH}	LOW to HIGH propagation delay	A to B	2.5	23.5	2.1	19.4	1.8	14.9	1.5	13.0	1.4	11.6	ns
		B to A	2.5	23.5	2.3	21.1	2.0	16.4	2.0	13.7	1.9	13.2	ns
t _{PHL}	HIGH to LOW propagation delay	A to B	2.3	21.3	1.9	16.9	1.6	13.0	1.5	12.0	1.5	11.9	ns
		B to A	2.3	21.3	2.1	19.1	2.0	14.6	1.9	12.5	2.0	12.1	ns
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	2.7	20.6	2.7	20.6	2.7	20.6	2.7	20.6	2.7	20.6	ns
		DIR to B	3.1	27.3	3.1	26.0	2.7	12.1	2.9	12.5	2.5	11.4	ns
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	2.1	12.6	2.1	12.6	2.1	12.6	2.1	12.6	2.1	12.6	ns
		DIR to B	2.5	20.2	2.7	19.0	2.2	10.4	2.7	11.2	2.2	10.4	ns
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	-	43.7	-	40.1	-	26.8	-	24.9	-	23.6	ns
		DIR to B [1]	-	36.1	-	32.0	-	27.5	-	25.6	-	24.2	ns
t _{PZL}	OFF-state to LOW propagation delay	DIR to A [1]	-	48.6	-	45.1	-	26.7	-	25.0	-	23.5	ns
		DIR to B [1]	-	41.9	-	37.5	-	33.6	-	32.6	-	32.5	ns

V_{CC(A)} = 1.65 V to 1.95 V

t _{PLH}	LOW to HIGH propagation delay	A to B	2.3	21.1	1.9	19.5	1.9	10.3	1.5	8.0	1.2	7.5	ns
		B to A	2.1	19.4	1.9	19.5	2.0	17.6	1.8	17.1	1.7	16.7	ns
t _{PHL}	HIGH to LOW propagation delay	A to B	2.1	19.1	1.8	15.8	1.4	9.4	1.6	7.9	1.5	7.7	ns
		B to A	1.9	16.9	1.8	15.8	1.8	14.2	1.8	13.9	1.6	13.5	ns
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	2.6	18.9	2.6	18.9	2.6	18.9	2.6	18.9	2.6	18.9	ns
		DIR to B	2.8	26.6	2.8	24.1	2.4	12.7	2.7	11.4	2.2	9.1	ns
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	2.1	11.6	2.1	11.6	2.1	11.6	2.1	11.6	2.1	11.6	ns
		DIR to B	2.2	19.4	2.3	17.6	1.9	10.2	2.4	9.3	2.1	7.4	ns
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A [1]	-	38.8	-	37.1	-	27.8	-	26.4	-	24.1	ns
		DIR to B [1]	-	32.7	-	31.1	-	21.9	-	19.6	-	19.1	ns

Table 13. Dynamic characteristics for temperature range –40 °C to +125 °C ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V _{CC(B)}											Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t _{PZL}	OFF-state to LOW propagation delay	DIR to A (1)	-	43.5	-	39.9	-	26.9	-	25.3	-	22.6	ns	
		DIR to B (1)	-	38.0	-	34.7	-	28.3	-	26.8	-	26.6	ns	
V _{CC(A)} = 2.3 V to 2.7 V														
t _{PLH}	LOW to HIGH propagation delay	A to B	2.0	19.7	2.0	17.6	1.3	9.4	1.1	6.9	0.9	5.3	ns	
		B to A	1.8	14.9	1.9	10.3	1.3	9.4	1.2	8.8	0.9	8.3	ns	
t _{PHL}	HIGH to LOW propagation delay	A to B	2.0	17.4	1.8	14.2	1.2	8.3	1.1	6.0	0.8	5.1	ns	
		B to A	1.6	13.0	1.7	9.4	1.2	8.3	1.1	7.7	0.8	6.9	ns	
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	1.8	9.0	1.8	9.0	1.8	9.0	1.8	9.0	1.8	9.0	ns	
		DIR to B	2.7	24.8	2.7	23.6	2.2	12.1	2.5	10.3	2.0	7.6	ns	
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	1.5	6.4	1.5	6.4	1.5	6.4	1.5	6.4	1.5	6.4	ns	
		DIR to B	2.0	16.1	2.2	14.6	1.8	9.9	2.2	9.3	1.6	5.9	ns	
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A (1)	-	31.0	-	24.9	-	19.3	-	18.1	-	14.2	ns	
		DIR to B (1)	-	26.1	-	24.0	-	15.8	-	13.3	-	11.7	ns	
t _{PZL}	OFF-state to LOW propagation delay	DIR to A (1)	-	37.8	-	33.0	-	20.4	-	18.0	-	14.5	ns	
		DIR to B (1)	-	26.4	-	23.2	-	17.3	-	15.0	-	14.1	ns	
V _{CC(A)} = 3.0 V to 3.6 V														
t _{PLH}	LOW to HIGH propagation delay	A to B	2.0	18.9	1.8	17.1	1.2	8.8	0.7	6.2	0.6	4.9	ns	
		B to A	1.5	13.0	1.5	8.0	1.1	6.9	0.6	6.2	0.5	6.0	ns	
t _{PHL}	HIGH to LOW propagation delay	A to B	1.9	17.2	1.8	13.9	1.1	7.7	0.7	5.5	0.6	4.4	ns	
		B to A	1.5	12.0	1.6	7.9	1.1	6.0	0.7	5.5	0.6	5.0	ns	
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	2.0	8.1	2.0	8.1	2.0	8.1	2.0	8.1	2.4	8.1	ns	
		DIR to B	2.6	19.8	2.6	18.2	2.0	11.2	2.4	9.5	1.9	7.0	ns	
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	1.8	6.2	1.8	6.2	1.8	6.2	1.8	6.2	1.8	6.2	ns	
		DIR to B	2.0	15.0	2.1	13.8	1.7	8.6	2.0	7.9	1.5	5.4	ns	
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A (1)	-	28.0	-	21.8	-	15.5	-	14.1	-	11.4	ns	
		DIR to B (1)	-	25.1	-	23.3	-	15.0	-	12.4	-	11.1	ns	
t _{PZL}	OFF-state to LOW propagation delay	DIR to A (1)	-	31.8	-	26.1	-	17.2	-	15.0	-	12.0	ns	
		DIR to B (1)	-	25.3	-	22.0	-	15.8	-	13.6	-	12.5	ns	
V _{CC(A)} = 4.5 V to 5.5 V														
t _{PLH}	LOW to HIGH propagation delay	A to B	1.9	18.3	1.7	16.7	0.9	8.3	0.6	6.0	0.4	4.3	ns	
		B to A	1.4	11.6	1.2	7.5	0.9	5.3	0.6	4.9	0.4	4.3	ns	
t _{PHL}	HIGH to LOW propagation delay	A to B	2.0	16.9	1.6	13.5	0.9	6.9	0.6	5.0	0.4	3.9	ns	
		B to A	1.5	11.9	1.5	7.7	0.8	5.1	0.6	4.4	0.4	3.9	ns	
t _{PHZ}	HIGH to OFF-state propagation delay	DIR to A	1.5	6.0	1.5	6.0	1.5	6.0	1.5	6.0	1.5	6.0	ns	
		DIR to B	2.6	19.1	2.6	17.8	2.0	10.7	2.4	8.8	2.2	6.3	ns	
t _{PLZ}	LOW to OFF-state propagation delay	DIR to A	1.2	4.1	1.2	4.1	1.1	4.1	0.9	4.1	0.8	4.1	ns	
		DIR to B	2.0	14.5	2.1	13.4	1.7	8.2	2.0	7.7	1.6	5.0	ns	

Table 13. Dynamic characteristics for temperature range –40 °C to +125 °C ...continued
Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V _{CC(B)}											Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	
t _{PZH}	OFF-state to HIGH propagation delay	DIR to A 1	-	26.1	-	20.9	-	13.5	-	12.6	-	9.3	ns	
		DIR to B 1	-	22.4	-	20.8	-	12.4	-	10.1	-	8.4	ns	
t _{PZL}	OFF-state to LOW propagation delay	DIR to A 1	-	31.0	-	25.5	-	15.8	-	13.2	-	10.2	ns	
		DIR to B 1	-	22.9	-	19.5	-	12.9	-	11.0	-	9.9	ns	

[1] t_{PZH} and t_{PZL} are calculated values using the formula shown in [Section 14.4 “Enable times”](#)

12. Waveforms

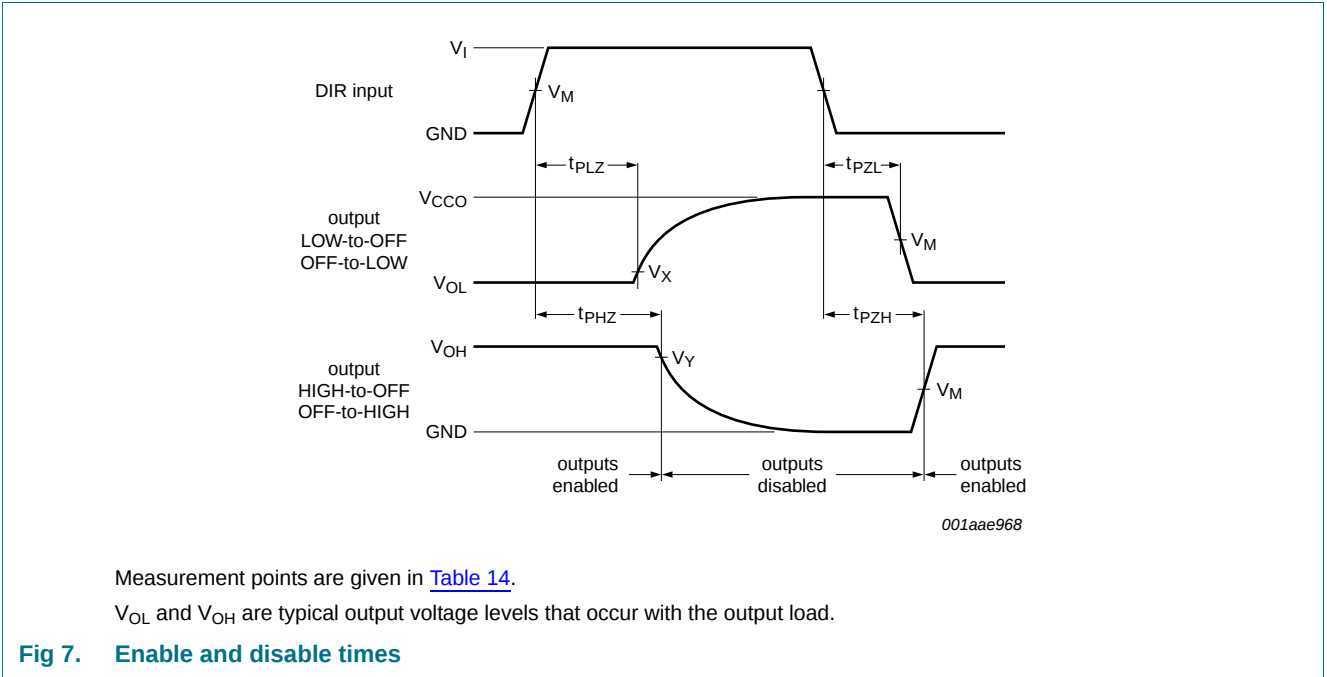
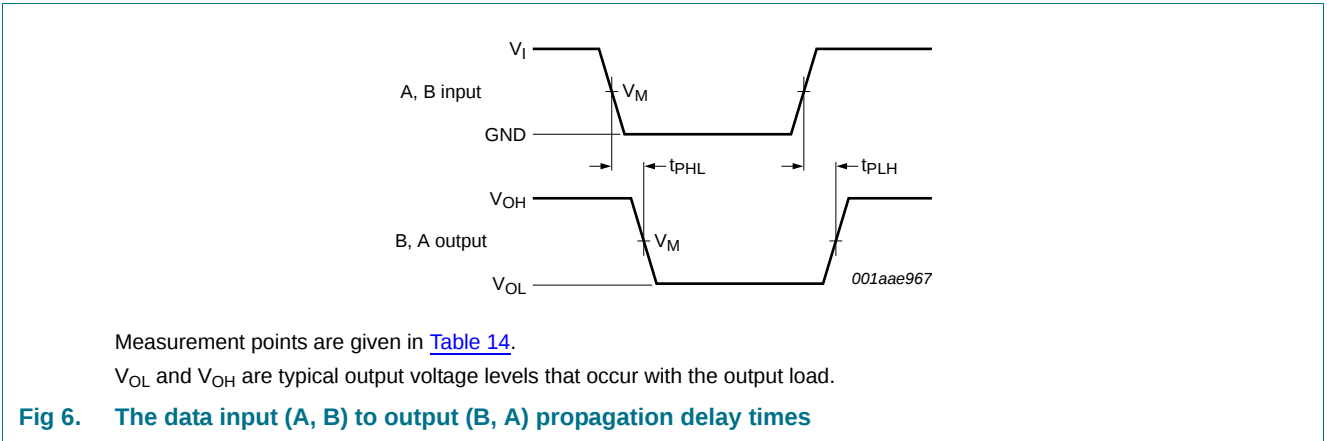
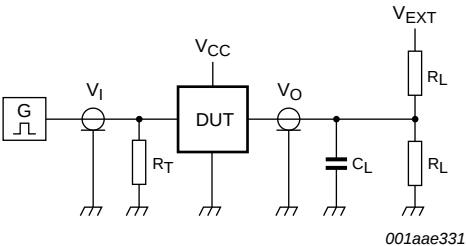
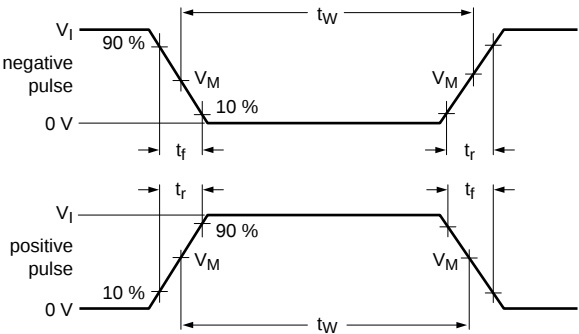


Table 14. Measurement points

Supply voltage	Input ^[1]	Output ^[2]		
V _{CC(A)} , V _{CC(B)}	V _M	V _M	V _X	V _Y
1.2 V to 1.6 V	0.5V _{CCI}	0.5V _{CCO}	V _{OL} + 0.1 V	V _{OH} – 0.1 V
1.65 V to 2.7 V	0.5V _{CCI}	0.5V _{CCO}	V _{OL} + 0.15 V	V _{OH} – 0.15 V
3.0 V to 5.5 V	0.5V _{CCI}	0.5V _{CCO}	V _{OL} + 0.3 V	V _{OH} – 0.3 V

- [1] V_{CCI} is the supply voltage associated with the data input port.
- [2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in [Table 15](#).

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance.

V_{EXT} = External voltage for measuring switching times.

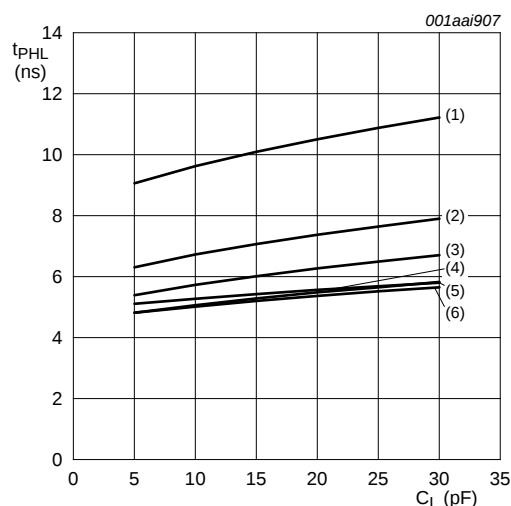
Fig 8. Test circuit for measuring switching times

Table 15. Test data

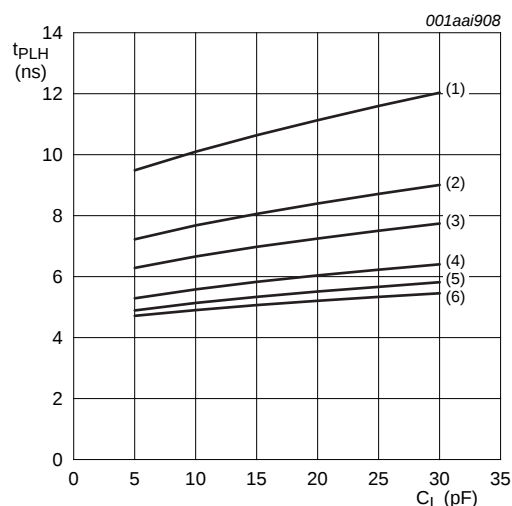
Supply voltage	Input		Load		V _{EXT}		
V _{CC(A)} , V _{CC(B)}	V _I ^[1]	Δt/ΔV ^[2]	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ} ^[3]
1.2 V to 5.5 V	V _{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	2V _{CCO}

- [1] V_{CCI} is the supply voltage associated with the data input port.
- [2] dV/dt ≥ 1.0 V/ns
- [3] V_{CCO} is the supply voltage associated with the output port.

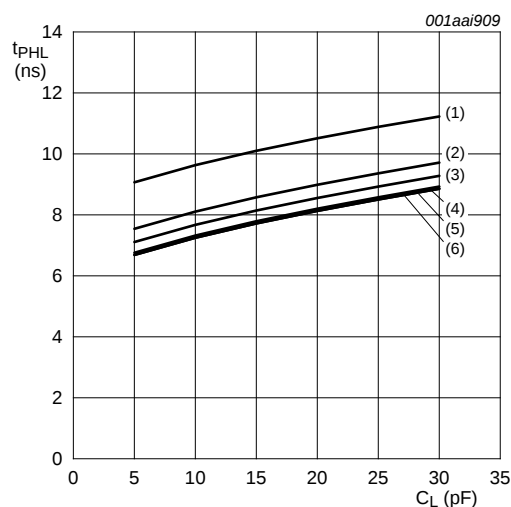
13. Typical propagation delay characteristics



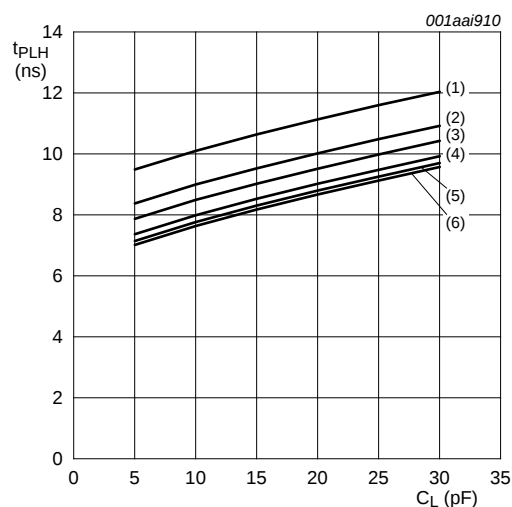
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



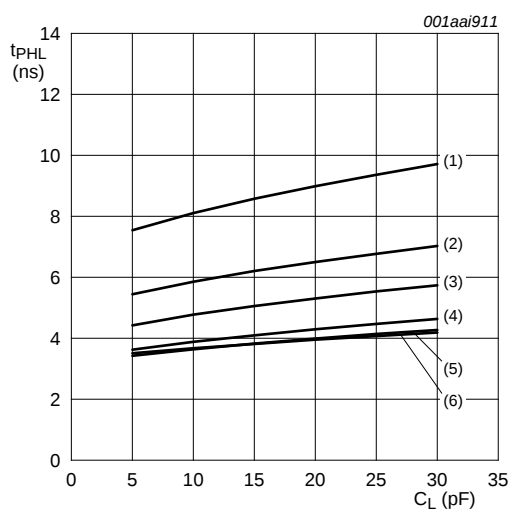
c. HIGH to LOW propagation delay (B to A)



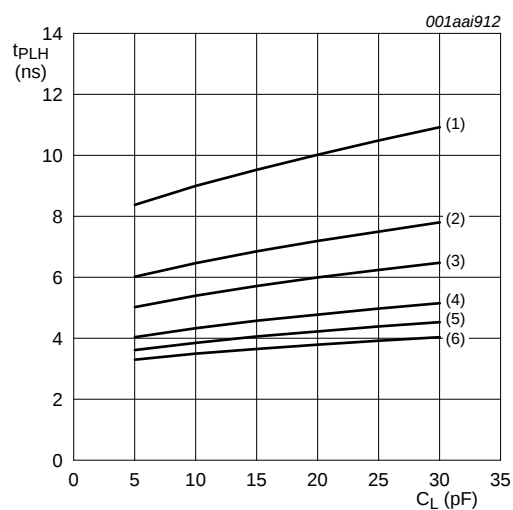
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2$ V.
- (2) $V_{CC(B)} = 1.5$ V.
- (3) $V_{CC(B)} = 1.8$ V.
- (4) $V_{CC(B)} = 2.5$ V.
- (5) $V_{CC(B)} = 3.3$ V.
- (6) $V_{CC(B)} = 5.0$ V.

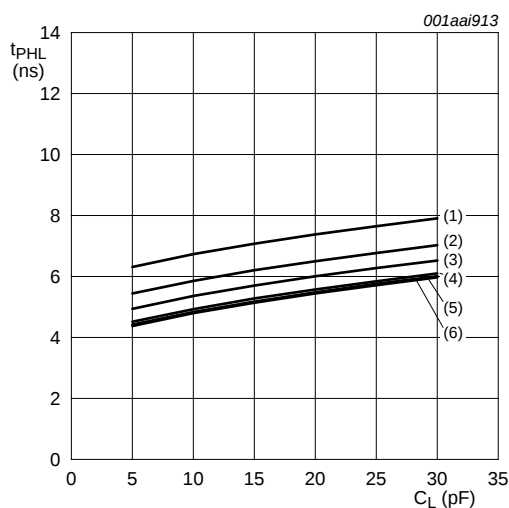
Fig 9. Typical propagation delay vs load capacitance; $T_{amb} = 25$ °C; $V_{CC(A)} = 1.2$ V



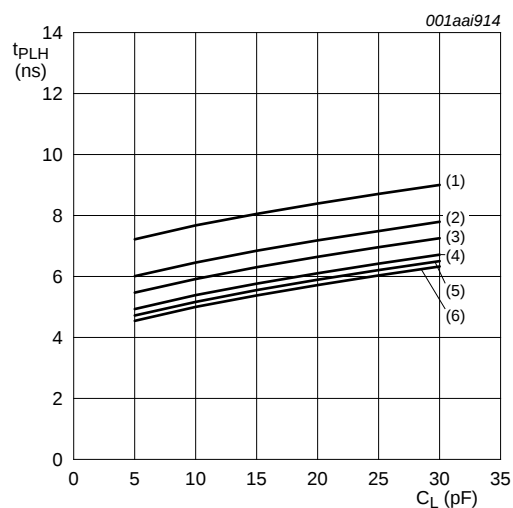
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



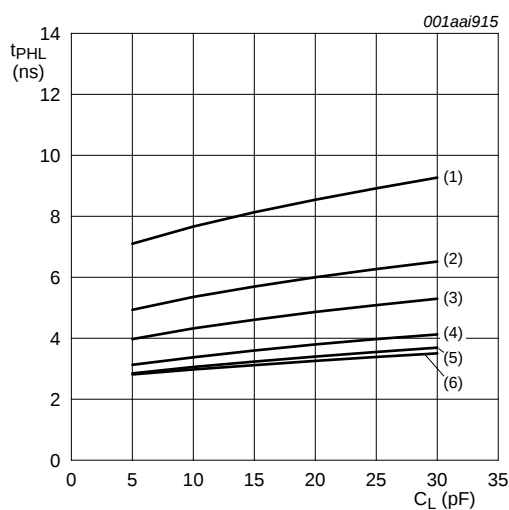
c. HIGH to LOW propagation delay (B to A)



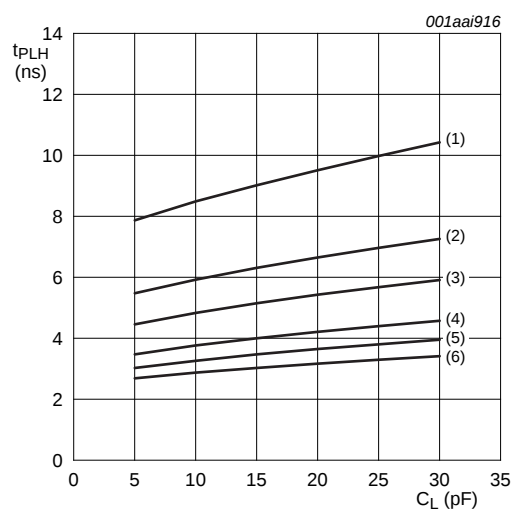
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.
- (6) $V_{CC(B)} = 5.0 \text{ V}$.

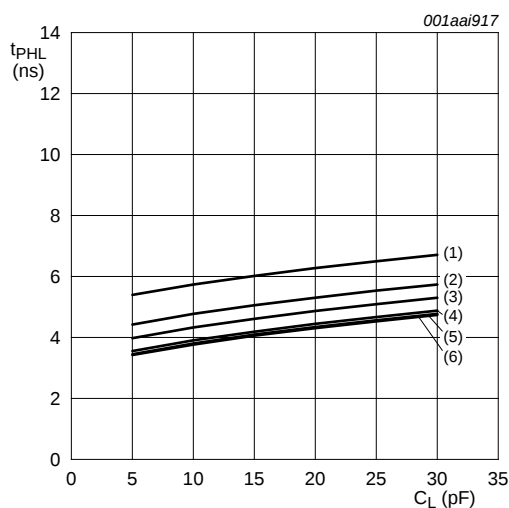
Fig 10. Typical propagation delay vs load capacitance; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $V_{CC(A)} = 1.5 \text{ V}$



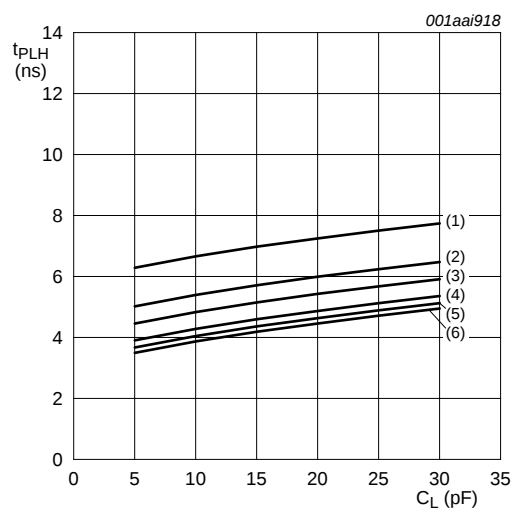
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



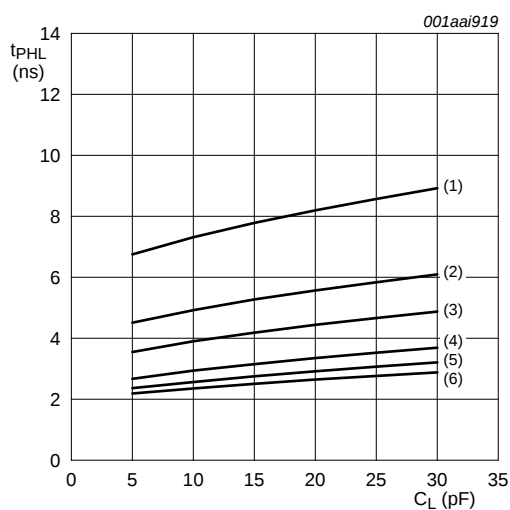
c. HIGH to LOW propagation delay (B to A)



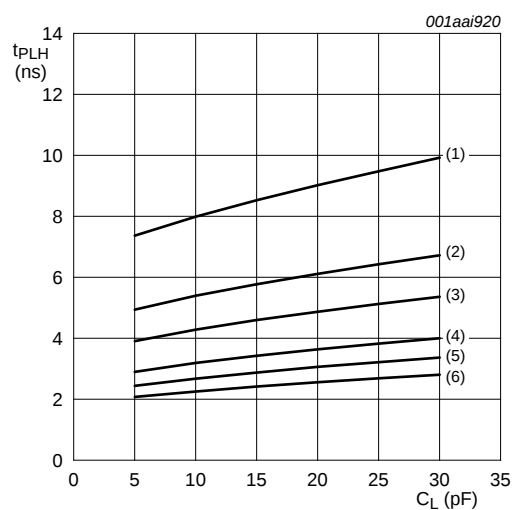
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.
- (6) $V_{CC(B)} = 5.0 \text{ V}$.

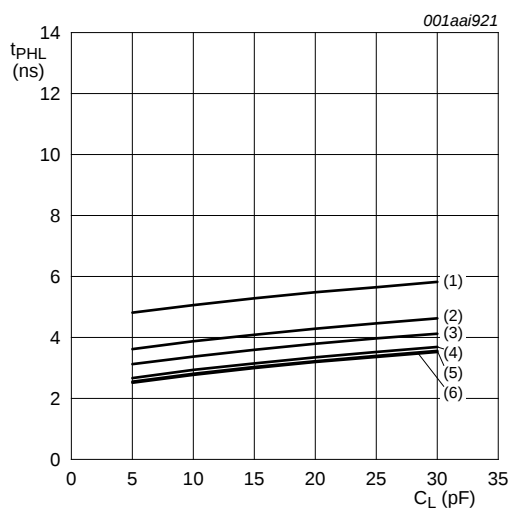
Fig 11. Typical propagation delay vs load capacitance; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $V_{CC(A)} = 1.8 \text{ V}$



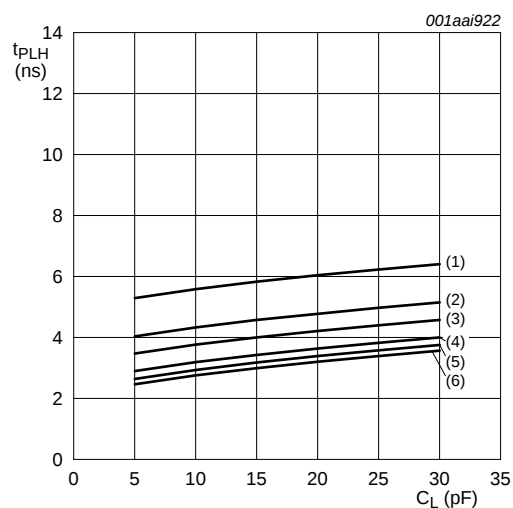
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



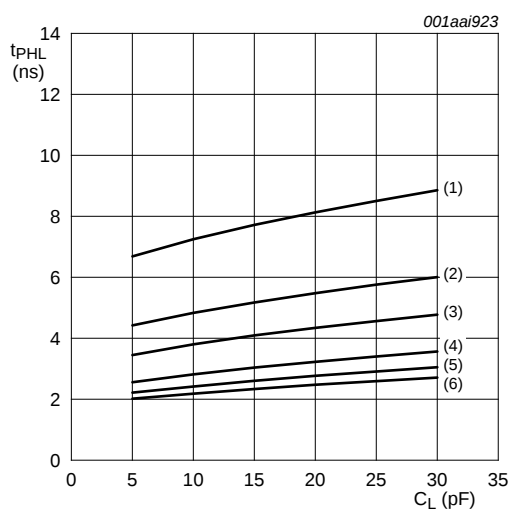
c. HIGH to LOW propagation delay (B to A)



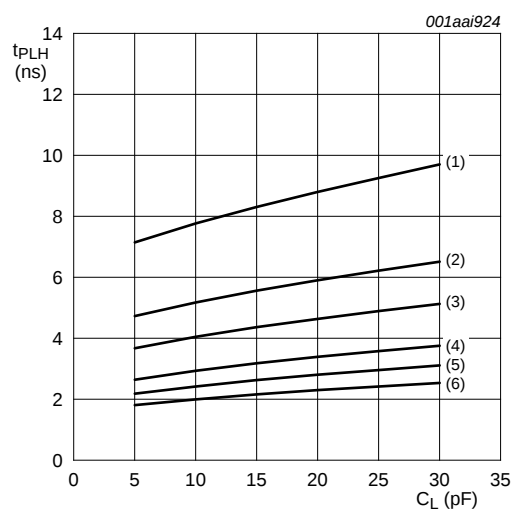
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.
- (6) $V_{CC(B)} = 5.0 \text{ V}$.

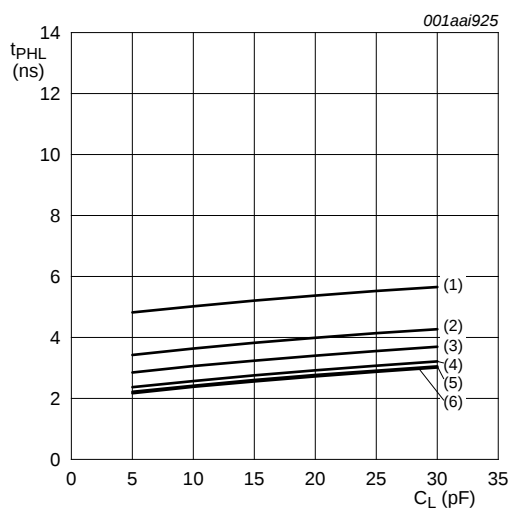
Fig 12. Typical propagation delay vs load capacitance; $T_{amb} = 25^\circ\text{C}$; $V_{CC(A)} = 2.5 \text{ V}$



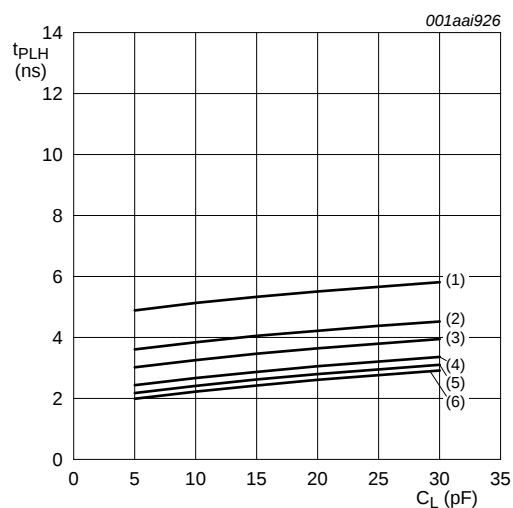
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



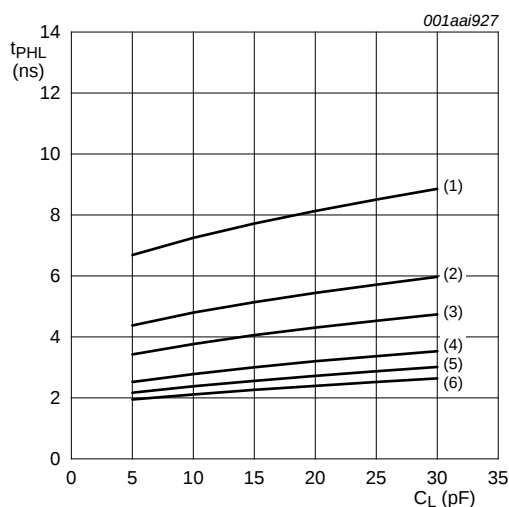
c. HIGH to LOW propagation delay (B to A)



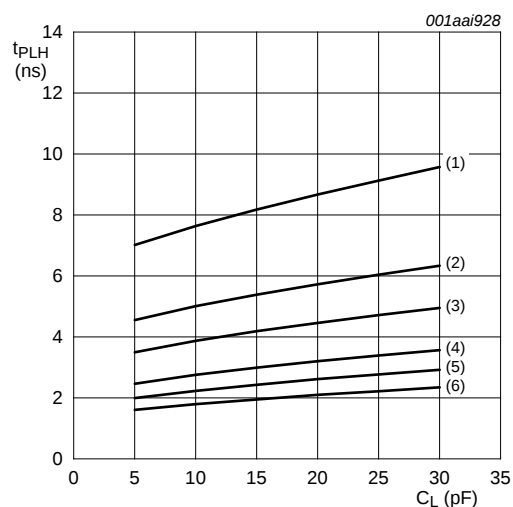
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.
- (6) $V_{CC(B)} = 5.0 \text{ V}$.

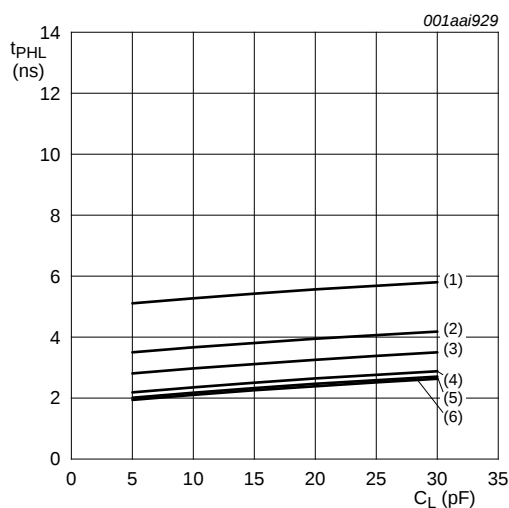
Fig 13. Typical propagation delay vs load capacitance; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $V_{CC(A)} = 3.3 \text{ V}$



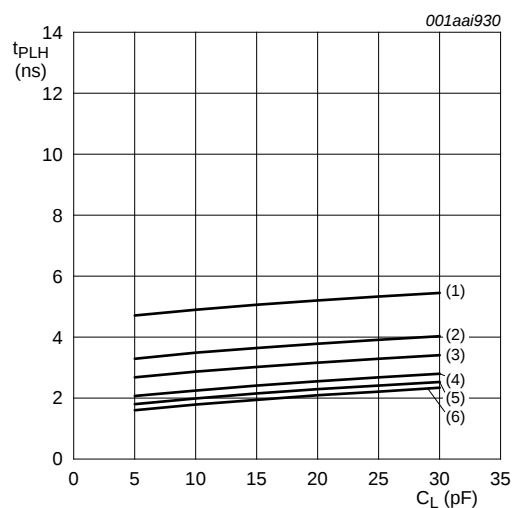
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



c. HIGH to LOW propagation delay (B to A)



d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.
- (6) $V_{CC(B)} = 5.0 \text{ V}$.

Fig 14. Typical propagation delay vs load capacitance; $T_{amb} = 25^\circ\text{C}$; $V_{CC(A)} = 5 \text{ V}$

14. Application information

14.1 Unidirectional logic level-shifting application

The circuit given in [Figure 15](#) is an example of the 74LVC1T45; 74LVCH1T45 being used in a unidirectional logic level-shifting application.

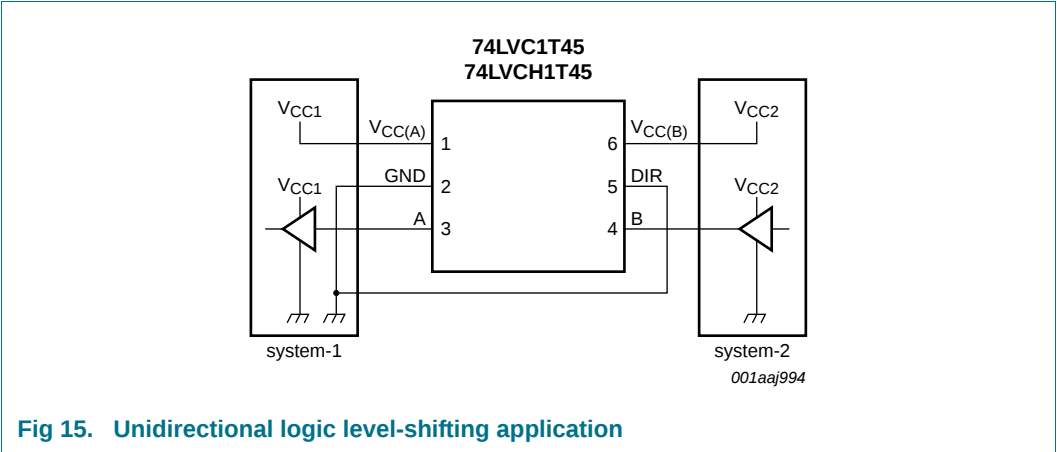


Table 16. Description unidirectional logic level-shifting application

Pin	Name	Function	Description
1	V _{CC(A)}	V _{CC1}	supply voltage of system-1 (1.2 V to 5.5 V)
2	GND	GND	device GND
3	A	OUT	output level depends on V _{CC1} voltage
4	B	IN	input threshold value depends on V _{CC2} voltage
5	DIR	DIR	the GND (LOW level) determines B port to A port direction
6	V _{CC(B)}	V _{CC2}	supply voltage of system-2 (1.2 V to 5.5 V)

14.2 Bidirectional logic level-shifting application

Figure 16 shows the 74LVC1T45; 74LVCH1T45 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.

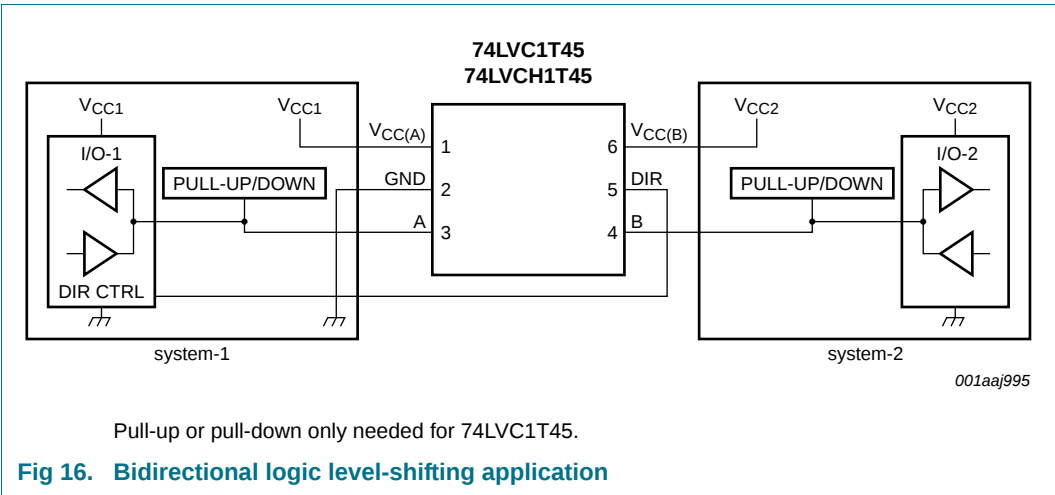


Table 17 provides a sequence that illustrates data transmission from system-1 to system-2 and then from system-2 to system-1.

Table 17. Description bidirectional logic level-shifting application^[1]

State	DIR CTRL	I/O-1	I/O-2	Description
1	H	output	input	system-1 data to system-2
2	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 are still disabled. The bus-line state depends on bus hold.
4	L	input	output	system-2 data to system-1

[1] H = HIGH voltage level;
 L = LOW voltage level;
 Z = high-impedance OFF-state.

14.3 Power-up considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

Table 18. Typical total supply current ($I_{CC(A)} + I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$					Unit
	0 V	1.8 V	2.5 V	3.3 V	5.0 V	
0 V	0	< 1	< 1	< 1	< 1	μA
1.8 V	< 1	< 2	< 2	< 2	2	μA
2.5 V	< 1	< 2	< 2	< 2	< 2	μA
3.3 V	< 1	< 2	< 2	< 2	< 2	μA
5.0 V	< 1	2	< 2	< 2	< 2	μA

14.4 Enable times

Calculate the enable times for the 74LVC1T45; 74LVCH1T45 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the 74LVC1T45; 74LVCH1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

15. Package outline

Plastic surface-mounted package; 6 leadsSOT363

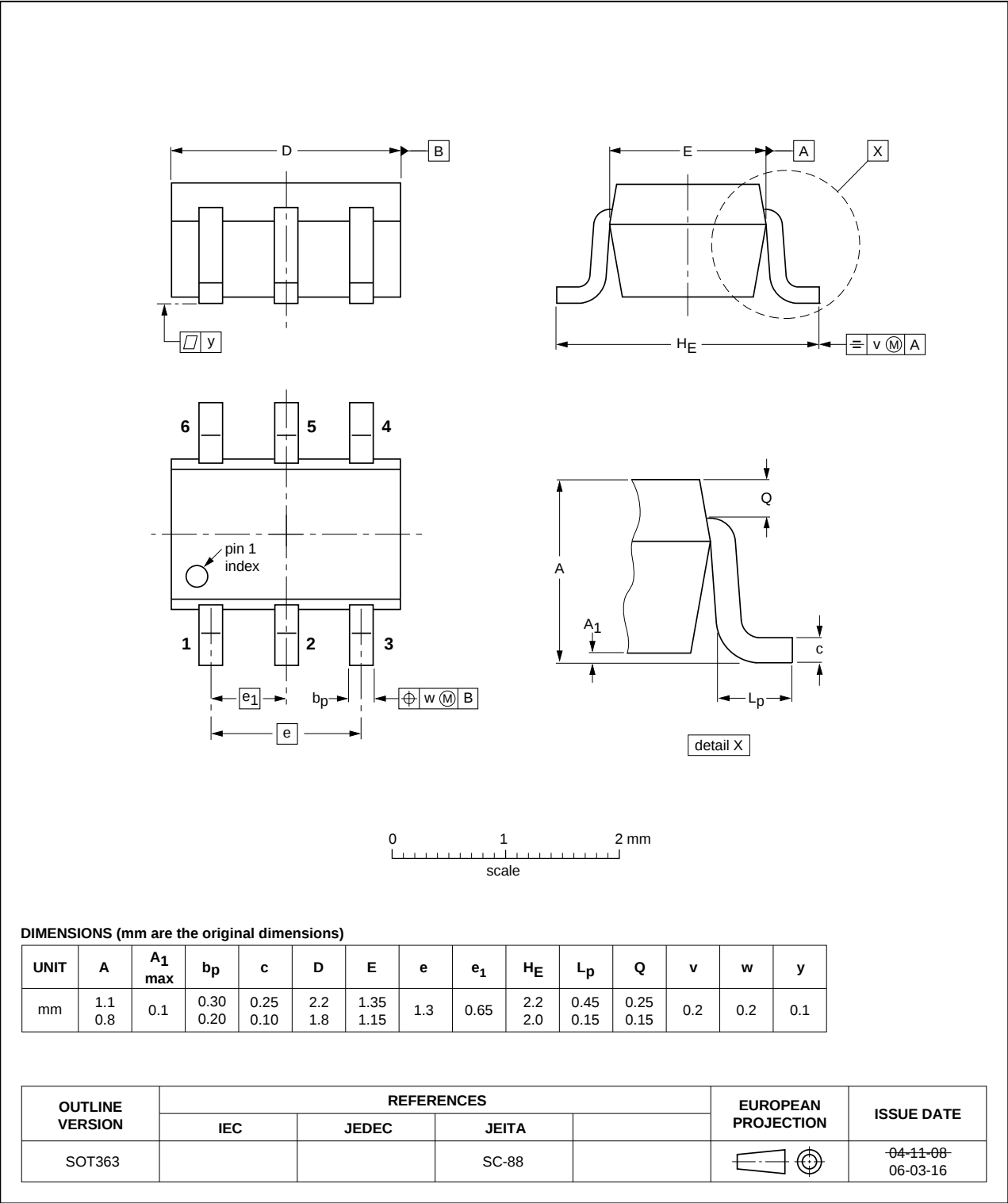


Fig 17. Package outline SOT363 (SC-88)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

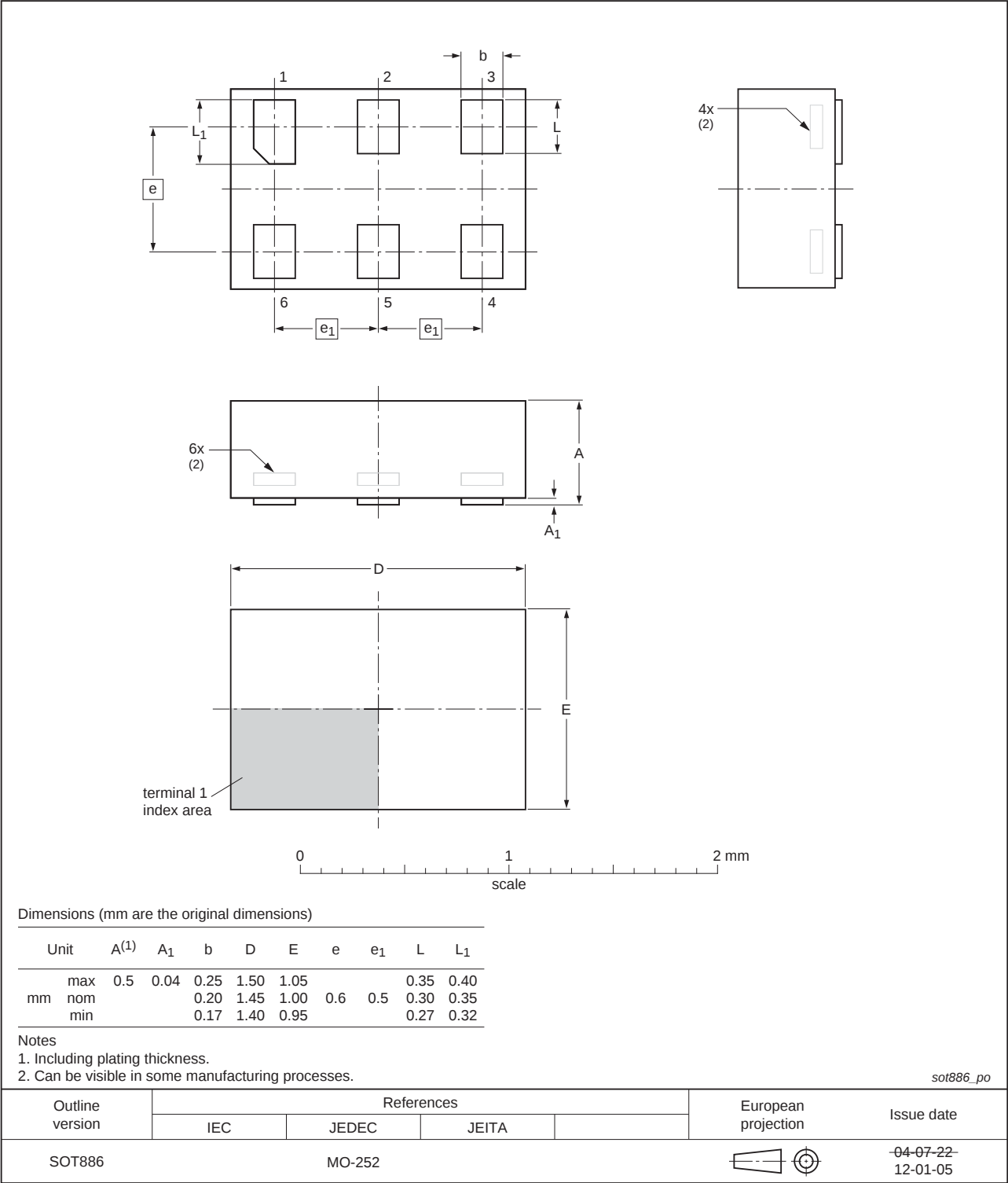


Fig 18. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

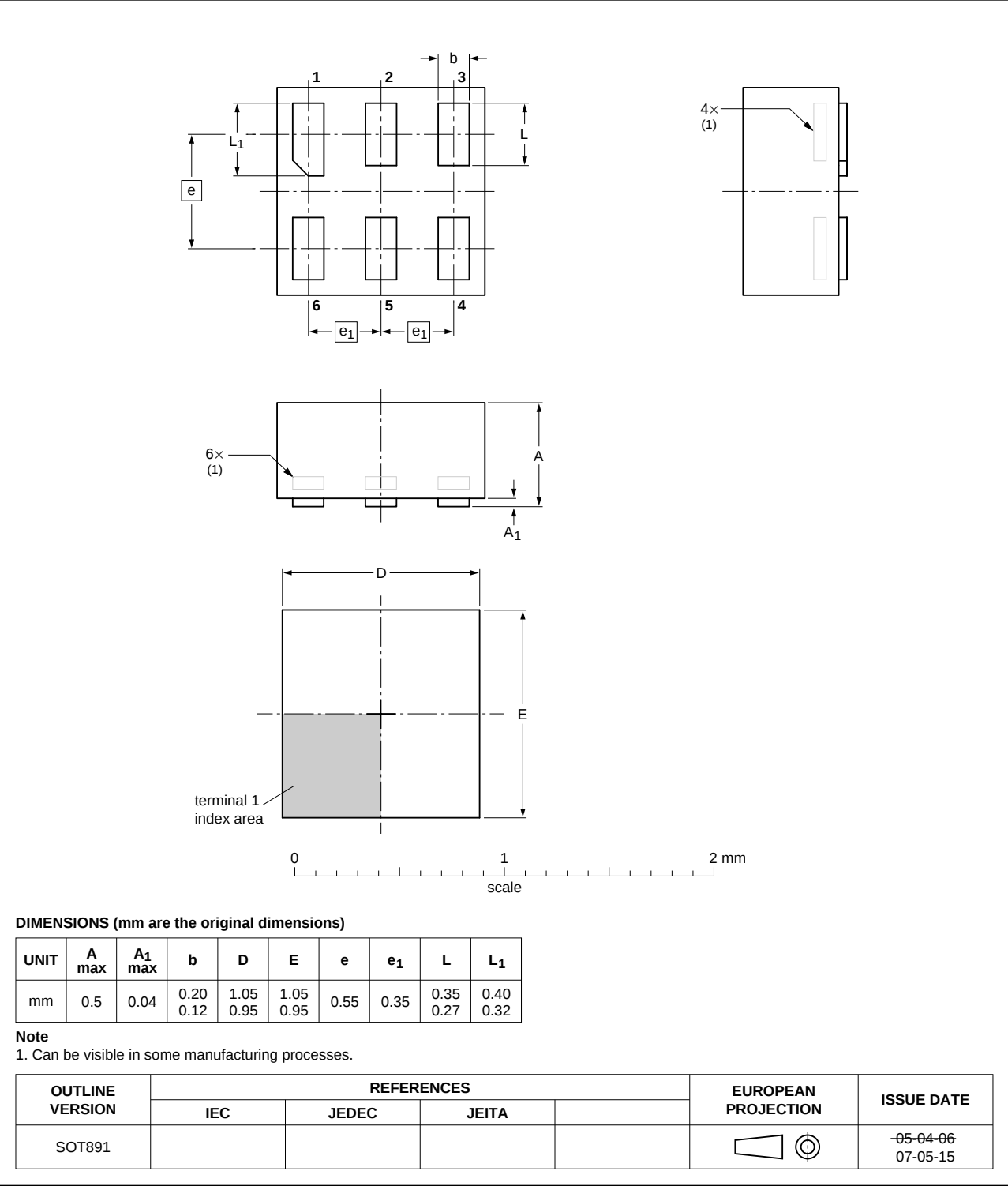


Fig 19. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115

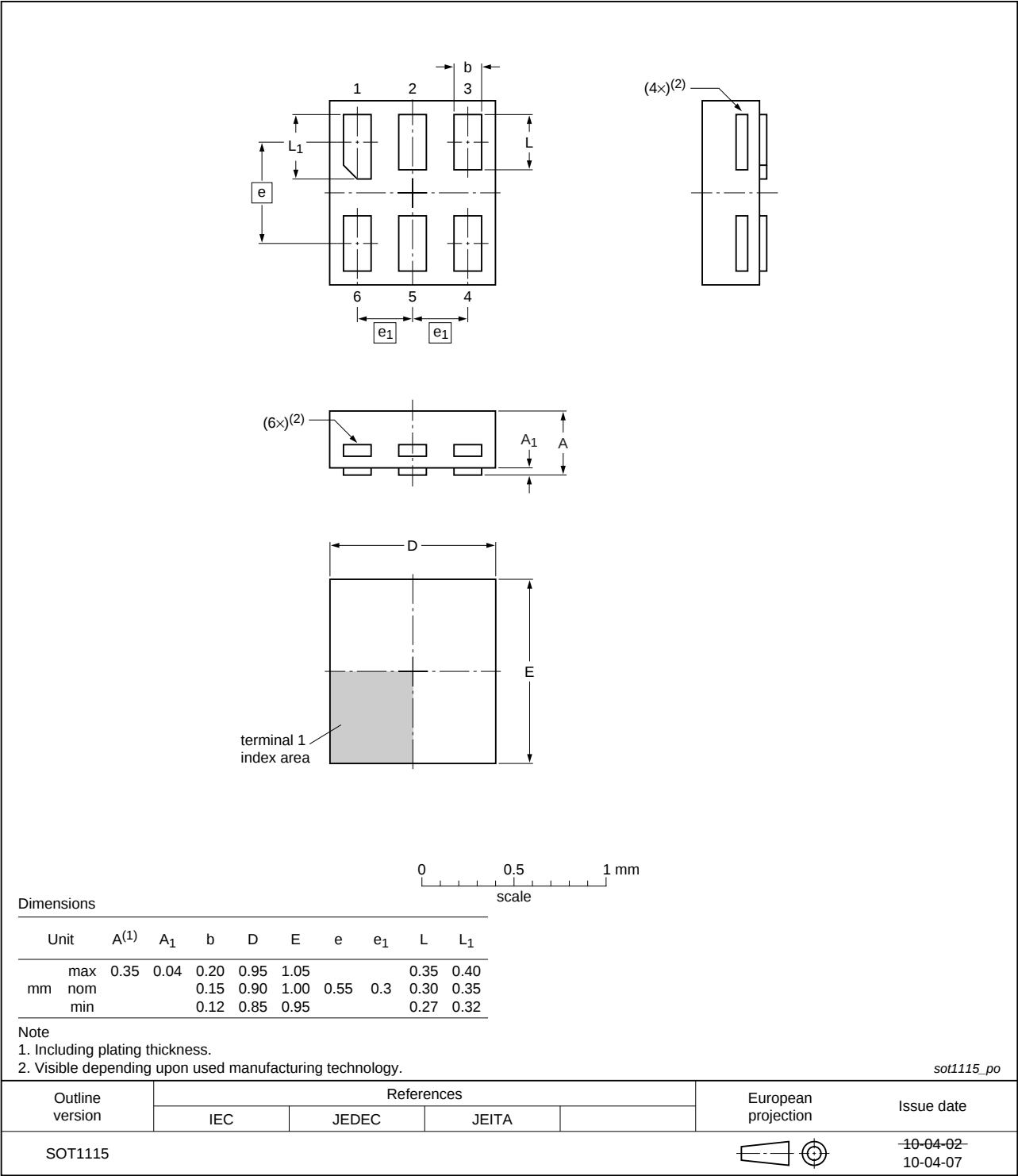


Fig 20. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202

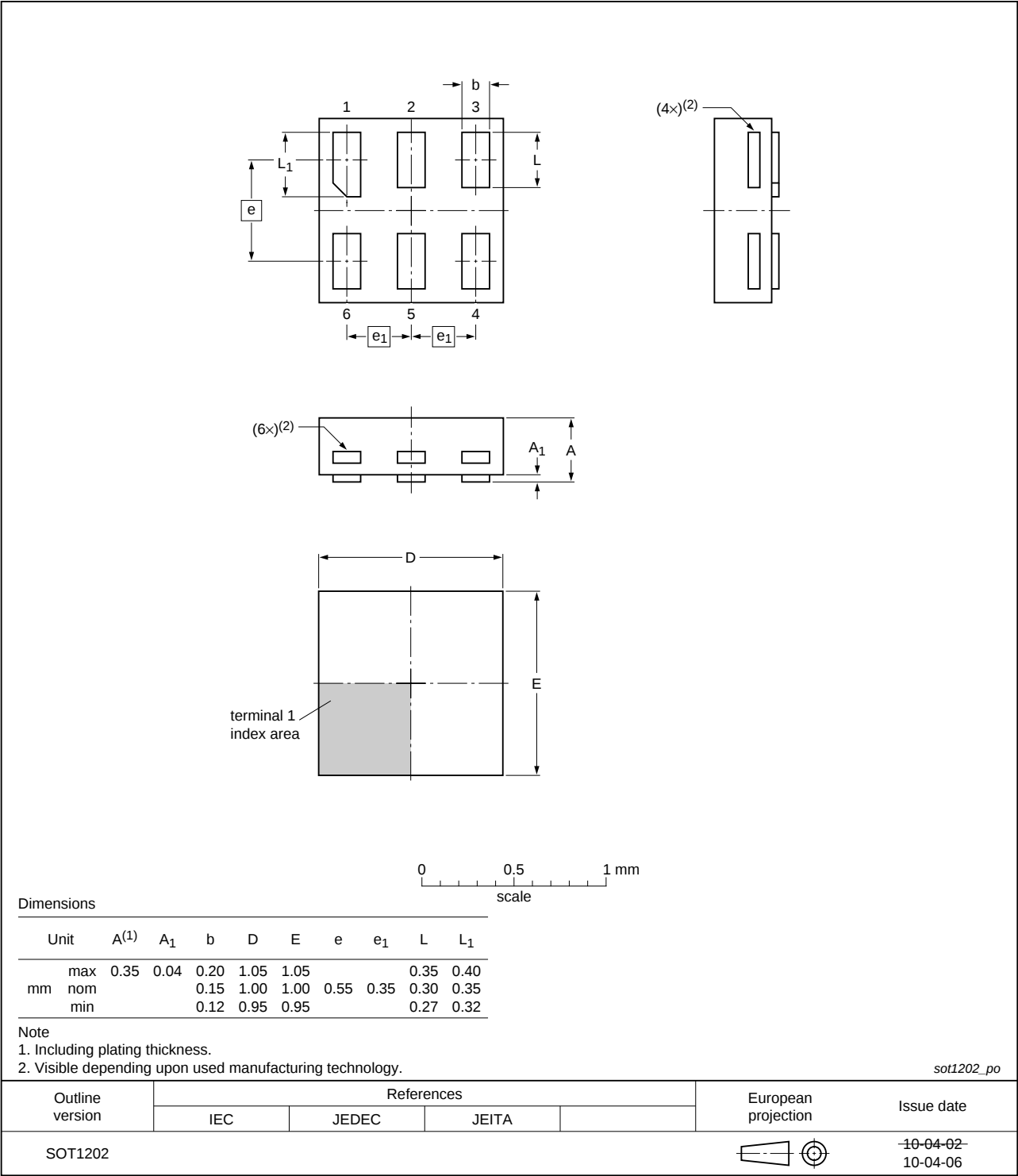


Fig 21. Package outline SOT1202 (XSON6)

16. Abbreviations

Table 19. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

17. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH1T45 v.6	20120806	Product data sheet	-	74LVC_LVCH1T45 v.5
Modifications:	• Package outline drawing of SOT886 (Figure 18) modified.			
74LVC_LVCH1T45 v.5	20111219	Product data sheet	-	74LVC_LVCH1T45 v.4
Modifications:	• Legal pages updated.			
74LVC_LVCH1T45 v.4	20110927	Product data sheet	-	74LVC_LVCH1T45 v.3
74LVC_LVCH1T45 v.3	20100819	Product data sheet	-	74LVC_LVCH1T45 v.2
74LVC_LVCH1T45 v.2	20100119	Product data sheet	-	74LVC_LVCH1T45 v.1
74LVC_LVCH1T45 v.1	20090511	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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20. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	3
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
8	Limiting values	4
9	Recommended operating conditions	4
10	Static characteristics	5
11	Dynamic characteristics	9
12	Waveforms	14
13	Typical propagation delay characteristics ..	16
14	Application information	22
14.1	Unidirectional logic level-shifting application ..	22
14.2	Bidirectional logic level-shifting application. .	23
14.3	Power-up considerations	24
14.4	Enable times	24
15	Package outline	25
16	Abbreviations	30
17	Revision history	30
18	Legal information	31
18.1	Data sheet status	31
18.2	Definitions	31
18.3	Disclaimers	31
18.4	Trademarks	32
19	Contact information	32
20	Contents	33

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