



BUK9612-55B

N-channel TrenchMOS logic level FET

Rev. 02 — 4 June 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	[1]	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	157	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$	-	9	10	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11 ; see Figure 12	-	10.2	12	mΩ

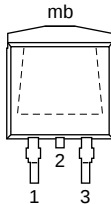
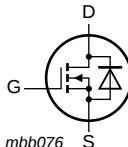
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 5\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; unclamped	-	-	172	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 44\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; see Figure 13	-	12	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		
SOT404 (D2PAK)				

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9612-55B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	55	V	
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	-	55	V	
V _{GS}	gate-source voltage		-15	-	15	V	
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; see Figure 1 ; see Figure 3	[1]	-	-	75	A
			[2]	-	-	79	A
		T _{mb} = 100 °C; V _{GS} = 5 V; see Figure 1	[2]	-	-	56	A
I _{DM}	peak drain current	T _{mb} = 25 °C; t _p ≤ 10 μs; pulsed; see Figure 3	-	-	322	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	157	W	
T _{stg}	storage temperature		-55	-	175	°C	
T _j	junction temperature		-55	-	175	°C	
Source-drain diode							
I _S	source current	T _{mb} = 25 °C	[1]	-	-	75	A
			[2]	-	-	79	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	-	322	A	
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 75 A; V _{sup} ≤ 55 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped	-	-	172	mJ	

[1] Continuous current is limited by package.

[2] Current is limited by power dissipation chip rating.

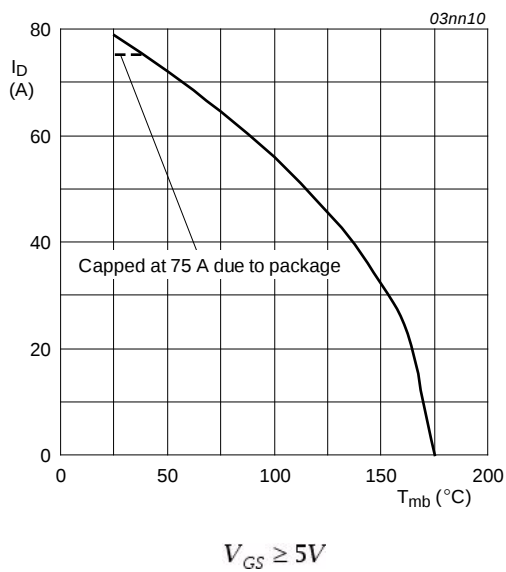


Fig 1. Normalized continuous drain current as a function of mounting base temperature

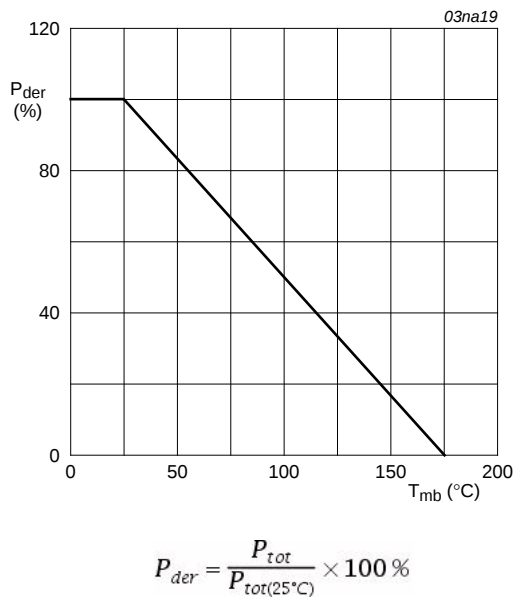


Fig 2. Normalized total power dissipation as a function of mounting base temperature

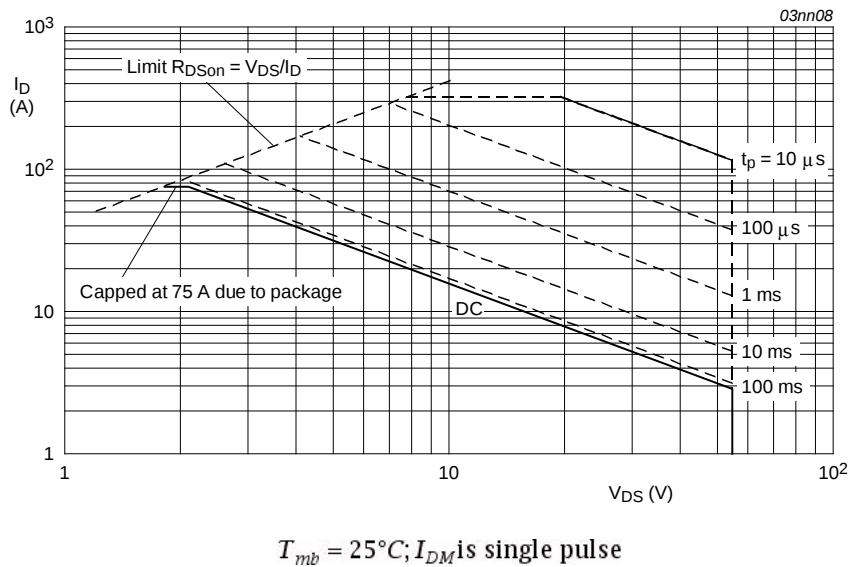


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

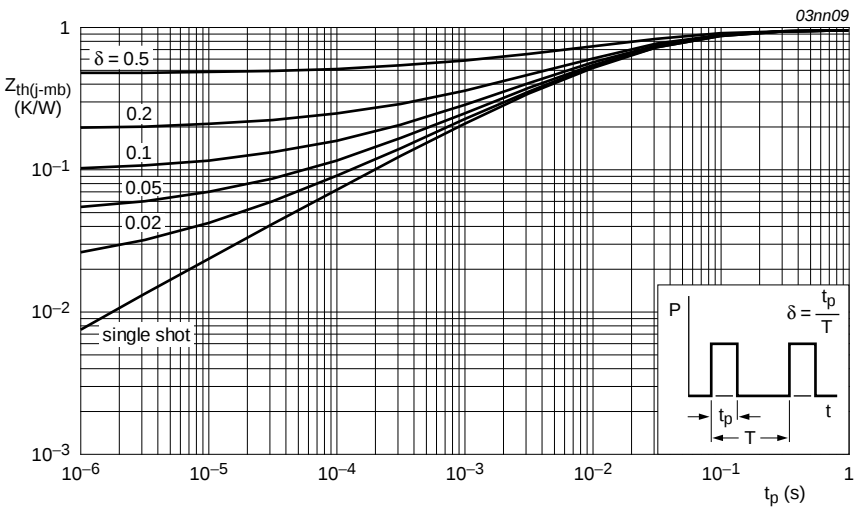


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _J = 25 °C	55	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _J = -55 °C	50	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; see Figure 10	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; see Figure 10	-	-	2.3	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; see Figure 10	1.1	1.5	2	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _J = 175 °C	-	-	500	µA
		V _{DS} = 55 V; V _{GS} = 0 V; T _J = 25 °C	-	0.02	1	µA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = 15 V; T _J = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -15 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _J = 175 °C; see Figure 11 ; see Figure 12	-	-	24	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _J = 25 °C	-	-	13.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C	-	9	10	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _J = 25 °C; see Figure 11 ; see Figure 12	-	10.2	12	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 44 V; V _{GS} = 5 V; T _J = 25 °C; see Figure 13	-	31	-	nC
Q _{GS}	gate-source charge		-	6	-	nC
Q _{GD}	gate-drain charge		-	12	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _J = 25 °C; see Figure 14	-	2770	3693	pF
C _{oss}	output capacitance		-	360	431	pF
C _{rss}	reverse transfer capacitance		-	160	220	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _J = 25 °C	-	19	-	ns
t _r	rise time		-	101	-	ns
t _{d(off)}	turn-off delay time		-	96	-	ns
t _f	fall time		-	75	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to centre of die ; T _J = 25 °C	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die ; T _J = 25 °C	-	4.5	-	nH
L _S	internal source inductance	from source lead 6 mm from package to source bond pad ; T _J = 25 °C	-	7.5	-	nH

Source-drain diode

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$;	-	55	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	53	-	nC

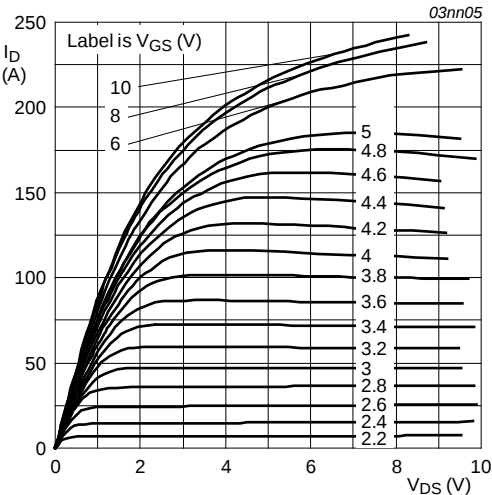


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

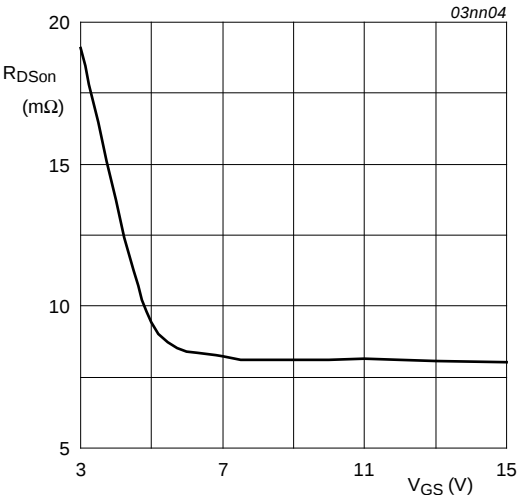


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

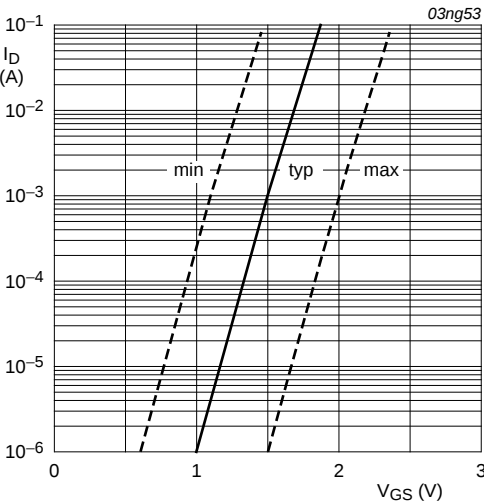


Fig 7. Sub-threshold drain current as a function of gate-source voltage

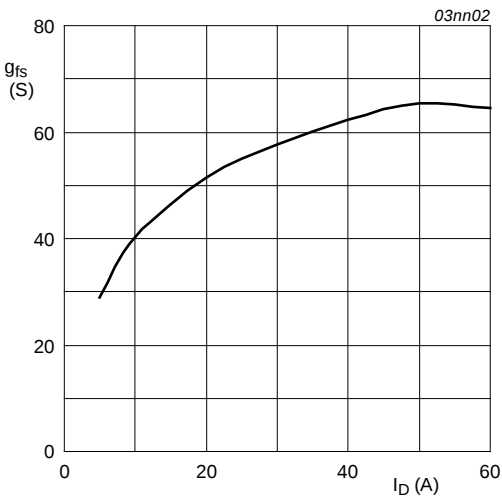


Fig 8. Forward transconductance as a function of drain current; typical values

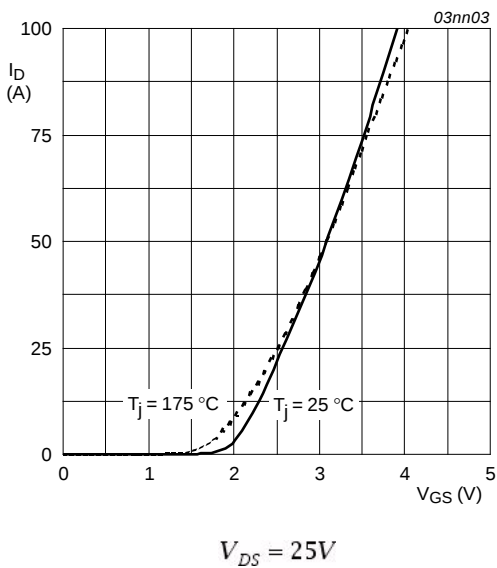


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

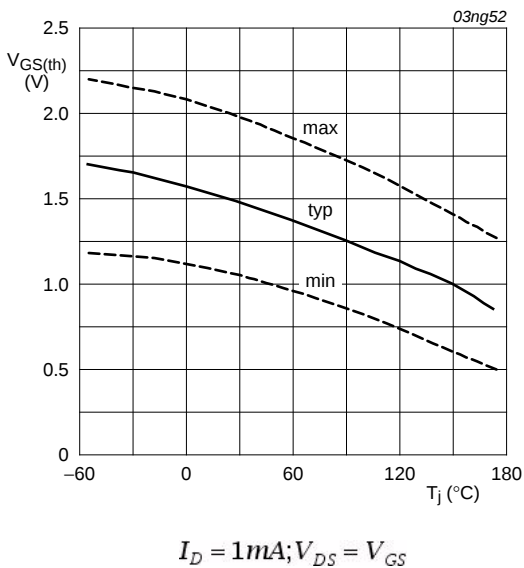


Fig 10. Gate-source threshold voltage as a function of junction temperature

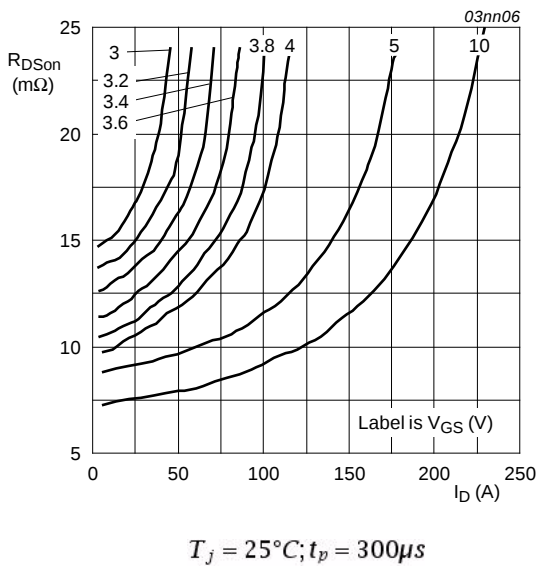


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

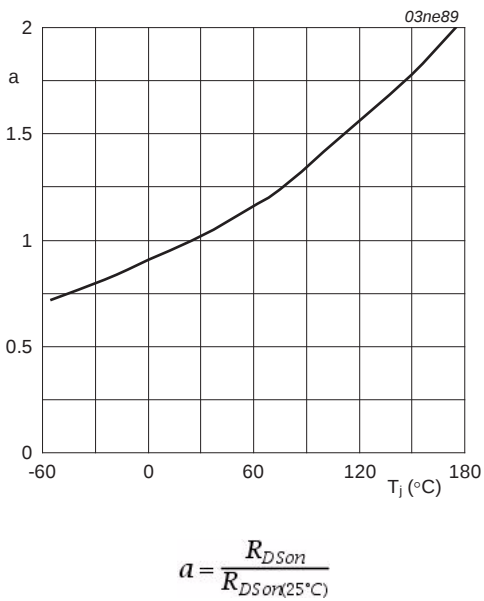


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

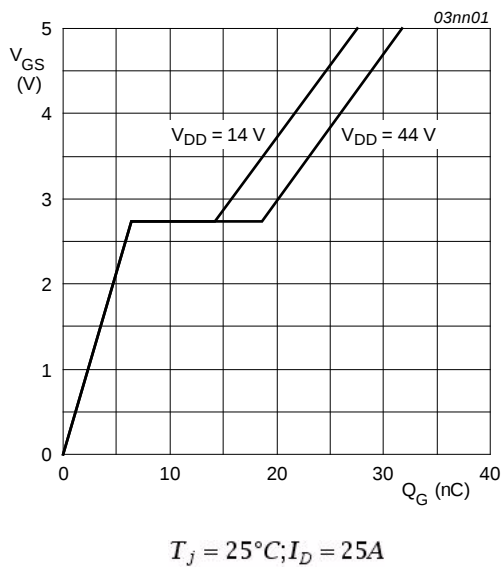


Fig 13. Gate-source voltage as a function of gate charge; typical values

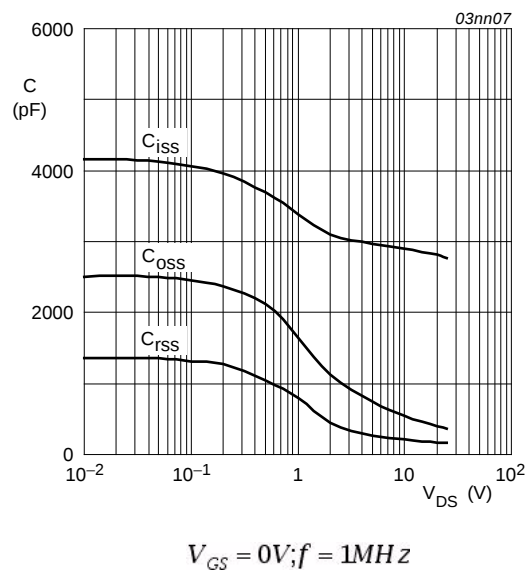


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

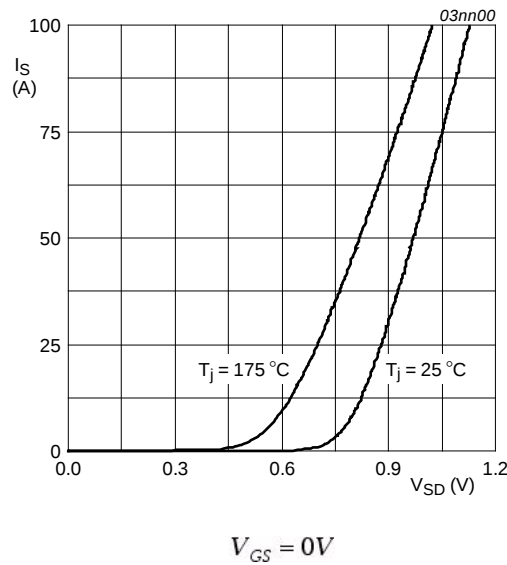
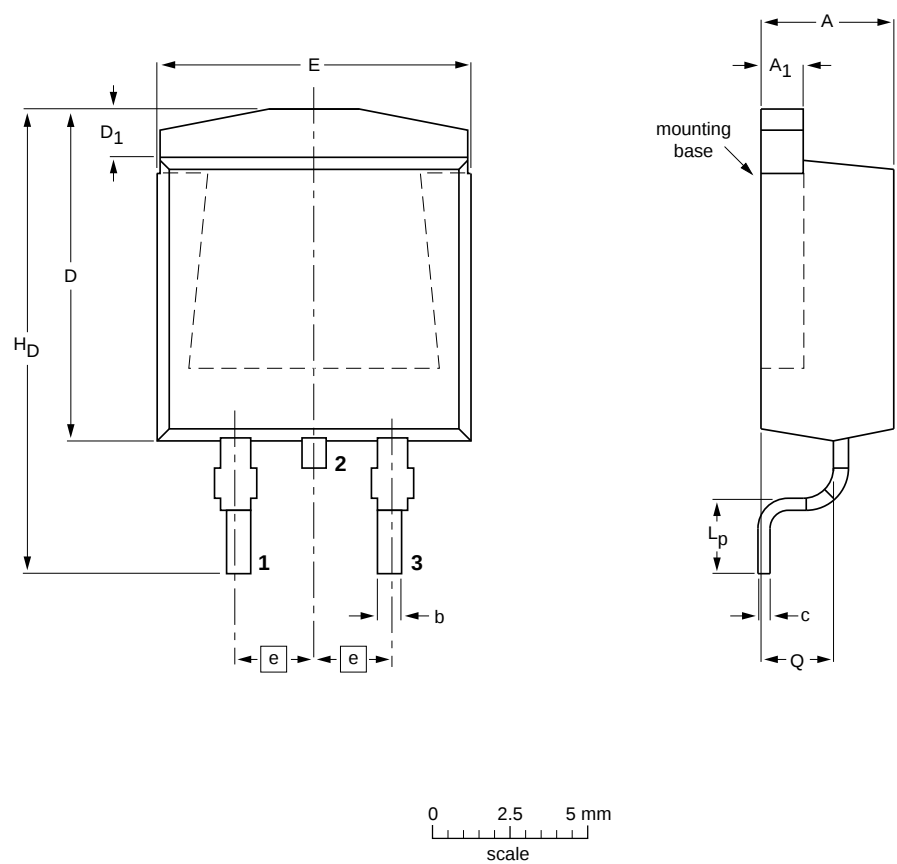


Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

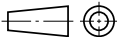
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9612-55B v.2	20100604	Product data sheet	-	BUK95_9612_55B-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number BUK9612-55B separated from data sheet BUK95_9612_55B-01.			
BUK95_9612_55B-01 (9397 750 11247)	20030428	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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