Low Inductance Capacitors

Introduction

The signal integrity characteristics of a Power Delivery Network (PDN) are becoming critical aspects of board level and semiconductor package designs due to higher operating frequencies, larger power demands, and the ever shrinking lower and upper voltage limits around low operating voltages. These power system challenges are coming from mainstream designs with operating frequencies of 300MHz or greater, modest ICs with power demand of 15 watts or more, and operating voltages below 3 volts.

The classic PDN topology is comprised of a series of capacitor stages. Figure 1 is an example of this architecture with multiple capacitor stages.

An ideal capacitor can transfer all its stored energy to a load instantly. A real capacitor has parasitics that prevent instantaneous transfer of a capacitor's stored energy. The true nature of a capacitor can be modeled as an RLC equivalent circuit. For most simulation purposes, it is possible to model the characteristics of a real capacitor with one capacitor, one resistor, and one inductor. The RLC values in this model are commonly referred to as equivalent series capacitance (ESC), equivalent series resistance (ESR), and equivalent series inductance (ESL).

The ESL of a capacitor determines the speed of energy transfer to a load. The lower the ESL of a capacitor, the faster that energy can be transferred to a load. Historically, there has been a tradeoff between energy storage (capacitance) and inductance (speed of energy delivery). Low ESL devices typically have low capacitance. Likewise, higher capacitance devices typically have higher ESLs. This tradeoff between ESL (speed of energy delivery) and capacitance (energy storage) drives the PDN design topology that places the fastest low ESL capacitors as close to the load as possible. Low Inductance MLCCs are found on semiconductor packages and on boards as close as possible to the load.

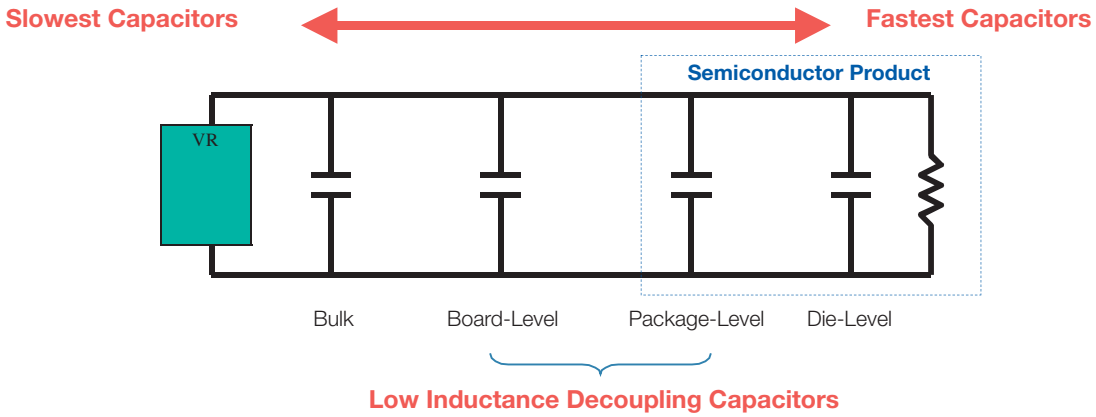


Figure 1 Classic Power Delivery Network (PDN) Architecture

LOW INDUCTANCE CHIP CAPACITORS

The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL. A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer side of its rectangular shape.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL then an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC versus a standard MLCC.

INTERDIGITATED CAPACITORS

The size of a current loop has the greatest impact on the ESL characteristics of a surface mount capacitor. There is a secondary method for decreasing the ESL of a capacitor. This secondary method uses adjacent opposing current loops to reduce ESL. The InterDigitated Capacitor (IDC) utilizes both primary and secondary methods of reducing inductance. The IDC architecture shrinks the distance between terminations to minimize the current loop size, then further reduces inductance by creating adjacent opposing current loops.

An IDC is one single capacitor with an internal structure that has been optimized for low ESL. Similar to standard MLCC versus LICCs, the reduction in ESL varies by EIA case size. Typically, for the same EIA size, an IDC delivers an ESL that is at least 80% lower than an MLCC.

LAND GRID ARRAY (LGA) CAPACITORS

Land Grid Array (LGA) capacitors are based on the first Low ESL MLCC technology created to specifically address the design needs of current day Power Delivery Networks (PDNs). This is the 3rd low inductance capacitor technology developed by AVX. LGA technology provides engineers with new options. The LGA internal structure and manufacturing technology eliminates the historic need for a device to be physically small to create small current loops to minimize inductance.

The first family of LGA products are 2 terminal devices. A 2 terminal 0306 LGA delivers ESL performance that is equal to or better than an 0306 8 terminal IDC. The 2 terminal 0805 LGA delivers ESL performance that approaches the 0508 8 terminal IDC. New designs that would have used 8 terminal IDCs are moving to 2 terminal LGAs because the layout is easier for a 2 terminal device and manufacturing yield is better for a 2 terminal LGA versus an 8 terminal IDC.

LGA technology is also used in a 4 terminal family of products that AVX is sampling and will formerly introduce in 2008. Beyond 2008, there are new multi-terminal LGA product families that will provide even more attractive options for PDN designers.

LOW INDUCTANCE CHIP ARRAYS (LICA®)

The LICA® product family is the result of a joint development effort between AVX and IBM to develop a high performance MLCC family of decoupling capacitors. LICA was introduced in the 1980s and remains the leading choice of designers in high performance semiconductor packages and high reliability board level decoupling applications.

LICA® products are used in 99.999% uptime semiconductor package applications on both ceramic and organic substrates. The C4 solder ball termination option is the perfect compliment to flip-chip packaging technology. Mainframe class CPUs, ultimate performance multi-chip modules, and communications systems that must have the reliability of 5 9's use LICA®.

LICA® products with either Sn/Pb or Pb-free solder balls are used for decoupling in high reliability military and aerospace applications. These LICA® devices are used for decoupling of large pin count FPGAs, ASICs, CPUs, and other high power ICs with low operating voltages.

When high reliability decoupling applications require the very lowest ESL capacitors, LICA® products are the best option.

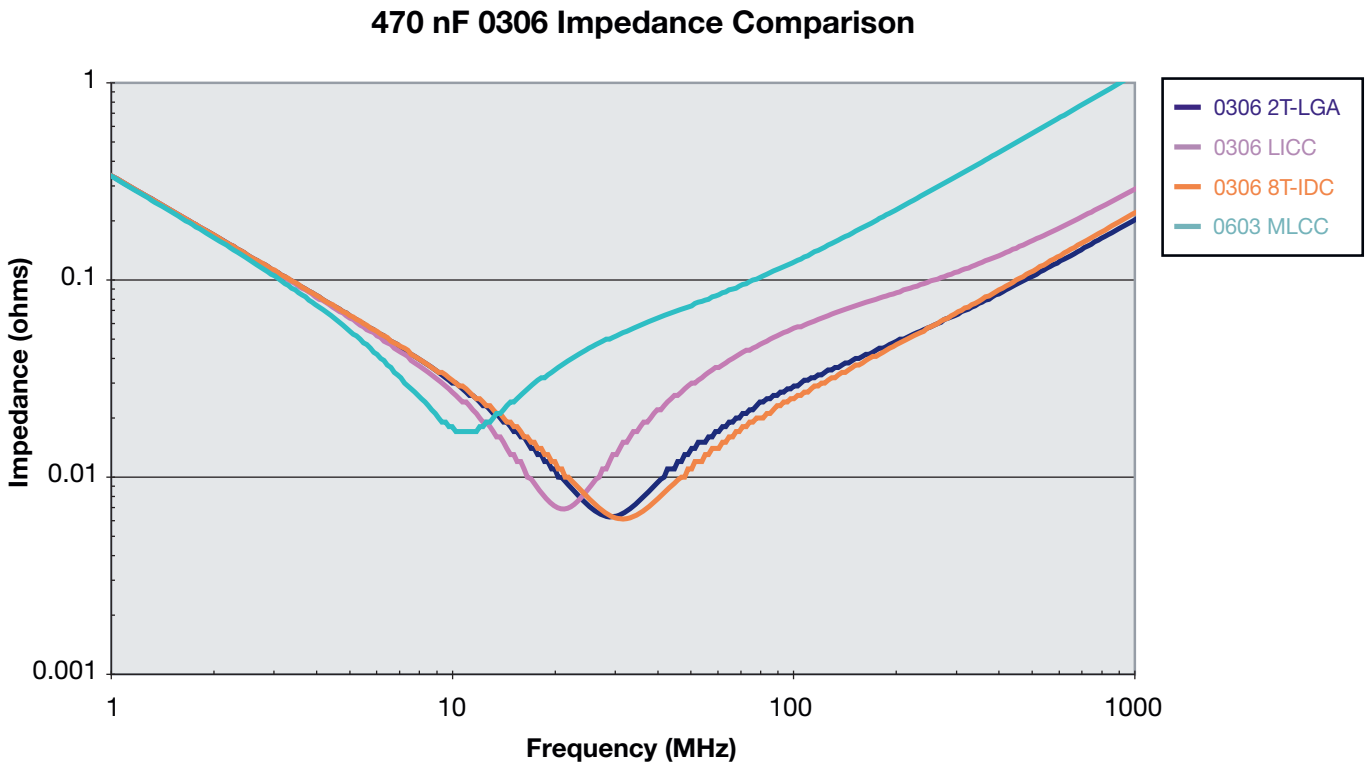
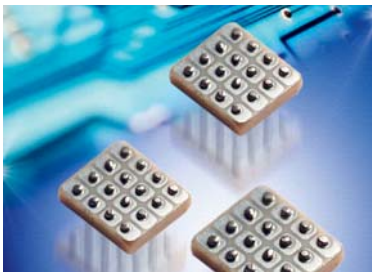


Figure 2 MLCC, LICC, IDC, and LGA technologies deliver different levels of equivalent series inductance (ESL).

Low Inductance Capacitors

LICA® (Low Inductance Decoupling Capacitor Arrays)



LICA® arrays utilize up to four separate capacitor sections in one ceramic body (see Configurations and Capacitance Options). These designs exhibit a number of technical advancements:

Low Inductance features–

- Low resistance platinum electrodes in a low aspect ratio pattern
- Double electrode pickup and perpendicular current paths
- C4 "flip-chip" technology for minimal interconnect inductance

HOW TO ORDER

LICA	3	T	102	M	3	F	C	4	A	A
Style & Size	**Voltage**	**Dielectric**	**Cap/Section (EIA Code)**	**Capacitance Tolerance**	**Height Code**	**Termination**	**Reel Packaging**	**# of Caps/Part**	**Inspection Code**	**Code Face**
	5V = 9 10V = Z 25V = 3	D = X5R T = T55T S = High K T55T	102 = 1000 pF 103 = 10 nF 104 = 100 nF	M = ±20% P = GMV	6 = 0.500mm 3 = 0.650mm 1 = 0.875mm 5 = 1.100mm 7 = 1.600mm	F = C4 Solder Balls- 97Pb/3Sn H = C4 Solder Balls Low ESR G = Lead Free SAC R = Cr-Cu-Au N = Cr-Ni-Au V = Eutectic Lead-Tin Bump-37%Pb/63%Sn X = None	M = 7" Reel R = 13" Reel 6 = 2"x2" Waffle Pack 8 = 2"x2" Black Waffle Pack 7 = 2"x2" Waffle Pack w/ termination facing up A = 2"x2" Black Waffle Pack w/ termination facing up C = 4"x4" Waffle Pack w/ clear lid	1 = one 2 = two 4 = four	A = Standard B = COTS+ X = MIL-PRF-123	A = Bar B = No Bar C = Dot, S55S Dielectrics D = Triangle

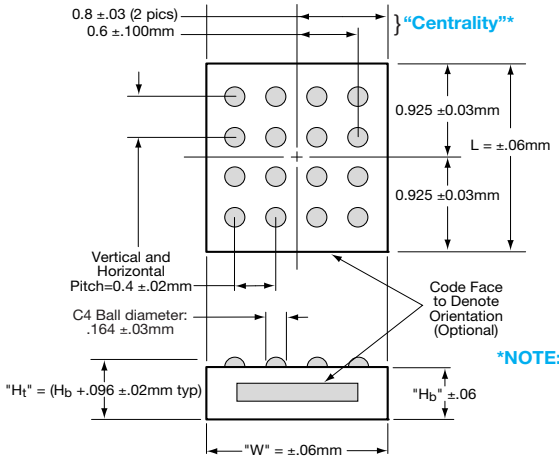
NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

RoHS COMPLIANT

TABLE 1

Typical Parameters	T55T/S55S	Units
Capacitance, 25°C	Co	Nanofarads
Capacitance, 55°C	1.45 x Co	Nanofarads
Capacitance, 85°C	0.7 x Co	Nanofarads
Dissipation Factor 25°	15	Percent
ESR (Nominal)	20	Milliohms
DC Resistance	0.2	Ohms
IR (Minimum @25°) (Design Dependent)	300	Megaohms
Dielectric Breakdown, Min	500	Volts
Thermal Coefficient of Expansion	8.5	ppm/°C 25-100°
Inductance: (Design Dependent) (Nominal)	30	Pico-Henries
Frequency of Operation	DC to 5 Gigahertz	
Ambient Temp Range	-55° to 125°C	

SOLDER BALL AND PAD DIMENSIONS



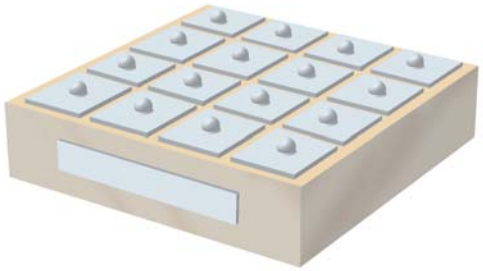
*NOTE: The C4 pattern will be within 0.1mm of the center of the LICA body, in both axes.

Pin A1 is the lower left hand ball.

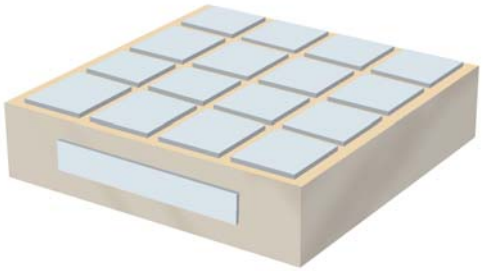
Code (Body Height)	Width (W)	Length (L)	Height Body (H_b)
1	1.600mm	1.850mm	0.875mm
3	1.600mm	1.850mm	0.650mm
5	1.600mm	1.850mm	1.100mm
6	1.600mm	1.850mm	0.500mm
7	1.600mm	1.850mm	1.600mm

TERMINATION OPTIONS

SOLDER BALLS
TERMINATION OPTION F, H, G OR V



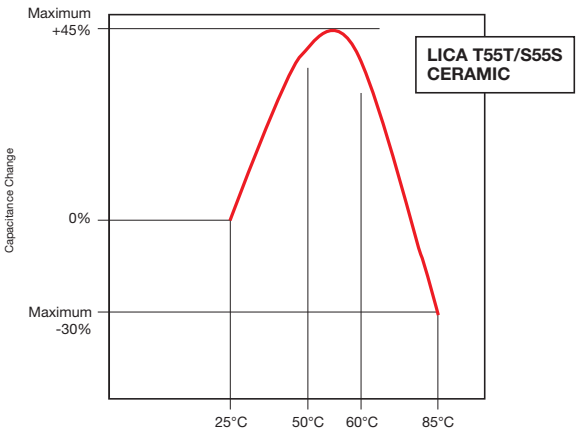
TERMINATION OPTION R OR N



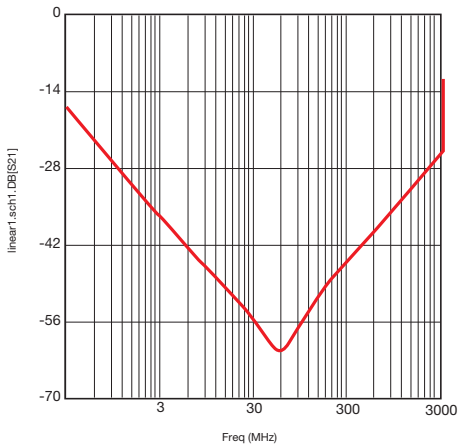
Low Inductance Capacitors

LICA® (Low Inductance Decoupling Capacitor Arrays)

TEMPERATURE VS CAPACITANCE CHANGE



TYPICAL S21 FOR LICA AT SINGLE VIA

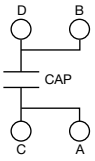


LICA COMMON PART NUMBER LIST

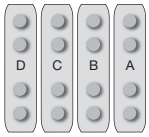
Part Number	Voltage	Thickness (mm)	Capacitors per Package
LICA3T193M3FC4AA	25	0.650	4
LICA3T153P3FC4AA	25	0.650	4
LICA3T134M1FC1AA	25	0.875	1
LICA3T104P1FC1AA	25	0.875	1
LICA3T333M1FC4AA	25	0.875	4
LICA3T263P3FC4AA	25	0.650	4
LICA3T244M5FC1AA	25	1.100	1
LICA3T194P5FC1AA	25	1.100	1
LICA3T394M7FC1AB	25	1.600	1
LICA3T314P7FC1AB	25	1.600	1
Extended Range			
LICAZT623M3FC4AB	10	0.650	4
LICA3T104M3FC1A	25	0.650	1
LICA3T803P3FC1A	25	0.650	1
LICA3T423M3FC2A	25	0.650	2
LICA3T333P3FC2A	25	0.650	2
LICA3S253M3FC4A	25	0.650	4
LICAZD753M3FC4AD	10	0.650	4
LICAZD504M3FC1AB	10	0.650	1
LICAZD604M7FC1AB	10	1.600	1
LICA3D193M3FC4AB	25	0.650	4

CONFIGURATION

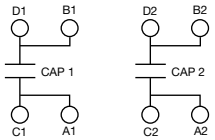
Schematic



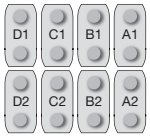
Code Face



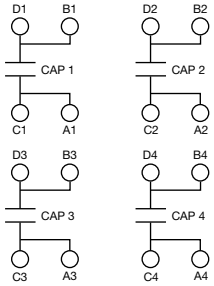
Schematic



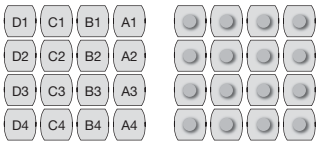
Code Face



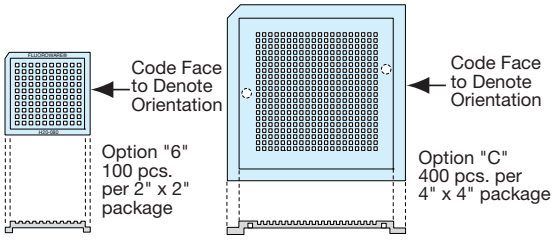
Schematic



Code Face



WAFFLE PACK OPTIONS FOR LICA®



Note: Standard configuration is Termination side down

LICA® PACKAGING SCHEME "M" AND "R"

8mm conductive plastic tape on reel:
"M"=7" reel max. qty. 3,000, "R"=13" reel max. qty. 8,000