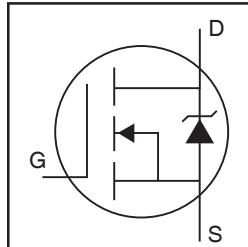


Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

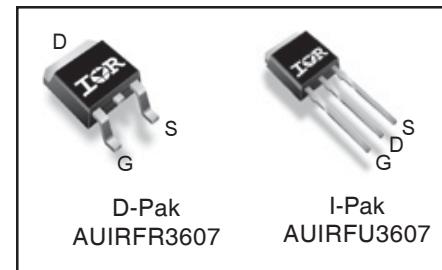


HEXFET® Power MOSFET

V_{DSS}	75V
R_{DS(on)} typ.	7.34mΩ
	9.0mΩ
I_D (Silicon Limited)	80A①
I_D (Package Limited)	56A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	80①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	56①	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	56	
I _{DM}	Pulsed Drain Current ②	310	
P _D @ T _C = 25°C	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.96	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	120	mJ
I _{AR}	Avalanche Current ②	46	A
E _{AR}	Repetitive Avalanche Energy ③	14	mJ
dv/dt	Peak Diode Recovery ④	27	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑤	—	1.045	°C/W
R _{θJA}	Junction-to-Ambient ⑤	—	50	
R _{θJA}	Junction-to-Ambient (PCB Mount) ⑤	—	110	

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.096	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5\text{mA}$ ②
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	7.34	9.0	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$, $I_D = 46\text{A}$ ⑤
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 100\mu\text{A}$
g_{fs}	Forward Transconductance	115	—	—	S	$V_{\text{DS}} = 50\text{V}$, $I_D = 46\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 75\text{V}$, $V_{\text{GS}} = 0\text{V}$
				250		$V_{\text{DS}} = 60\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -20\text{V}$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	56	84	nC	$I_D = 46\text{A}$
Q_{gs}	Gate-to-Source Charge	—	13	—		$V_{\text{DS}} = 38\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	16	—		$V_{\text{GS}} = 10\text{V}$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{\text{gd}}$)	—	40	—		$I_D = 46\text{A}$, $V_{\text{DS}} = 0\text{V}$, $V_{\text{GS}} = 10\text{V}$
$R_{\text{G}(\text{int})}$	Internal Gate Resistance	—	0.55	—	Ω	
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	16	—	ns	$V_{\text{DD}} = 49\text{V}$
t_r	Rise Time	—	110	—		$I_D = 46\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	43	—		$R_{\text{G}} = 6.8\Omega$
t_f	Fall Time	—	96	—		$V_{\text{GS}} = 10\text{V}$ ⑤
C_{iss}	Input Capacitance	—	3070	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	280	—		$V_{\text{DS}} = 50\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	130	—		$f = 1.0\text{MHz}$
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	380	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 60V ⑧
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	610	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 60V ⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	80①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	310		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 46\text{A}$, $V_{\text{GS}} = 0\text{V}$ ⑤
t_{rr}	Reverse Recovery Time	—	33	50		
Q_{rr}	Reverse Recovery Charge	—	39	59	ns	$T_J = 25^\circ\text{C}$ $V_R = 64\text{V}$, $T_J = 125^\circ\text{C}$ $I_F = 46\text{A}$
		—	32	48		
I_{RRM}	Reverse Recovery Current	—	47	71	nC	$T_J = 25^\circ\text{C}$ $\text{di}/\text{dt} = 100\text{A}/\mu\text{s}$ ⑤ $T_J = 125^\circ\text{C}$
		—	1.9	—		
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.12\text{mH}$
 $R_G = 25\Omega$, $I_{\text{AS}} = 46\text{A}$, $V_{\text{GS}} = 10\text{V}$. Part not recommended for use above this value.

④ $I_{\text{SD}} \leq 46\text{A}$, $\text{di}/\text{dt} \leq 1920\text{A}/\mu\text{s}$, $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑨ R_{θ} is measured at T_J approximately 90°C .

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101) ^{††}	
Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.			
Moisture Sensitivity Level		3L-D PAK	MSL1
		3L-I-PAK	N/A
ESD	Machine Model	Class M4(+/- 600V) ^{†††} (per AEC-Q101-002)	
	Human Body Model	Class H1C(+/- 2000V) ^{†††} (per AEC-Q101-001)	
	Charged Device Model	Class C4(+/- 1000V) ^{†††} (per AEC-Q101-005)	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Exceptions to AEC-Q101 requirements are noted in the qualification report.

^{†††} Highest passing voltage

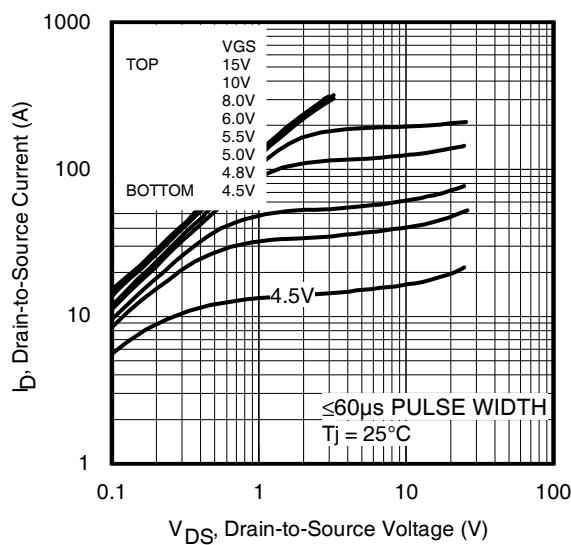


Fig 1. Typical Output Characteristics

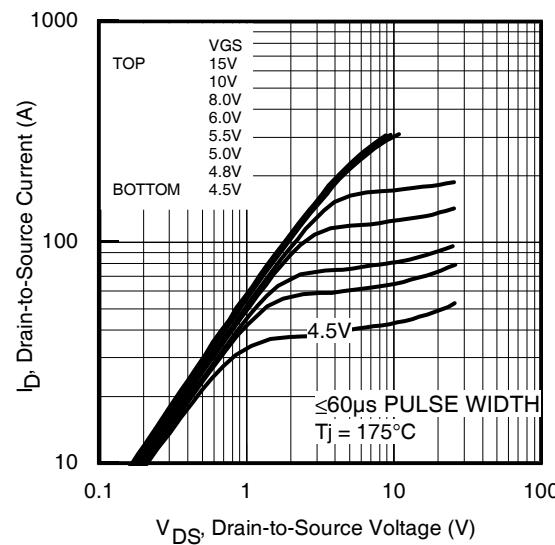


Fig 2. Typical Output Characteristics

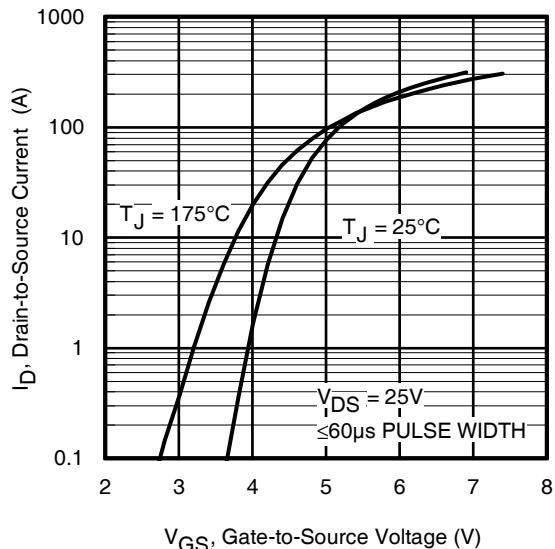


Fig 3. Typical Transfer Characteristics

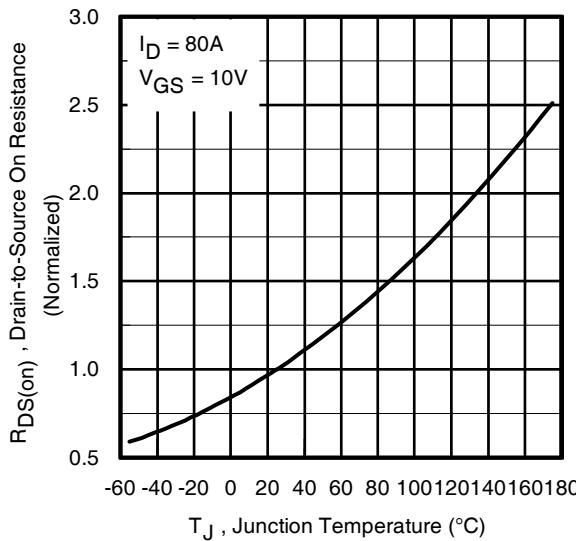


Fig 4. Normalized On-Resistance vs. Temperature

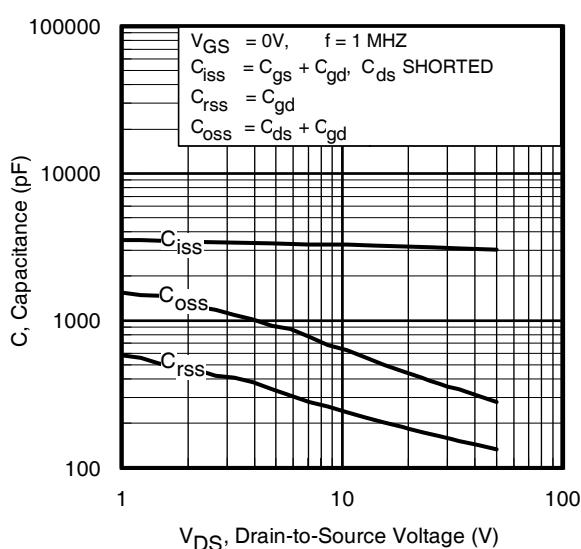


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

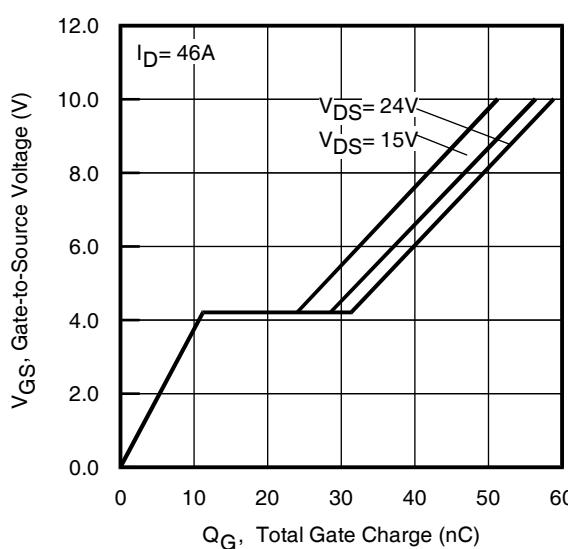


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

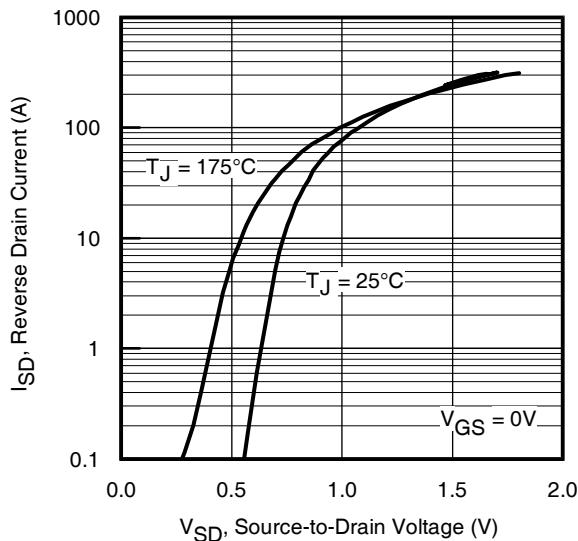


Fig 7. Typical Source-Drain Diode Forward Voltage

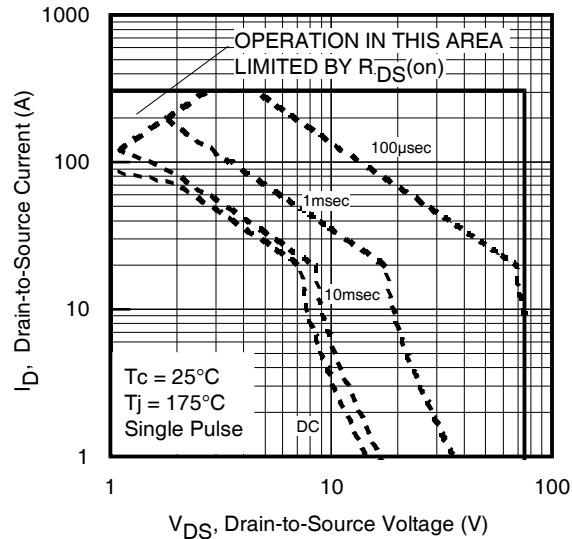


Fig 8. Maximum Safe Operating Area

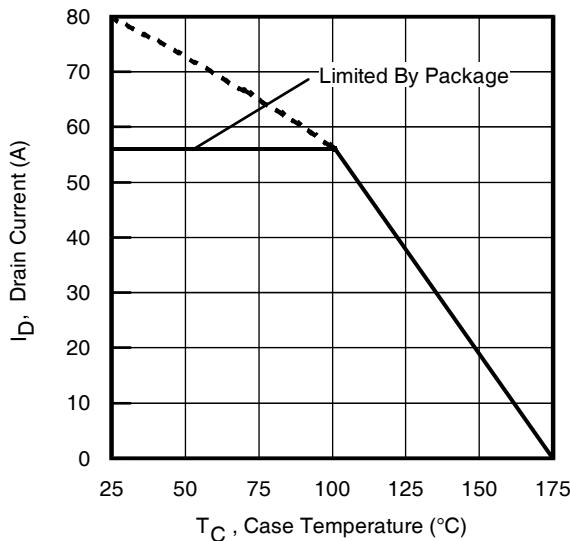


Fig 9. Maximum Drain Current vs. Case Temperature

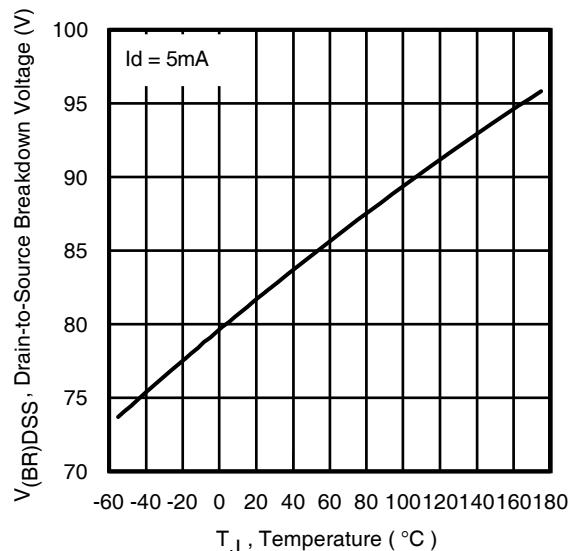


Fig 10. Drain-to-Source Breakdown Voltage

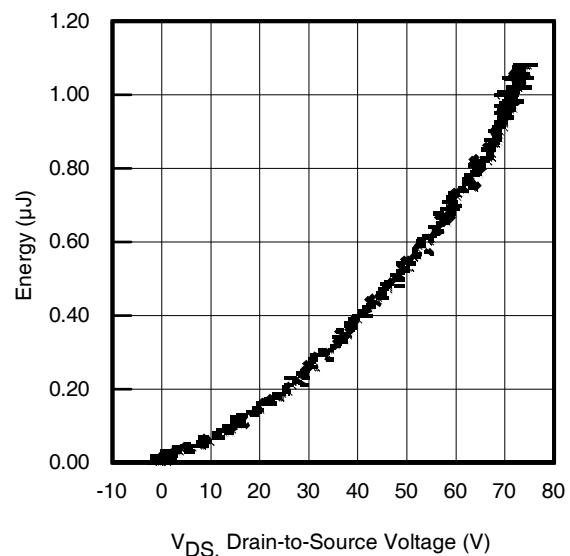


Fig 11. Typical C_{oss} Stored Energy

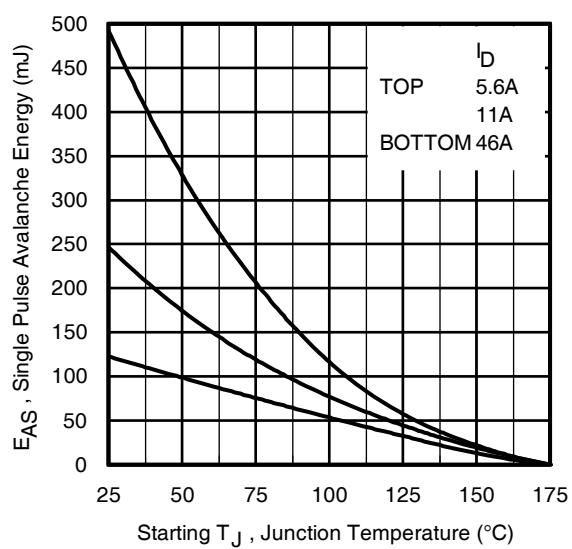


Fig 12. Maximum Avalanche Energy vs. Drain Current

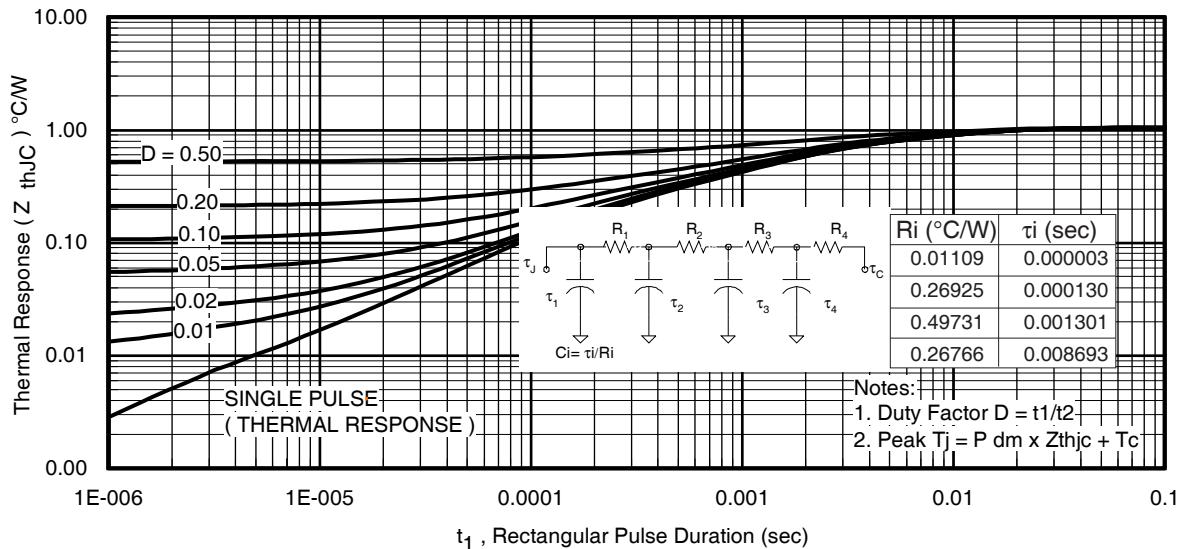


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

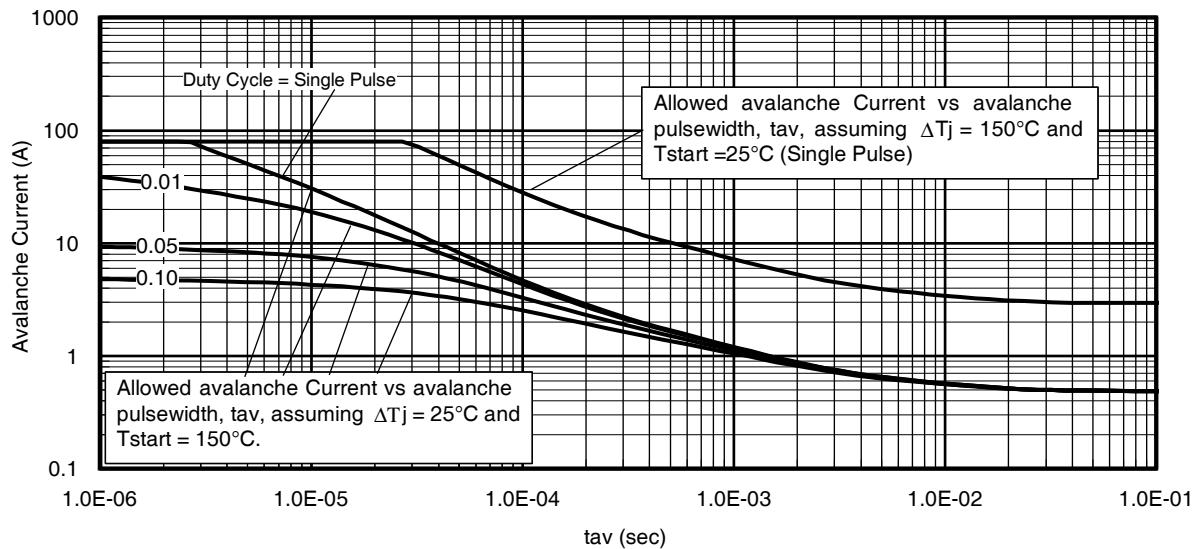


Fig 14. Typical Avalanche Current vs. Pulsewidth

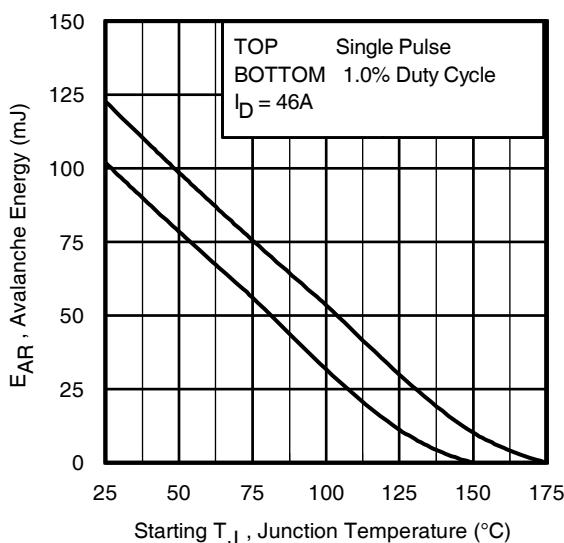


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

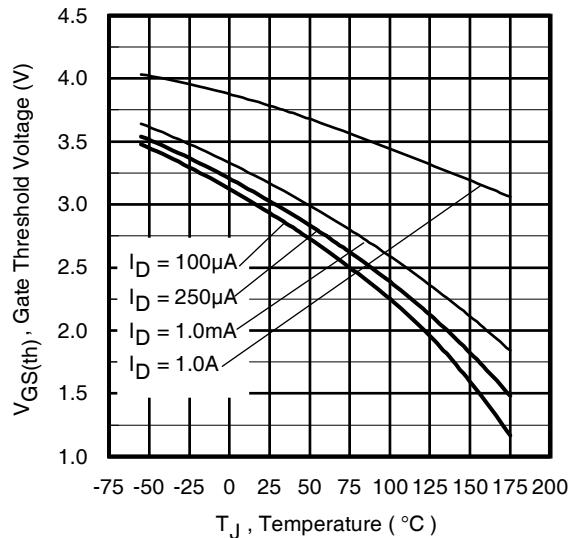


Fig. 16. Threshold Voltage vs. Temperature

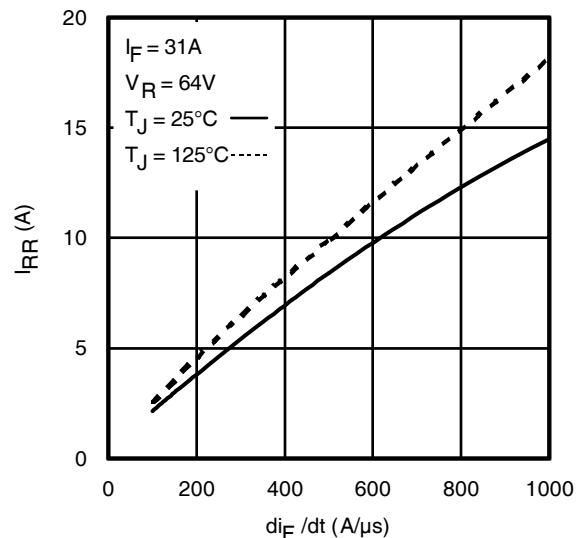


Fig. 17 - Typical Recovery Current vs. di_f/dt

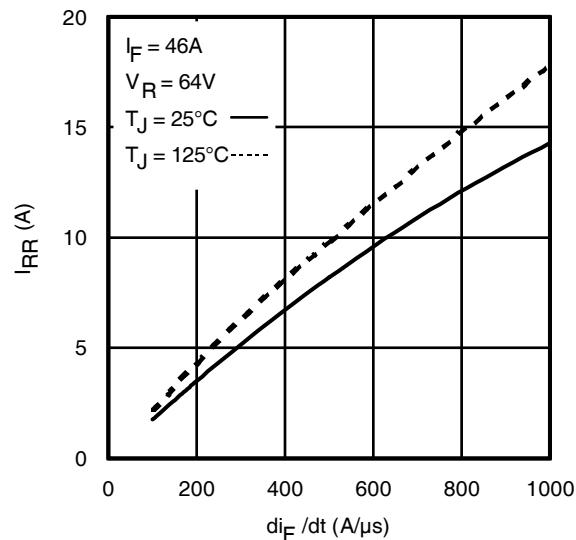


Fig. 18 - Typical Recovery Current vs. di_f/dt

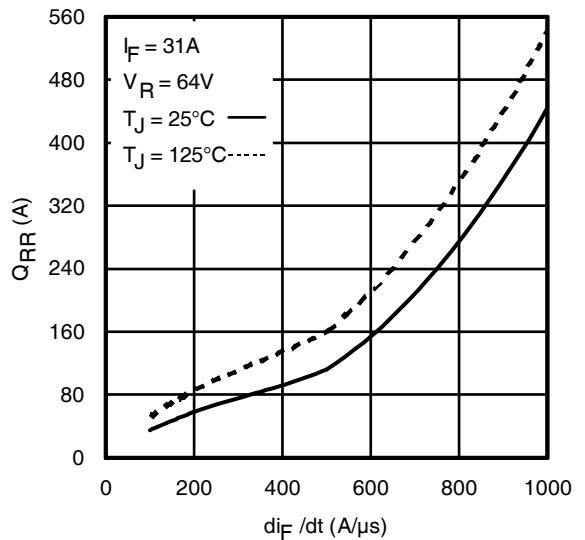


Fig. 19 - Typical Stored Charge vs. di_f/dt

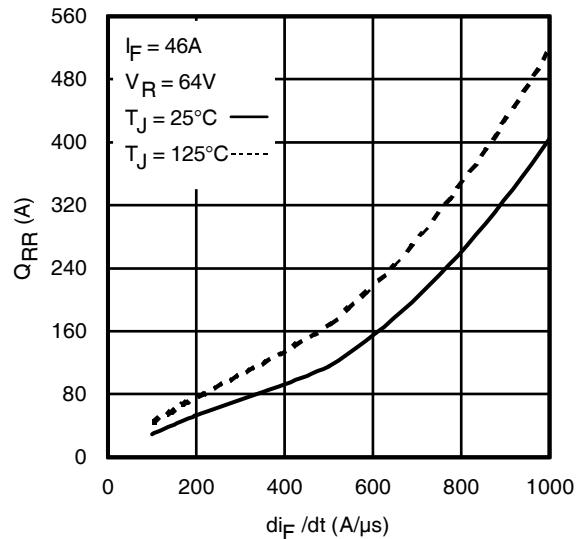


Fig. 20 - Typical Stored Charge vs. di_f/dt

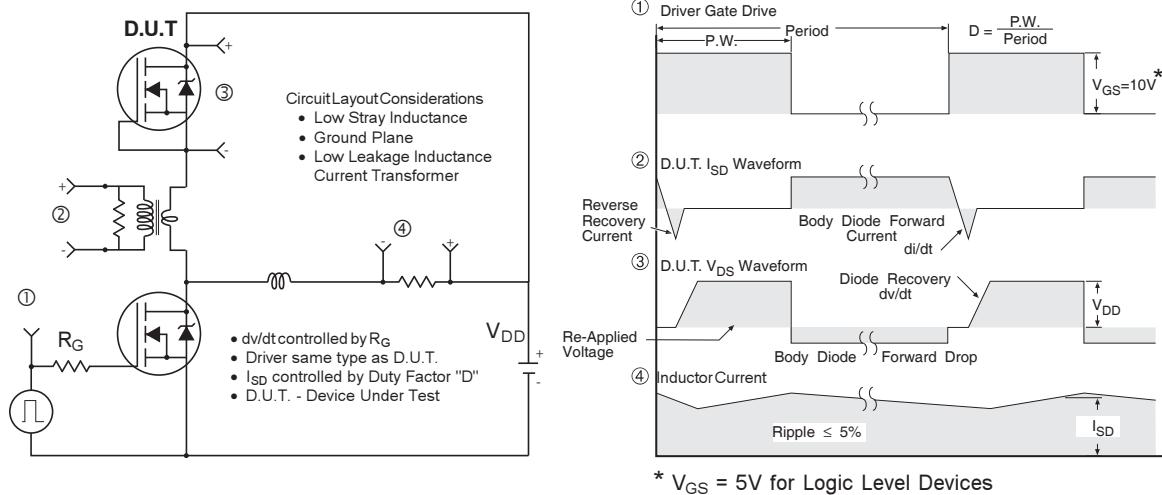


Fig 20. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

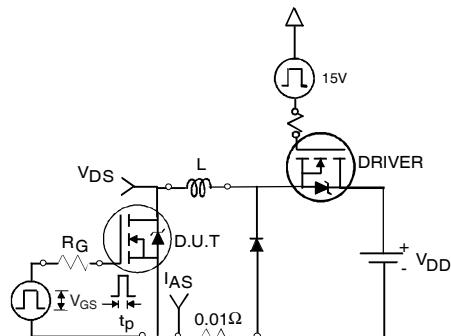


Fig 21a. Unclamped Inductive Test Circuit

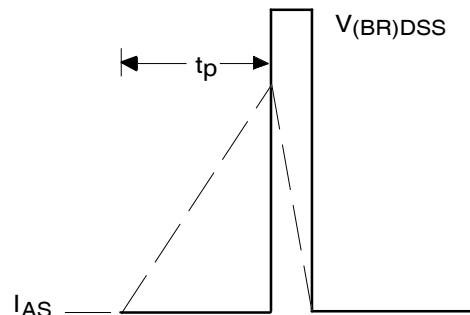


Fig 21b. Unclamped Inductive Waveforms

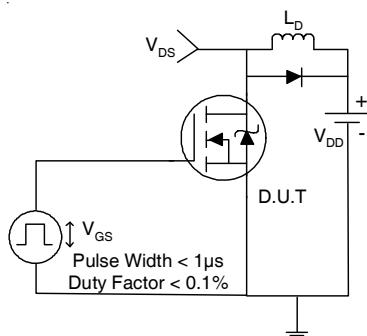


Fig 22a. Switching Time Test Circuit

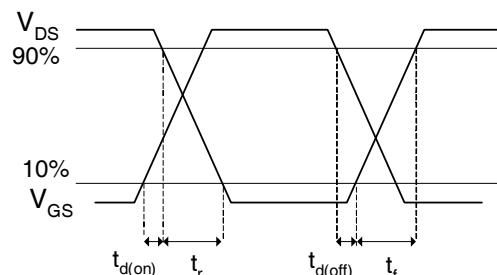


Fig 22b. Switching Time Waveforms

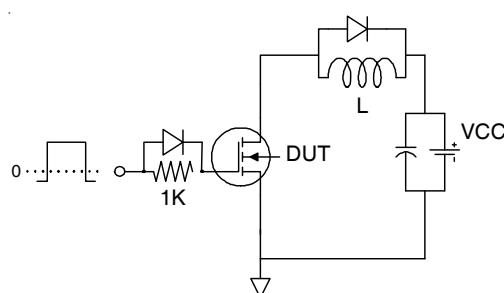


Fig 23a. Gate Charge Test Circuit

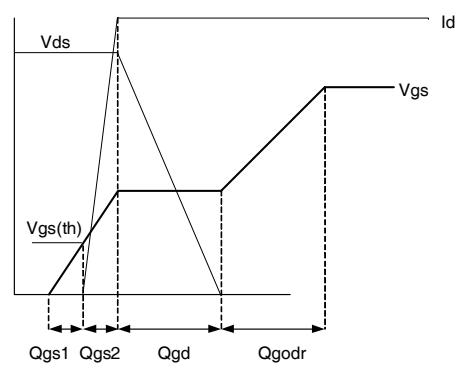
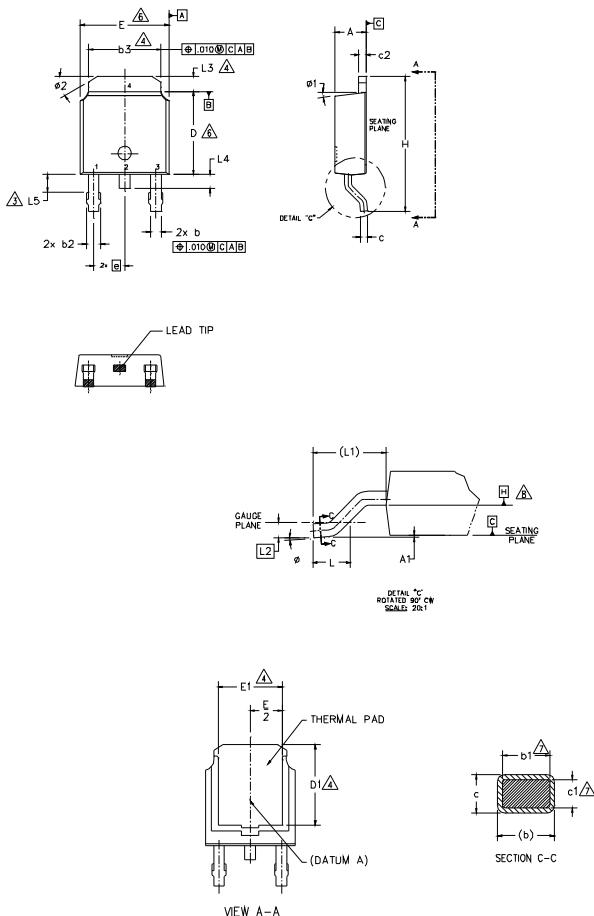


Fig 23b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
3. LEAD DIMENSION UNCONTROLLED IN L5.
4. DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5. SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7. DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9. OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	.086	.094	7	
A1	—	0.13	—	.005		
b	0.64	0.89	.025	.035		
b1	0.65	0.79	.025	.031		
b2	0.76	1.14	.030	.045		
b3	4.95	5.46	.195	.215		
c	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022	7	
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245		
D1	5.21	—	.205	—		
E	6.35	6.73	.250	.265		
E1	4.32	—	.170	—		
e	2.29	BSC	.090	BSC		
H	9.40	10.41	.370	.410	4	
L	1.40	1.78	.055	.070		
L1	2.74	BSC	.108	REF.		
L2	0.51	BSC	.020	BSC		
L3	0.89	1.27	.035	.050		
L4	—	1.02	—	.040		
L5	1.14	1.52	.045	.060		
Ø	0°	10°	0°	10°	3	
Ø1	0°	15°	0°	15°		
Ø2	25°	35°	25°	35°		

LEAD ASSIGNMENTS

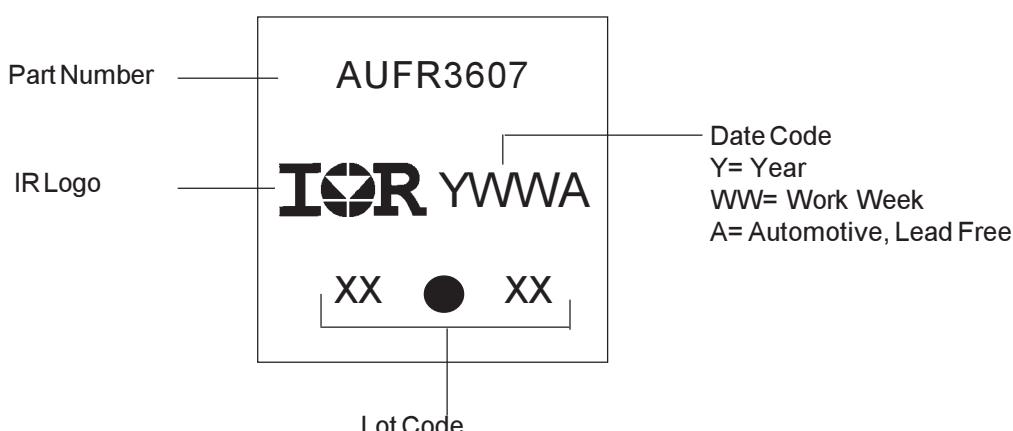
HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

IGBT & CoPAK

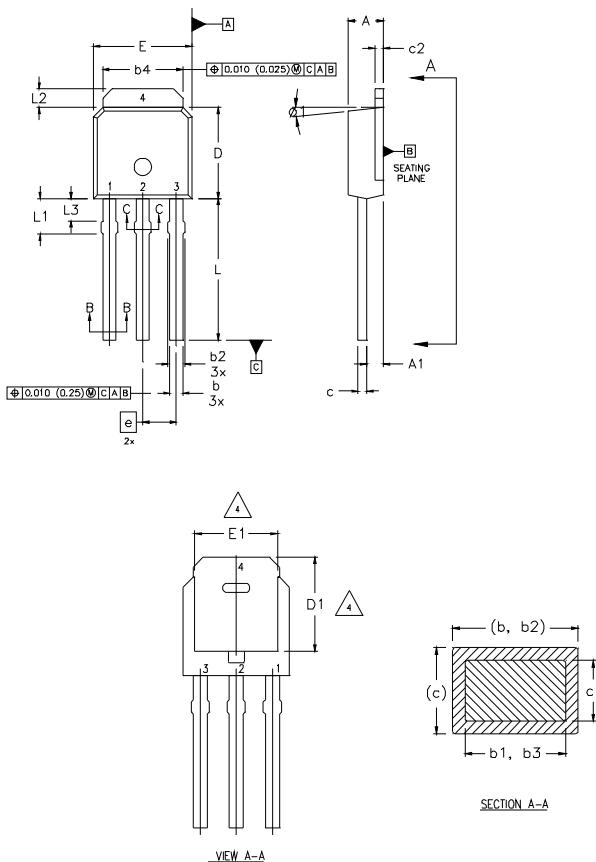
1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>
www.irf.com

I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

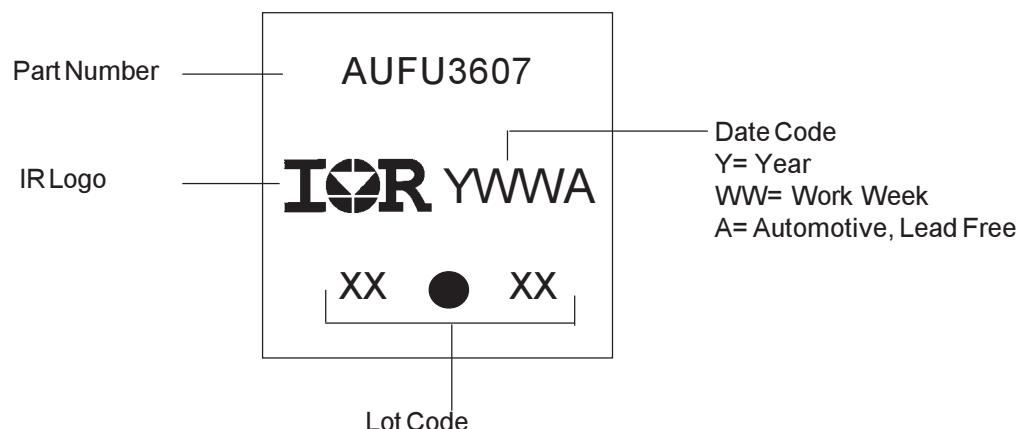
LEAD ASSIGNMENTS

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	—	0.205	—	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	—	0.170	—	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	
L3	1.14	1.52	0.045	0.060	5
Ø1	0'	15'	0'	15'	

HEXFET

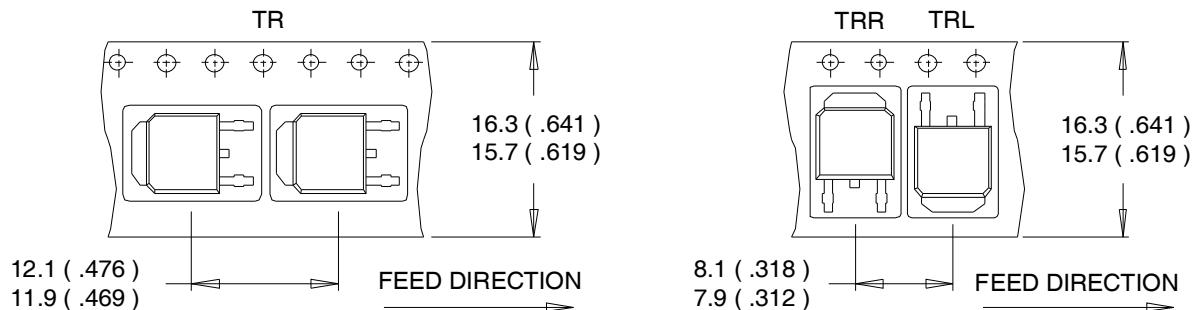
1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

I-Pak (TO-251AA) Part Marking Information



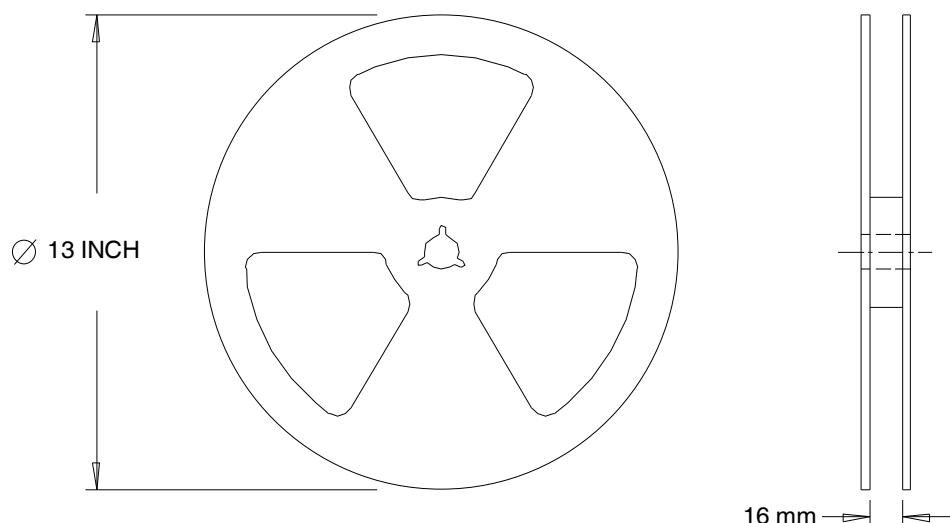
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Ordering Information

Base part	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFR3607	DPak	Tube	75	AUIRFR3607
		Tape and Reel	2000	AUIRFR3607TR
		Tape and Reel Left	3000	AUIRFR3607TRL
		Tape and Reel Right	3000	AUIRFR3607TRR
AUIRFU3607	IPak	Tube	75	AUIRFU3607

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<http://www.irf.com/technical-info/>

WORLD HEADQUARTERS:

101 N. Sepulveda Blvd., El Segundo, California 90245

Tel: (310) 252-7105