APPLICATION NOTE
FOLLOWS DATA SHEETS

MAXIM

Dual Over/Under Voltage Detector

ICL7665

General Description

The ICL7665 is a low power dual over/under voltage detector drawing a typical operating current of only 3μA. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors to any voltage greater than 1.3V. The ICL7665 will operate from any supply voltage in the 1.6V to 16V range, while monitoring voltages from 1.3V to several hundred volts.

The Maxim ICL7665 and ICL7665B are equivalent to the original manufacturer's parts in both pinout and specification. The Maxim ICL7665A is an improved version with a 2% accurate V_{SET1} threshold and guaranteed performance over temperature. All three versions of the Maxim ICL7665 undergo 100% burn-in and are rigorously tested at temperature extremes to enhance their quality and reliability.

Applications

The 3μA quiescent current of the ICL7665 makes it ideal for voltage monitoring in battery powered systems. In both battery and line-powered systems, the unique combination of a reference, two comparators and hysteresis outputs reduces size and component count of many circuits.

- Low Battery Detection
- Power Fail and Brownout Detector
- Battery Backup Switching
- Power Supply Fault Monitoring
- Over/Under-Voltage Protection
- Hi/Low Temperature, Pressure and Voltage Alarms

Features

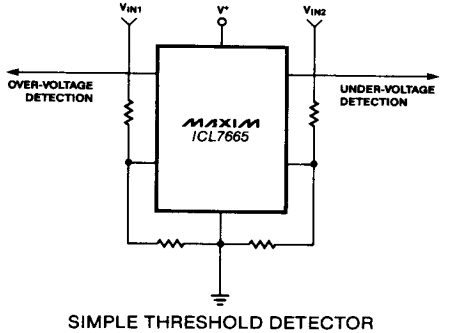
- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Dual Comparator with Precision Internal Reference**
- **3μA Operating Current**
- **2% Threshold Accuracy (ICL7665A)**
- **1.6V to 16V Supply Voltage Range**
- **Onboard Hysteresis Outputs**
- **Trip Points Externally Programmable**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7665C/D*	0°C to +70°C	Dice
ICL7665CJA*	0°C to +70°C	8 Lead Cerdip
ICL7665CPA*	0°C to +70°C	8 Lead Plastic Dip
ICL7665CSA*	0°C to +70°C	8 Lead Small Outline
ICL7665CTV*	0°C to +70°C	8 Lead TO-99
ICL7665AC/D	0°C to +70°C	Dice
ICL7665ACJA	0°C to +70°C	8 Lead Cerdip
ICL7665ACPA	0°C to +70°C	8 Lead Plastic Dip
ICL7665ACSA	0°C to +70°C	8 Lead Small Outline
ICL7665ACTV	0°C to +70°C	8 Lead TO-99

"B" version also available. Order part number ICL7665BXXX

Typical Operating Circuit

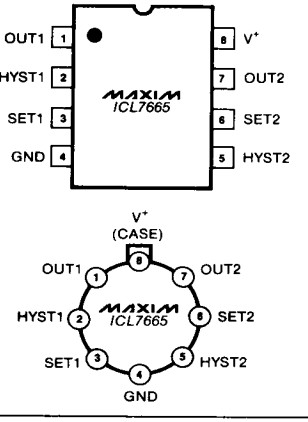


SIMPLE THRESHOLD DETECTOR

(Detailed Circuit Diagram — Figure 3)

Pin Configuration

Top View



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Dual Over/Under Voltage Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ..... −0.3V to +18V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) ..... −0.3V to +18V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) ..... +0.3V to −18V
Input Voltages SET1 and SET2
(Note 2) ..... (GND − 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current
OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... −25mA
Power Dissipation (Note 1) 200mW
Operating Temperature Range
ICL7665BCPA* ..... 0°C to +70°C
ICL7665BCTV* ..... 0°C to +70°C
ICL7665BCSO* ..... 0°C to +70°C
ICL7665BC/D* ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +160°C
Lead Temperature
(Soldering, 10 seconds) ..... +300°C

*Also applies to "A" version (Maxim).

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, T_A = +25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C −20°C ≤ T_A ≤ +70°C	1.6 1.8		16.0 16.0	V
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit V^+ = 2V V^+ = 9V V^+ = 15V		2.5 [illegible] [illegible]	10 10 15	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.1[illegible]	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	V_{SET} = 0V or V_{SET} [illegible]		10 −10	200 −100	nA
	I_{OLK} I_{HLK}	V^+ = 15V, T_A = [illegible]°C V^+ = 15V, [illegible]70°C			2000 −500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	V^+ = 2V, V_{SET1} = 0V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 0V, I_{OUT1} = 2mA V^+ = 15V, V_{SET1} = 0V, I_{OUT1} = 2mA		0.2 0.1 0.06	0.5 0.3 0.2	V
	V_{HYST1} V_{HYST1} V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 15V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.15 −0.05 −0.02	−0.3 −0.15 −0.10	
	V_{OUT2} V_{OUT2} V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 15V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.25	
	V_{HYST2} V_{HYST2} V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = −0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = −0.5mA V^+ = 15V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.25 −0.43 −0.35	−0.8 −1.0 −0.8	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±1		

Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND − 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

- ◆ 2% V_{SET} Threshold Accuracy (ICL7665A)
- ◆ Key Specifications Guaranteed over Temperature
- ◆ Improved Temperature Coefficient (ICL7665A)
- ◆ Significantly Improved ESD Protection (Note 1)
- ◆ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: ICL7665 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = 5V, T_A = +25°C, test circuit unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7665A MIN	ICL7665A TYP	ICL7665A MAX	ICL7665 MIN	ICL7665 TYP	ICL7665 MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C				1.6		16.0	V
		-20°C ≤ T_A ≤ +70°C				1.8		16.0	V
		0°C ≤ T_A ≤ +70°C	2.0		16.0				V
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit 0°C ≤ T_A ≤ +70°C (ICL7665A only)							
		V^+ = 2V		2.5	10		2.5	10	µA
		V^+ = 9V		2.6	10		2.6	10	µA
		V^+ = 15V		2.9	15		2.9	15	µA
Input Trip Voltage	V_{SET1}		1.275	1.3	1.325	1.15	1.3	1.45	V
	V_{SET2}		1.225	1.3	1.375	1.2	1.3	1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			100			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		.004			.004		%/V
Output Leakage Currents of OUT and HYST	I_{OLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10	200		10	200	nA
	I_{HLK}			-10	-100		-10	-100	nA
	I_{OLK}	V^+ = 15V, T_A = 70°C			2000			2000	nA
	I_{HLK}	V^+ = 15V, T_A = 70°C			-500			-500	nA
Output Saturation Voltages	V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2			0.2	0.5	V
	V_{OUT1}	V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.1	0.3		0.1	0.3	V
	V_{OUT1}	V^+ = 15V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.06	0.2		0.06	0.2	V
	V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = -0.5mA		-0.15	-0.3		-0.15	-0.3	V
	V_{HYST1}	V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = -0.5mA		-0.05	-0.15		-0.05	-0.15	V
	V_{HYST1}	V^+ = 15V, V_{SET1} = 2V, I_{HYST1} = -0.5mA		-0.02	-0.10		-0.02	-0.10	V
	V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2	0.5		0.2	0.5	V
	V_{OUT2}	V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.15	0.3		0.15	0.3	V
	V_{OUT2}	V^+ = 15V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.11	0.25		0.11	0.25	V
	V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = -0.2mA		-0.25	-0.8		-0.25	-0.8	V
	V_{HYST2}	V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = -0.5mA		-0.43	-1.0		-0.43	-1.0	V
	V_{HYST2}	V^+ = 15V, V_{SET2} = 2V, I_{HYST2} = -0.5mA		-0.35	-1.0		-0.35	-0.8	V
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		±0.01	±10		±0.01	±10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT} LO = 1% V^+, V_{OUT} HI = 99% V^+		0.1			1.0		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ		±5	±50		±5	±50	mV
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±0.1			±1		mV

Note 1: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Dual Over/Under Voltage Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ..... -0.3V to +12V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) ..... -0.3V to +12V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) ..... +0.3V to -12V
Input Voltages SET1 and SET2
(Note 2) ..... (GND - 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current
OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... -25mA

Power Dissipation (Note 1) 200mW
Operating Temperature Range
ICL7665BCPA ..... 0°C to +70°C
ICL7665BCTV ..... 0°C to +70°C
ICL7665BCSO ..... 0°C to +70°C
ICL7665BC/D ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature
(Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, ICL7665B

(V^+ = 5V, T_A = +25°C, test circuit unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C 0 ≤ T_A ≤ +70°C	1.6 1.8		10 10	V
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit V^+ = 2V V^+ = 9V		2.5 2.6	10 10	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			±200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10 -10	200 -100	nA
	I_{OLK} I_{HLK}	V^+ = 9V, T_A = 70°C V^+ = 9V, T_A = 70°C			2000 -500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 9V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2 0.1 0.06	0.5 0.3 0.25	V
	V_{HYST1} V_{HYST1} V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = -0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = -0.5mA V^+ = 9V, V_{SET1} = 2V, I_{HYST1} = -0.5mA		-0.15 -0.05 -0.02	-0.3 -0.15 -0.15	
	V_{OUT2} V_{OUT2} V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 9V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.3	
	V_{HYST2} V_{HYST2} V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = -0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = -0.5mA V^+ = 9V, V_{SET2} = 2V, I_{HYST2} = -0.5mA		-0.25 -0.43 -0.35	-0.8 -1 -1	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±1		

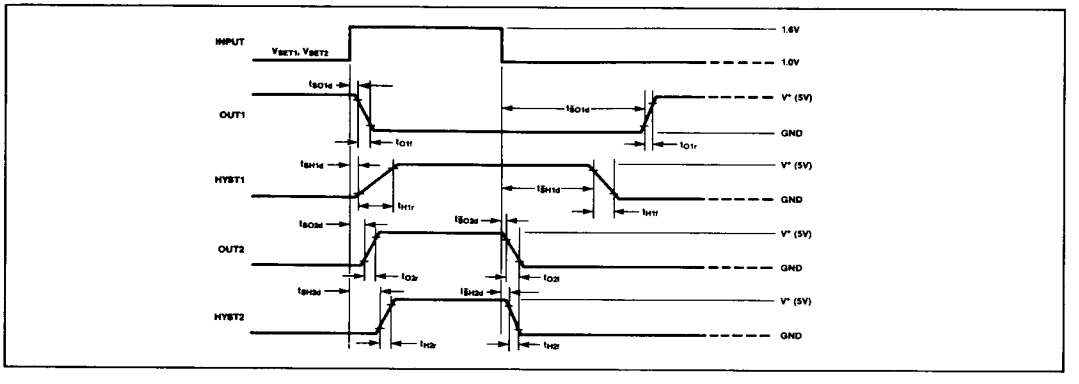
Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

AC OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Delay Times Input Going HI	t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	V_{SET} Switched from 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		85 90 55 55		µS
Input Going LO	$t_{\overline{SO}1d}$ $t_{\overline{SH}1d}$ $t_{\overline{SO}2d}$ $t_{\overline{SH}2d}$	V_{SET} Switched from 1.6V to 1.0V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		75 80 60 60		µS
Output Rise Times	t_{O1r} t_{O2r} t_{H1r} t_{H2r}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		0.6 0.8 7.5 0.7		µS
Output Fall Times	t_{O1f} t_{O2f} t_{H1f} t_{H2f}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		0.6 0.7 4 1.8		µS

Switching Waveforms



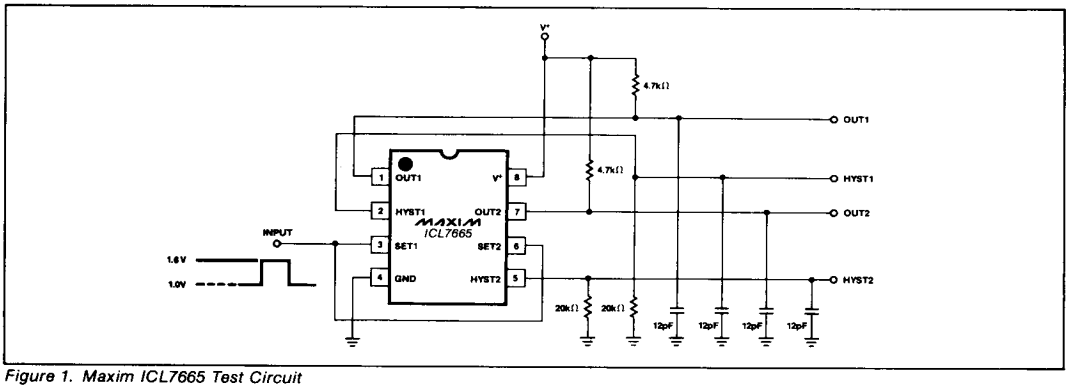
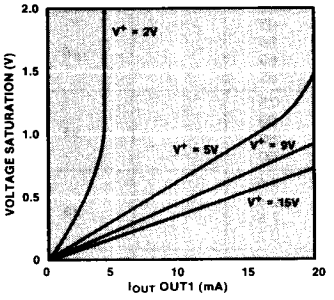


Figure 1. Maxim ICL7665 Test Circuit

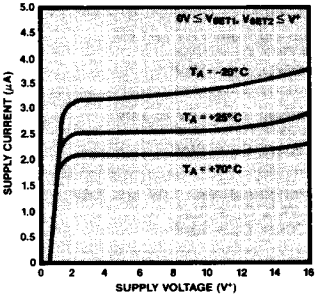
Dual Over/Under Voltage Detector

Typical Operating Characteristics

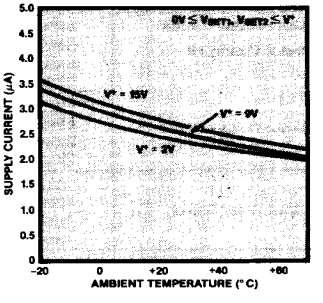
OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



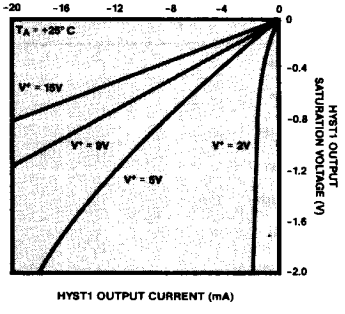
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



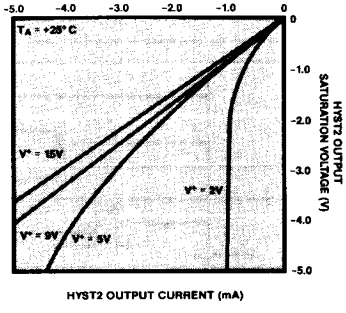
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



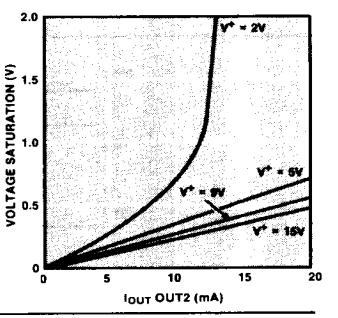
HYST1 OUTPUT SATURATION VOLTAGE vs HYST1 OUTPUT CURRENT



HYST2 OUTPUT SATURATION VOLTAGE vs HYST2 OUTPUT CURRENT



OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



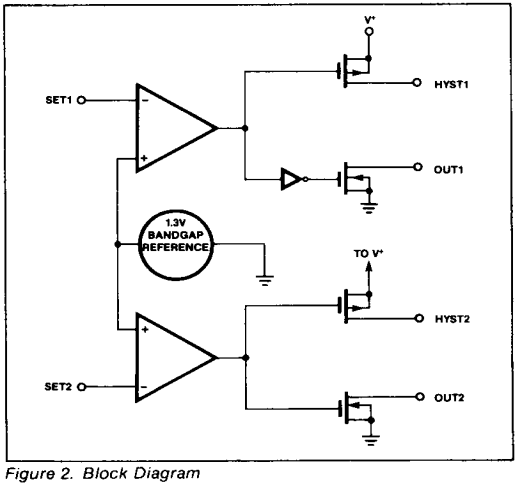


Figure 2. Block Diagram

Table I: ICL7665 TRUTH TABLE

INPUT*	OUTPUT	HYSTERESIS
V_{SET1} > 1.3V	OUT1 = ON = LOW	HYST1 = ON = HI
V_{SET1} < 1.3V	OUT = OFF = HI	HYST1 = OFF = LOW
V_{SET2} > 1.3V	OUT2 = OFF = HI	HYST2 = ON = HI
V_{SET2} < 1.3V	OUT2 = ON = LOW	HYST2 = OFF = LOW

OUT1 is an inverting output, all others are non-inverting.
OUT1 and OUT2 are open drain N-channel current sinks.
HYST1 and HYST2 are open drain P-channel current sources.
*See Electrical Characteristics for exact input threshold range.

Detailed Description

As shown in the block diagram of Figure 2, the Maxim ICL7665 combines a 1.3V reference with two comparators, two open drain n-channel outputs, and two open drain p-channel hysteresis outputs. The reference and comparator are very low power linear CMOS circuits, with a total operating current of 10μA maximum, 3μA typical. The n-channel outputs can sink greater than 10mA but are unable to source any current. These outputs are suitable for wired OR connections and capable of driving TTL inputs when an external pullup resistor is added.

The ICL7665 Truth Table is shown in Table I. OUT1 is an inverting output, all other outputs are non-inverting. HYST1 and HYST2 are p-channel current sources whose sources are connected to V+. OUT1 and OUT2 are n-channel current sinks with their sources connected to ground. Both OUT1 and OUT2 can drive at least one TTL load with a V_{OL} of 0.4V.

In spite of the very low operating current, the ICL7665 has a typical propagation delay of only 75μs. Since the comparator input bias current and the output leakages are very low, high impedance external resistors can be used. This design feature minimizes both the total supply current used and loading on the voltage source that is being monitored.

Basic Over/Under-Voltage Detection Circuits

Figures 3, 4, and 5 show the three basic voltage detection circuits.

The simplest circuit, depicted in Figure 3, does not have any hysteresis. The comparator trip point formulas can easily be derived by observing that the comparator changes state when the V_{SET} input is 1.3V. The external resistors are simply a voltage divider that attenuates the input signal. This ensures that the V_{SET} terminal is at 1.3V when the input voltage is at the desired comparator trip point. Since the bias current of the comparator is only a fraction of a nA the current in the voltage divider can be less than one μA without losing accuracy due to bias currents. The ICL7665A has a 2% threshold accuracy at 25°C and a typical temperature coefficient of 100 ppm/°C including comparator offset drift, eliminating the need for external potentiometers in most applications.

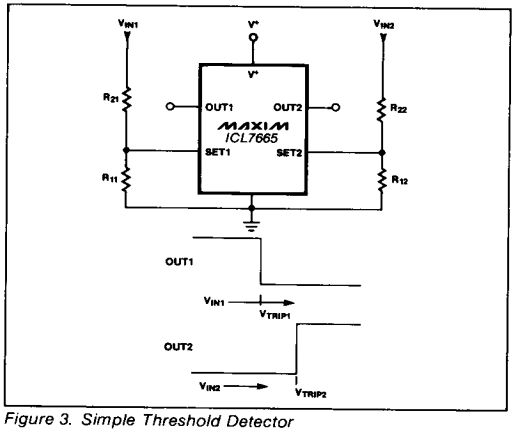


Figure 3. Simple Threshold Detector

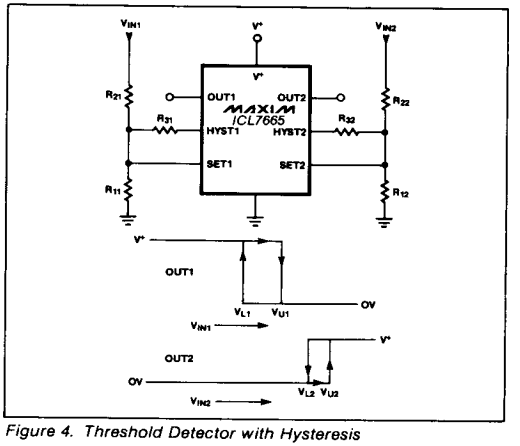


Figure 4. Threshold Detector with Hysteresis

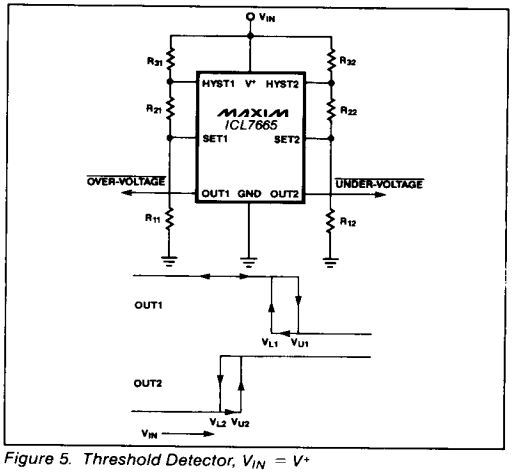


Figure 5. Threshold Detector, V_{IN} = V+

Dual Over/Under Voltage Detector

Figure 4 adds another resistor to each voltage detector. This third resistor supplies current from the HYST output whenever the V_{SET} input is above the 1.3V threshold. As the formulas show, this hysteresis resistor affects only the lower trip point. Hysteresis (defined as the difference between the upper and lower trip points) keeps noise or small variations in the input signal from repeatedly switching the output when the input signal remains near the trip point for a long period of time.

The third basic circuit (Figure 5), is suitable only when the voltage to be detected is also the power supply voltage for the ICL7665. This circuit has the advantage that all of the current flowing through the input divider resistors flows through the hysteresis resistor. This allows the use of higher value resistors without hysteresis output leakage having an appreciable effect on the trip point.

Resistor Value Calculations

Figure 3

1) First choose a value for R11. The value of R11 determines the amount of current flowing through the input divider, equal to $V_{SET}/R11$. R11 can typically be in the range of 10kΩ to 10MΩ.

2) Choose R21 based on the previously chosen R11 and the desired trip point.

$$R21 = R11 \times \frac{V_{TRIP} - V_{SET}}{V_{SET}} = R11 \times \frac{V_{TRIP} - 1.3V}{1.3V}$$

Figure 4

1) Choose a resistor value for R11. Typical values are in the 10kΩ to 10MΩ range.

2) Calculate R21 for the desired upper trip point, V_U using the formula

$$R21 = R11 \times \frac{V_U - V_{SET}}{V_{SET}} = R11 \times \frac{V_U - 1.3V}{1.3V}$$

3) Calculate R31 for the desired amount of hysteresis:

$$R31 = \frac{R21 \times (V^+ - V_{SET})}{V_U - V_L} = \frac{R21 \times (V^+ - 1.3V)}{V_U - V_L}$$

or if $V^+ = V_{IN}$:

$$R31 = \frac{R21 \times (V_L - V_{SET})}{V_U - V_L} = \frac{R21 \times (V_L - 1.3V)}{V_U - V_L}$$

4) The trip voltages are not affected by the absolute value of the resistors as long as the impedances are high enough that the resistance of R31 is much greater than the HYST output's resistance and the current through R31 is much higher than the HYST output's leakage current. Normally R31 will be in the 100kΩ to 22MΩ range. Multiplying or dividing all three resistors by the same factor will not affect the trip voltages.

Figure 5

1) First select a value for R11, usually between 10kΩ and 10MΩ.

2) Calculate R21.

$$R21 = R11 \times \frac{V_L - V_{SET}}{V_{SET}} = R11 \times \frac{V_L - 1.3V}{1.3V}$$

3) Calculate R31

$$R31 = R11 \times \frac{V_U - V_L}{V_{SET}}$$

4) As in the other circuits, all three resistor values may be scaled up or down in value without changing V_U and V_L. V_U and V_L depend only on the ratio of the three resistors if the absolute values are such that the hysteresis output resistance and the leakage currents of the V_{SET} input and hysteresis output can be ignored.

Typical Applications

Fault Monitor for a Single Supply

Figure 6 shows a typical over/under-voltage fault monitor for a single supply. In this case the upper trip points (controlling OUT1) are centered on 5.5V, with 100mV of hysteresis (V_U = 5.55V, V_L = 5.45V); and the lower trip points (controlling OUT2) are centered on 4.5V, also with 100mV of hysteresis. OUT1 and OUT2 are connected together in a wired OR configuration to generate a Power OK signal.

Multiple Supply Fault Monitor

The ICL7665 can simultaneously monitor several power supplies, as shown in Figure 7. The easiest way to calculate the resistor values is to note that when the V_{SET} input is at the trip point (1.3V), the current through R11 is 1.3V/R11. The sum of the currents through R21A, R21B and R31 must equal this current when the two input voltages are at the desired low voltage detection point. Ordinarily R21A and R21B are chosen so that the current through the two resistors is equal. Note that since the voltage at the ICL7665 V_{SET} input depends on the voltage of both supplies being monitored, there will be some interaction between the low voltage trip points for the two supplies. In this example OUT1 will go low when either supply is 10% below nominal (assuming the other supply is at the nominal voltage), or when both supplies are 5% or more below their nominal voltage. R31 sets the hysteresis, in this case, to about 43mV at the 5V supply or 170mV at the 15V supply. The second section of the ICL7665 can be used to detect overvoltage, or as shown in Figure 7, can be used to detect the absence of negative supplies. Note that the trip points for OUT2 depend on both the voltages of the negative power supplies and the actual voltage of the +5V supply.

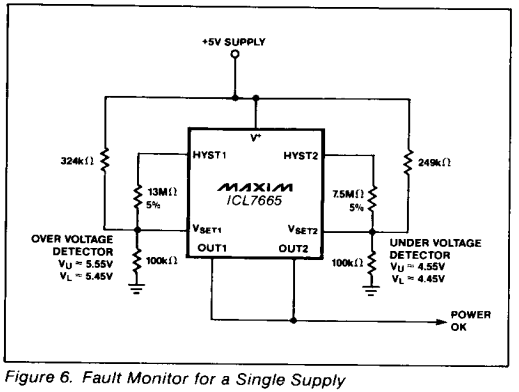


Figure 6. Fault Monitor for a Single Supply

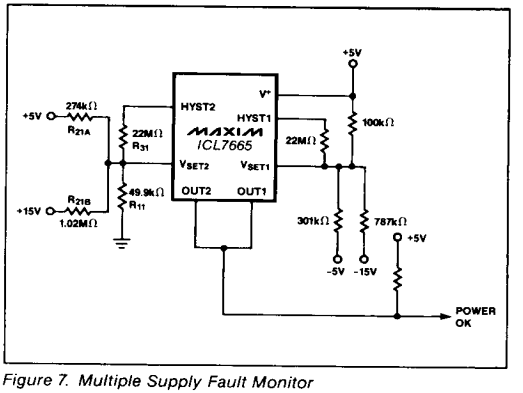


Figure 7. Multiple Supply Fault Monitor

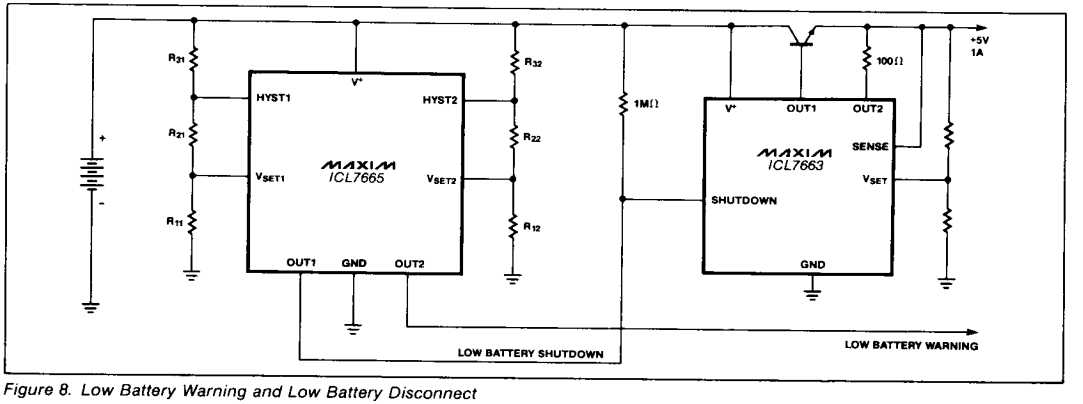


Figure 8. Low Battery Warning and Low Battery Disconnect

Combination Low Battery Warning and Low Battery Disconnect

Nickel Cadmium (NiCad) batteries are excellent rechargeable power sources for portable equipment, but care must be taken to ensure that NiCad batteries are not damaged by overdischarge. Specifically, a NiCad battery should not be discharged to the point where the polarity of lowest capacity cell is reversed and that cell is reverse charged by the higher capacity cells. This reverse charging will dramatically reduce the life of a NiCad battery. Figure 8 both prevents reverse charging and also gives a low battery warning. A typical low battery warning voltage is 1V per cell. Since a NiCad "9V" battery is ordinarily made up of 6 cells with a nominal voltage of 7.2V, a low battery warning of 6V is appropriate, with a small hysteresis of 100mV. To prevent overdischarge of a battery the load should be disconnected when the battery voltage is 1V x (N-1), where N = number of cells. In this case the low battery load disconnect should occur at 5V. Since the battery voltage will rise when the load is disconnected, 800mV of hysteresis is used to prevent repeated on-off cycling.

Power Fail Warning and Powerup/Powerdown Reset

Figure 9 illustrates a power fail warning circuit which monitors raw DC input voltage to the 7805 three terminal 5V regulator. The Power Fail warning signal goes high when the unregulated DC input falls below 8.0V. When the raw DC power source is disconnected or the AC power fails, the voltage on the input of the 7805 decays at a rate of I_{OUT}/C (in this case 200mV/ms). Since the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will give at least 3.5ms of warning before the 5V output begins to drop. If additional warning time is needed,

Dual Over/Under Voltage Detector

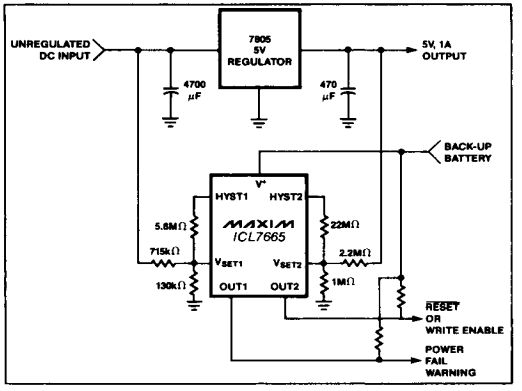


Figure 9. Power Fail Warning and Powerup/Powerdown Reset

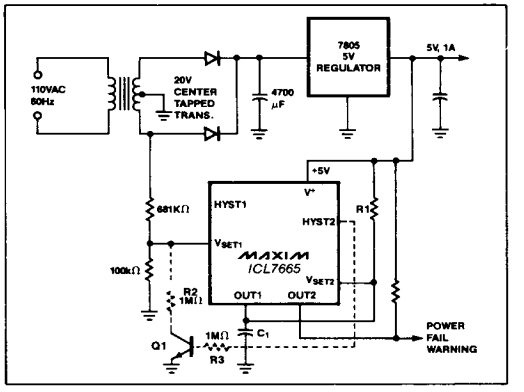


Figure 10. AC Power Fail and Brownout Detector

either the trip voltage or filter capacitance should be increased or the output current should be decreased.

The ICL7665 OUT2 is set to trip when the 5V output has decayed to 3.9V. This output can be used to prevent the microprocessor from writing spurious data to a CMOS battery backup memory, or can be used to activate a battery backup system.

AC Power Fail and Brownout Detector

By monitoring the secondary of the transformer, the circuit in Figure 10 performs the same power failure warning function as Figure 9. With a normal 110VAC input to the transformer, OUT1 will discharge C1 every 16.7ms when the peak transformer secondary voltage exceeds 10.2V. When the 110VAC power line voltage is either interrupted or reduced so that the peak voltage is less than 10.2V, C1 will be charged through R1. OUT2, the Power Fail Warning output, goes high when the voltage on C1 reaches 1.3V. The time constant R1 x C1 determines the delay time before the Power Fail Warning signal is activated, in this case 42ms or 2½ line cycles. Optional components R2, R3 and Q1 add hysteresis by increasing the peak secondary voltage required to discharge C1 once the Power Fail Warning is active.

Battery Switchover Circuit

The circuit in Figure 11 performs two functions: switching the power supply of a CMOS memory to a backup battery when the line-powered supply is turned off, and lighting a low-battery-warning LED when the backup battery is nearly discharged. The PNP transistor, Q1, connects the line-powered +5V to the CMOS memory whenever the line-powered +5V supply voltage is greater than 3.5V. The voltage drop across Q1 will only be a couple of hundred mV since it will be saturated. Whenever the input voltage falls below 3.5V. OUT1 goes high, turns off Q1 and connects the 3V lithium cell to the CMOS memory.

The second voltage detector of the ICL7665 monitors the voltage of the lithium cell. If the battery voltage falls below 2.6V, OUT2 goes low and the low-battery-warning LED turns on (assuming that the +5V is present, of course).

Another possible use for the second section of the ICL7665 is the detection of the input voltage falling below 4.5V. This signal could then be used to prevent the microprocessor from writing spurious data to the CMOS memory while its power supply voltage is outside its guaranteed operating range.

Simple High/Low Temperature Alarm

The circuit in Figure 12 is a simple high/low temperature alarm which uses a low cost NPN transistor as the sensor and an ICL7665 as the high/low detector. The NPN transistor and potentiometer R1 form a Vbe multiplier whose output voltage is determined by the Vbe of the transistor and the position of R1's wiper arm. The voltage at the top of R1 will have a temperature coefficient of approximately -5mV/°C. R1 is set so that the voltage at V_{SET2} is equal to the V_{SET2} trip voltage when the temperature of the NPN transistor reaches the temperature selected for the high temperature alarm desired. R2 can be adjusted so that the voltage at V_{SET1} is 1.3V when the NPN transistor's temperature reaches the low temperature limit.

SCR Latchup

Like all junction isolated CMOS circuits, the ICL7665 has an inherent 4 layer or SCR structure that can be triggered into destructive latchup under certain conditions. Avoid destructive latchup by following these precautions:

1) If either V_{SET} terminal can be driven to a voltage greater than V^+ or less than ground, limit the input current to 500µA maximum. Usually an input voltage

divider resistance can be chosen to ensure the input current remains below 500μA, even when the input voltage is applied before the ICL7665 V+ supply is connected.

2) Limit the rate-of-rise of V+ by using a bypass capacitor near the ICL7665. Rate-of-rise SCRs rarely occur unless: a) the battery has a low impedance — as is the case with NiCad and lead acid batteries; b) the battery is connected directly to the ICL7665 or is switched on via a mechanical switch with low resistance and c) there is little or no input filter capacitance near the ICL7665. In line-powered systems the rate-of-rise is usually limited by other factors and will not cause a rate-of-rise SCR action under normal circumstances.

3) Limit the maximum supply voltage (including transient spikes) to 18V. Likewise limit the maximum voltage on OUT1 and OUT2 to +18V and the maximum voltage on HYST1 and HYST2 to 18V below V+.

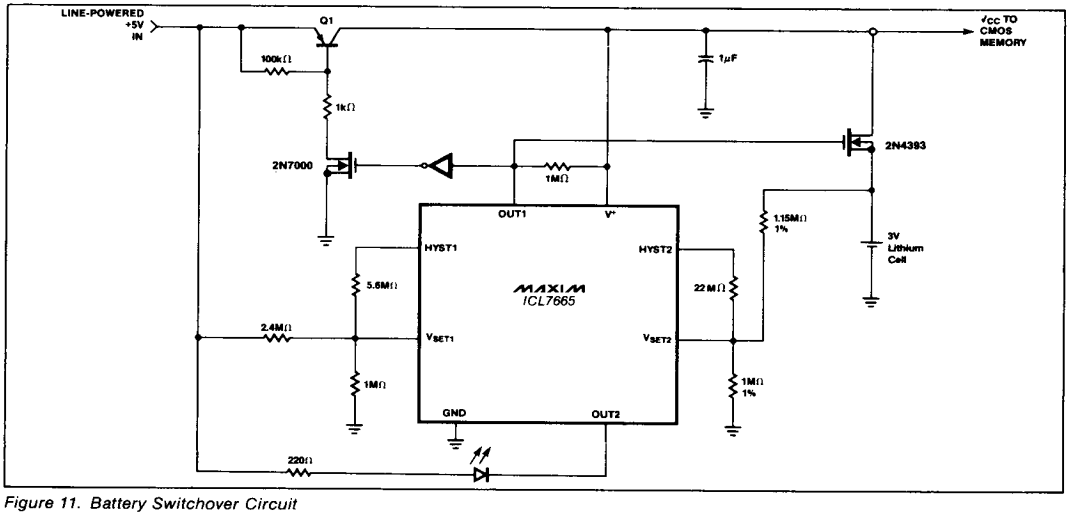


Figure 11. Battery Switchover Circuit

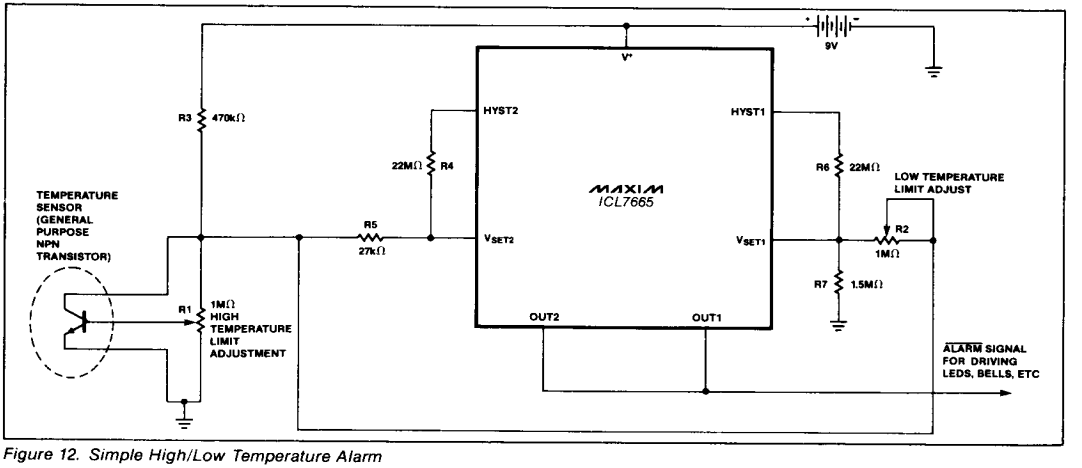
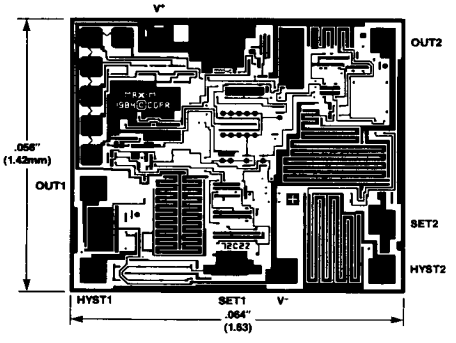


Figure 12. Simple High/Low Temperature Alarm

Dual Over/Under Voltage Detector

Chip Topography



027141