

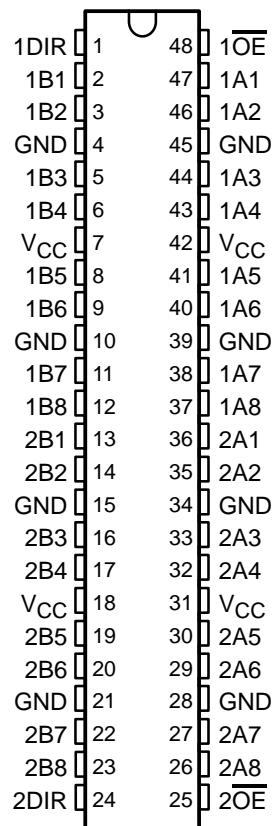
- Member of Texas Instruments' Widebus™ Family
- State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation
- Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot
- Industry Standard '16245 Pinout
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout

### description

The SN74ALB16245 is a 16-bit transceiver designed for high-speed, low-voltage (3.3-V) V<sub>CC</sub> operation. This device is intended to replace the conventional transceiver in any speed-critical path. The small propagation delay is achieved using a unity-gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ALB16245DL	ALB16245
		Tape and reel	SN74ALB16245DLR	
	TSSOP – DGG	Tape and reel	SN74ALB16245DGG	ALB16245
	TVSOP – DGV	Tape and reel	SN74ALB16245DGV	AV245

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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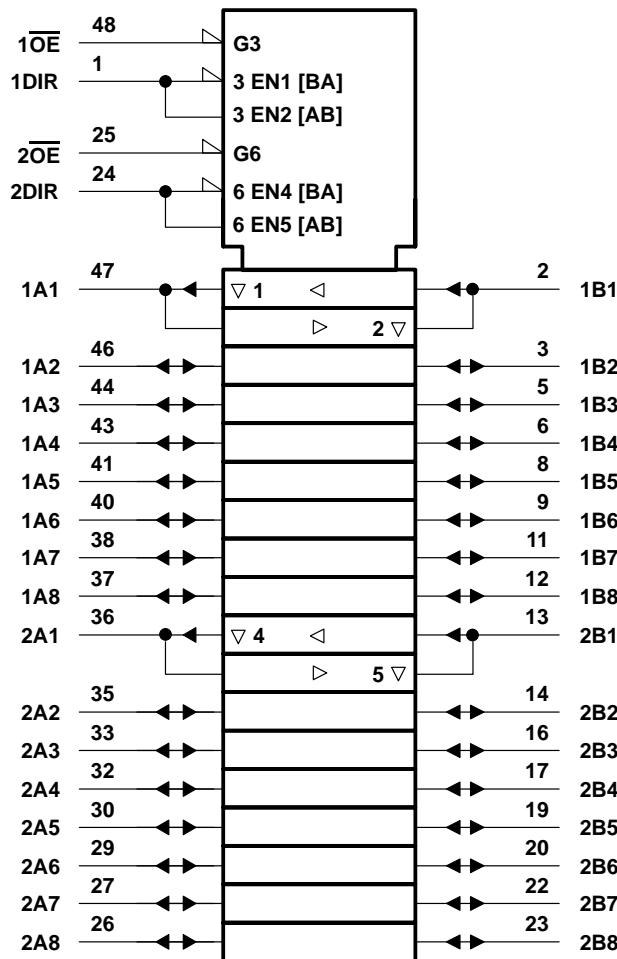
**SN74ALB16245**  
**3.3-V ALB 16-BIT TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

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FUNCTION TABLE  
(each 8-bit section)

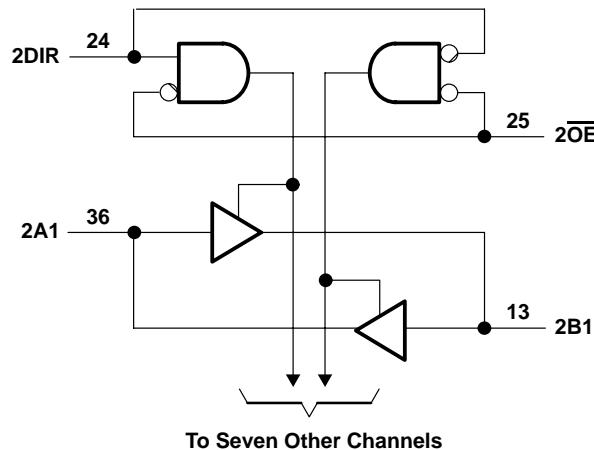
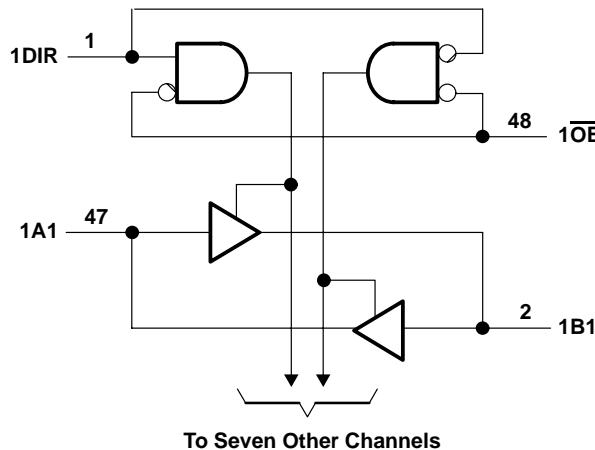
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	.....	-0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1)	.....	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	.....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	±50 mA
Continuous current through each $V_{CC}$ or GND	.....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):		
DGG package	.....	70°C/W
DGV package	.....	58°C/W
DL package	.....	63°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

### **recommended operating conditions**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.6	V
I <sub>OH</sub> <sup>‡</sup>	High-level output current		-25	mA
I <sub>OL</sub> <sup>‡</sup>	Low-level output current		25	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	5	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85 °C

<sup>‡</sup> See Figures 1 and 2 for typical I/O ranges.

**SN74ALB16245**  
**3.3-V ALB 16-BIT TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	A or B ports	V <sub>CC</sub> = 3 V	I <sub>I</sub> = 18 mA			3.7	V <sub>CC</sub> +1.2	V
			I <sub>I</sub> = -18 mA			-0.9	-1.2	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND			±10	μA	
	A or B ports	V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = V <sub>CC</sub>	OE low	0.4	0.6	mA	
				OE high	25	25	μA	
			V <sub>I</sub> = 0	OE low	-0.7	-1	mA	
				OE high	-60	-60	μA	
I <sub>OZH</sub>		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V		0.7	20	μA	
I <sub>OZL</sub>		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V		-0.2	-50	μA	
I <sub>CC</sub> /buffer		V <sub>CC</sub> = 3.6 V,	I <sub>O</sub> = 0,	V <sub>I</sub> = V <sub>CC</sub> or GND	3.7	5.6	mA	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6 V,	Control inputs = V <sub>CC</sub> or GND			0.8	mA	
ΔI <sub>CC</sub> ‡		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND			600	600	μA	
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0			3.5	3.5	pF	
C <sub>io</sub>		V <sub>O</sub> = 3 V or 0			7.5	7.5	pF	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V			UNIT
			MIN	TYP†	MAX	
t <sub>pd</sub>	A or B	B or A	0.6	1.3	2	ns
t <sub>en</sub>	OE	A or B	1.5	3.2	6	ns
t <sub>dis</sub>	OE	A or B	1.8	2.8	4.2	ns

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

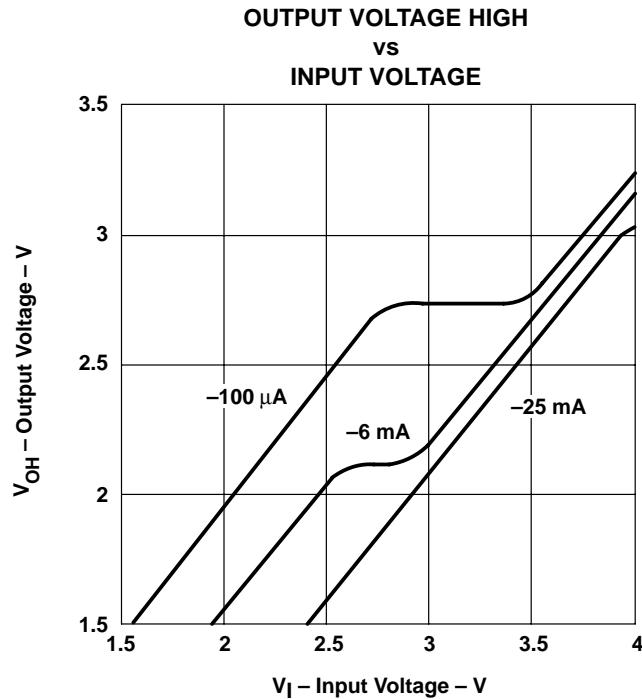


Figure 1.  $V_{OH}$  Over Recommended Free-Air Temperature Range

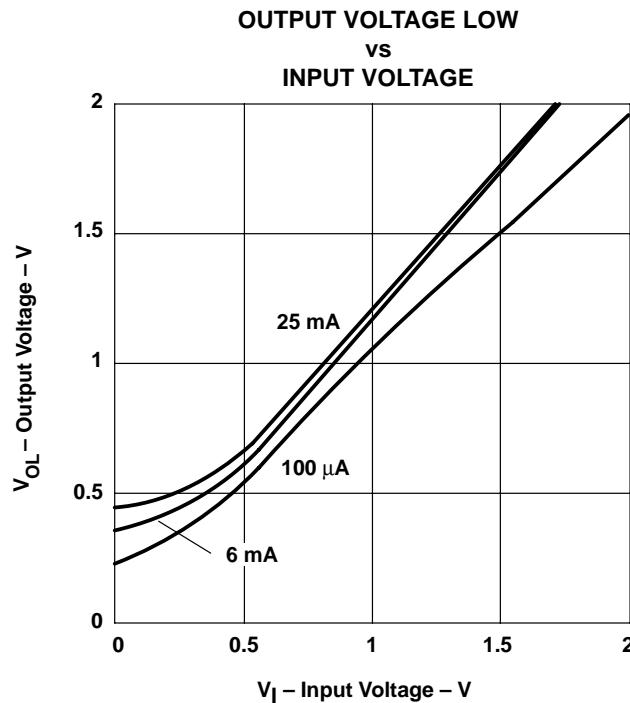
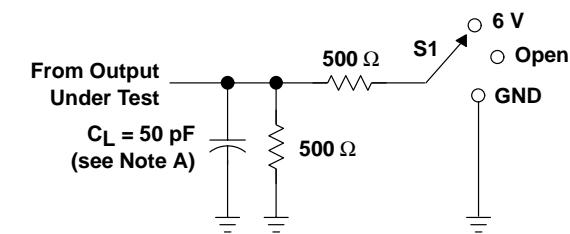


Figure 2.  $V_{OL}$  Over Recommended Free-Air Temperature Range

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**3.3-V ALB 16-BIT TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

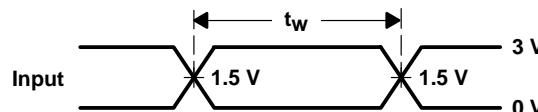
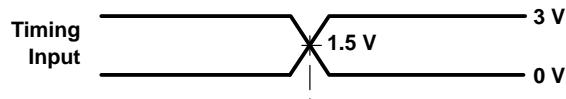
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**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

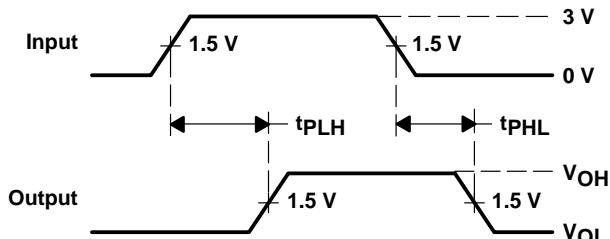
LOAD CIRCUIT



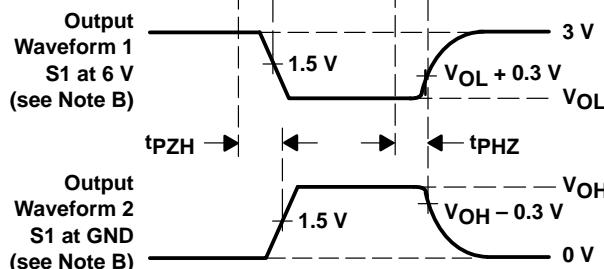
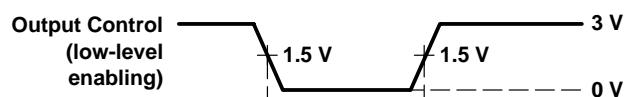
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PLZ}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ALB16245DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALB16245DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALB16245DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALB16245DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16245DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16245DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16245DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16245DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

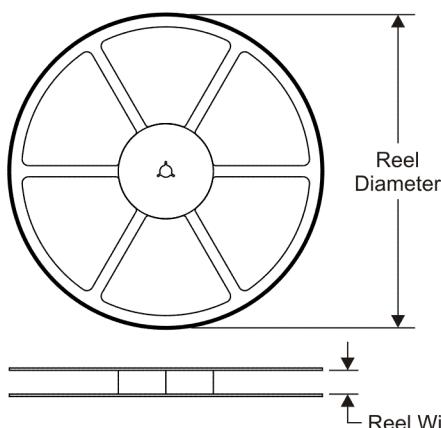
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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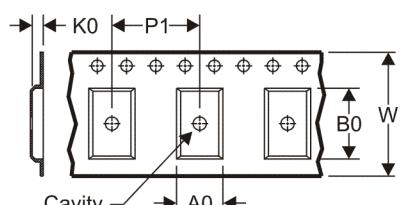
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## TAPE AND REEL INFORMATION

## REEL DIMENSIONS

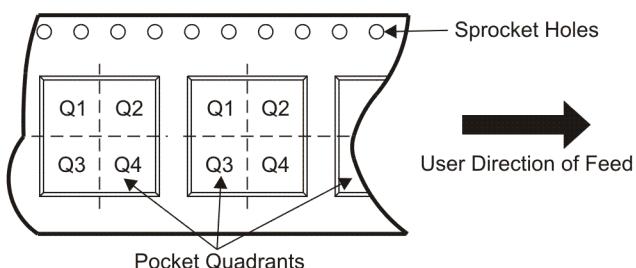


## TAPE DIMENSIONS



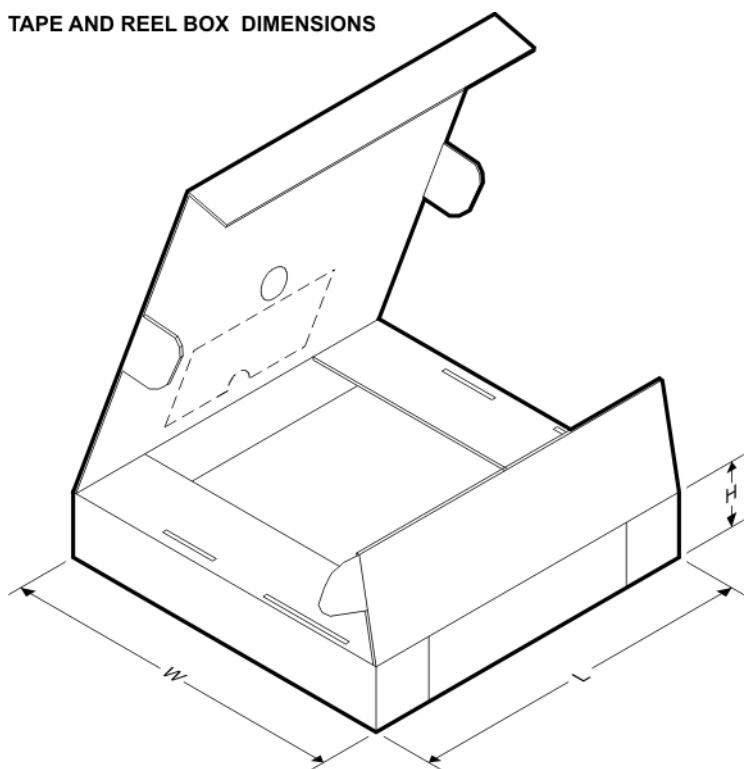
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALB16245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALB16245DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ALB16245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


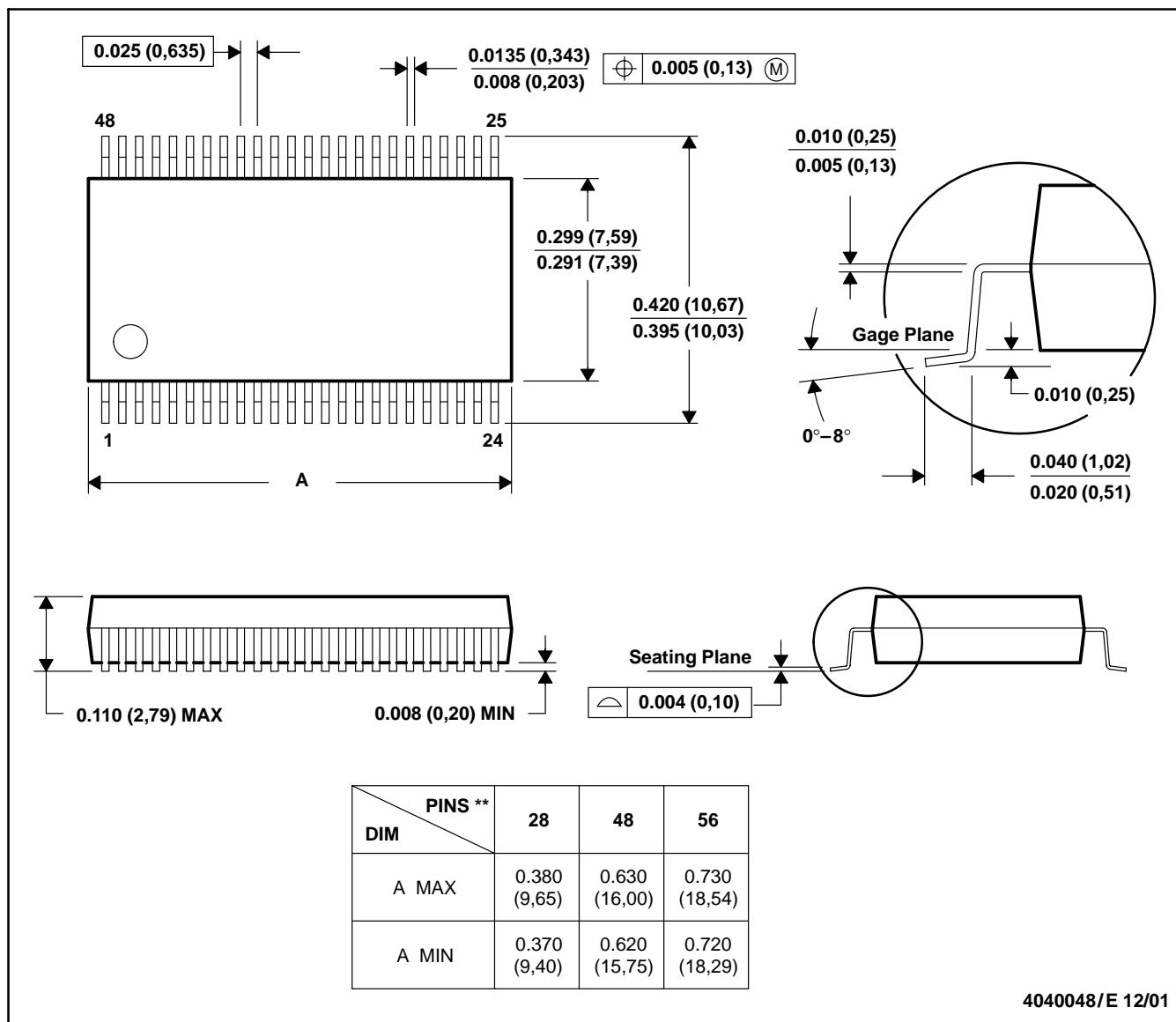
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALB16245DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ALB16245DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0
SN74ALB16245DLR	SSOP	DL	48	1000	346.0	346.0	49.0

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

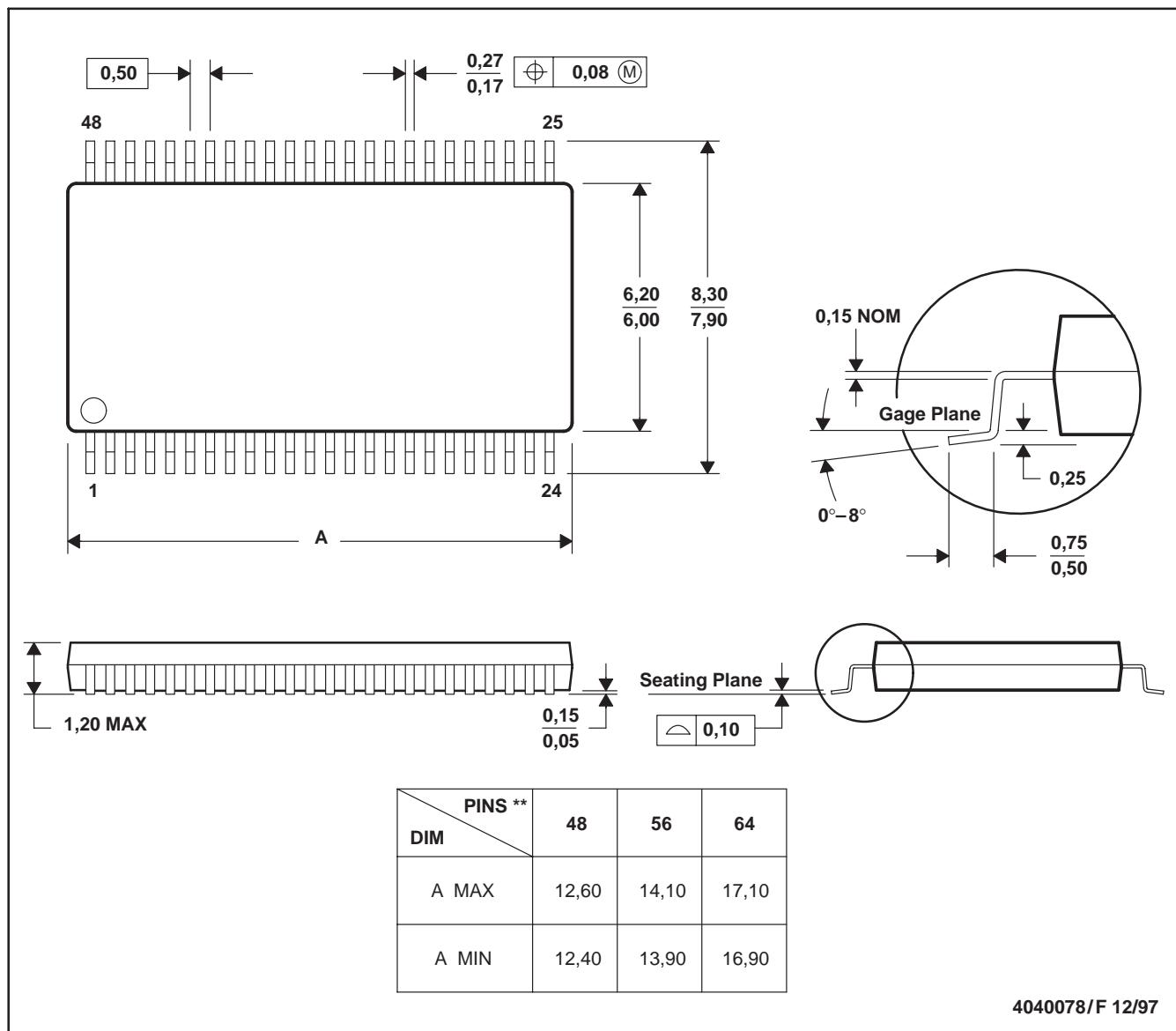


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

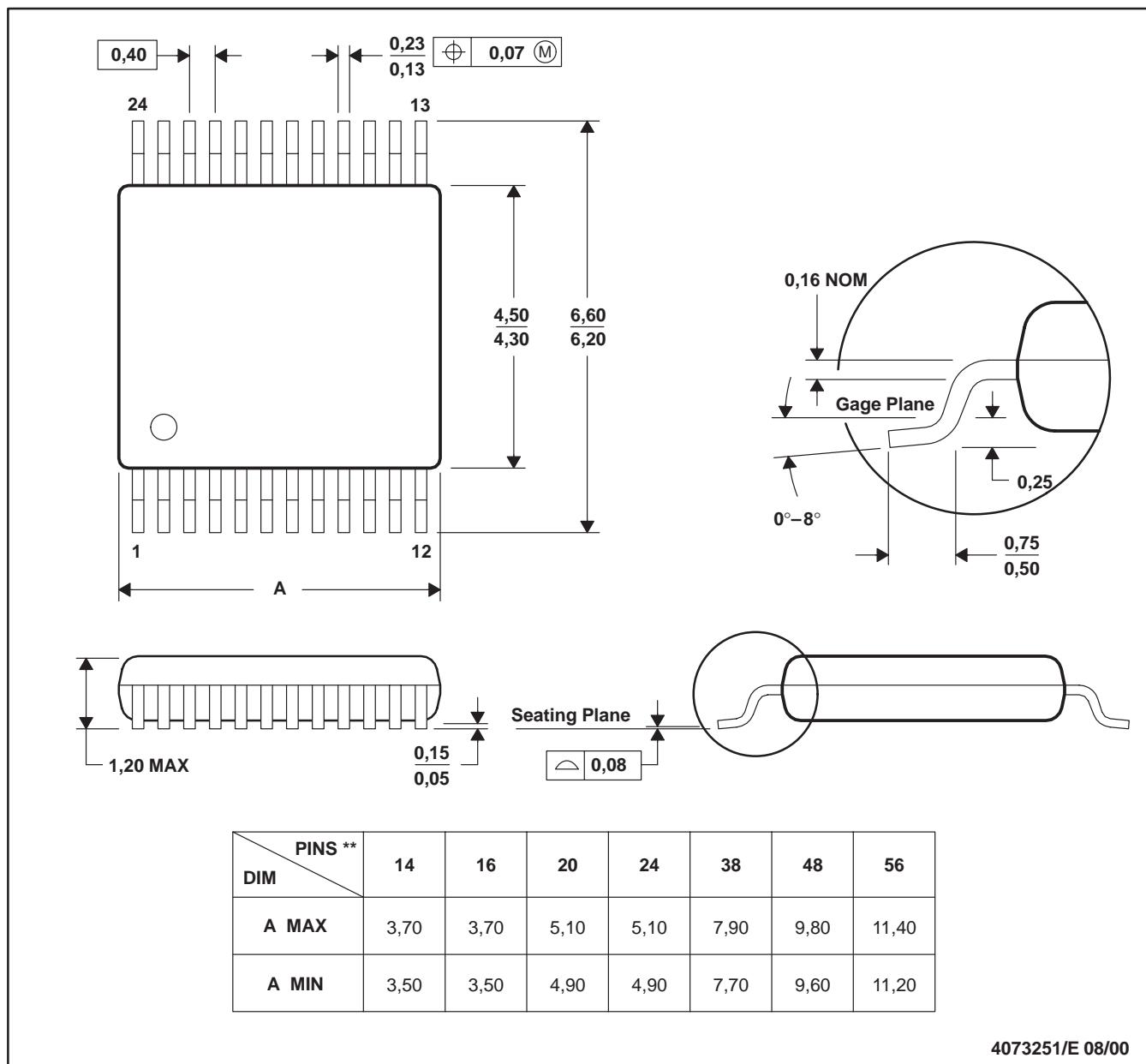


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

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