

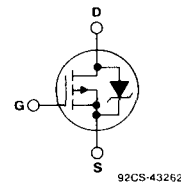
Avalanche-Energy-Rated P-Channel Power MOSFETs

-10A, and -12A, -60V and -100V
 $r_{DS(on)} = 0.30\Omega$ and 0.40Ω

Features:

- Single pulse avalanche energy rated
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance

TERMINAL DIAGRAM

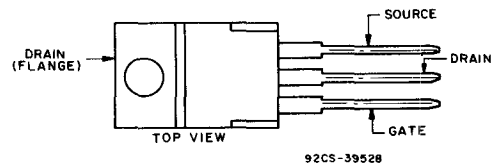


P-CHANNEL ENHANCEMENT MODE

The IRF9530, IRF9531, IRF9532 and IRF9533 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION

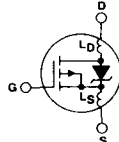


JEDEC TO-220AB

Absolute Maximum Ratings

Parameter	IRF9530	IRF9531	IRF9532	IRF9533	Units
V_{DS} Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ k}\Omega$) ①	-100	-60	-100	-60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	-12	-12	-10	-10	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	-7.5	-7.5	-6.5	-6.5	A
I_{DM} Pulsed Drain Current ③	-48	-48	-40	-40	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{AS} Single Pulse Avalanche Energy ④	500				mJ
T_J Operating Junction and Storage Temperature Range	-55 to 150				°C
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

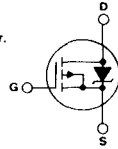
IRF9530, IRF9531, IRF9532, IRF9533
Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain-Source Breakdown Voltage		IRF9530	-100	-	-	V	V _{GS} = 0V	
		IRF9532						
		IRF9531	-60	-	-	V	I _D = -250μA	
		IRF9533						
V _{GS(th)} Gate Threshold Voltage		ALL	-2.0	-	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA	
I _{GSS} Gate-Source Leakage Forward		ALL	-	-	500	nA	V _{GS} = -20V	
I _{GSS} Gate-Source Leakage Reverse		ALL	-	-	500	nA	V _{GS} = 20V	
I _{DSS} Zero Gate Voltage Drain Current		ALL	-	-	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
			-	-	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②		IRF9530	-12	-	-	A	V _{DS} > I _{D(on)} x R _{DS(on)} max.; V _{GS} = 10V	
		IRF9531						
		IRF9532	-10	-	-	A		
		IRF9533						
R _{DS(on)} Static Drain-Source On-State Resistance ②		IRF9530	-	0.25	0.30	Ω	V _{GS} = -10V, I _D = -6.5A	
		IRF9531						
		IRF9532	-	0.30	0.40	Ω		
		IRF9533						
g _{fs} Forward Transconductance ②		ALL	2.0	3.8	-	S (l)	V _{DS} > I _{D(on)} x R _{DS(on)} max.; I _D = 6.5A	
C _{iss} Input Capacitance		ALL	-	500	-	pF	V _{GS} = 0V, V _{DS} = -25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance		ALL	-	300	-	pF		
C _{rss} Reverse Transfer Capacitance		ALL	-	100	-	pF		
t _{d(on)} Turn-On Delay Time		ALL	-	30	60	ns	V _{DD} = 0.5 BV _{DSS} , I _D = -6.5A, Z _o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time		ALL	-	70	140	ns		
t _{d(off)} Turn-Off Delay Time		ALL	-	70	140	ns		
t _f Fall Time		ALL	-	70	140	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)		ALL	-	25	45	nC	V _{GS} = -15V, I _D = -15A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge		ALL	-	13	23	nC		
Q _{gd} Gate-Drain ("Miller") Charge		ALL	-	12	22	nC		
L _D Internal Drain Inductance		ALL	-	3.5	-	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	Modified MOSFET symbol showing the internal device inductances. 
			-	4.5	-	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance		ALL	-	7.5	-	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

Thermal Resistance

R _{jc} Junction-to-Case	ALL	-	-	1.67	$^\circ\text{C/W}$	
R _{gs} Case-to-Sink	ALL	-	1.0	-	$^\circ\text{C/W}$	Mounting surface flat, smooth, and greased.
R _{ja} Junction-to-Ambient	ALL	-	-	80	$^\circ\text{C/W}$	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I _S	Continuous Source Current (Body Diode)	IRF9530 IRF9531	-	-	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	
		IRF9532 IRF9533	-	-	-10	A		
I _{SM}	Pulse Source Current (Body Diode) ③	IRF9530 IRF9531	-	-	-48	A		
		IRF9532 IRF9533	-	-	-40	A		
V _{SD}	Diode Forward Voltage ②	IRF9530 IRF9531	-	-	-1.5	V	T _C = 25°C, I _S = -12A, V _{GS} = 0V	
		IRF9532 IRF9533	-	-	-1.5	V	T _C = 25°C, I _S = -10A, V _{GS} = 0V	
t _{rr}	Reverse Recovery Time	ALL	-	300	-	ns	T _J = 150°C, I _F = -12A, dI _F /dt = 100 A/μs	
Q _{RR}	Reverse Recovered Charge	ALL	-	1.8	-	μC	T _J = 150°C, I _F = -12A, dI _F /dt = 100 A/μs	
t _{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .					

 ① T_J = 25 $^\circ$ C to 150 $^\circ$ C.

 ② Pulse Test: Pulse width $\leq$ 300 μ s.
Duty Cycle $\leq$ 2%.

 ③ Repetitive Rating: Pulse width limited by maximum junction temperature.
See Transient Thermal Impedance Curve (Fig. 5).

 ④ V_{DD} = 25V. Starting T_J = 25 $^\circ$ C, L = 5.2 mH,
R_g = 25 Ω , Peak I_L = 12A, (See Fig. 15 and 16).

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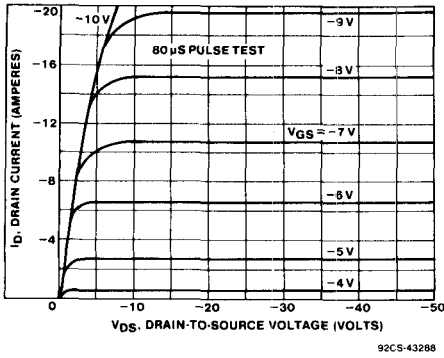


Fig. 1 - Typical Output Characteristics

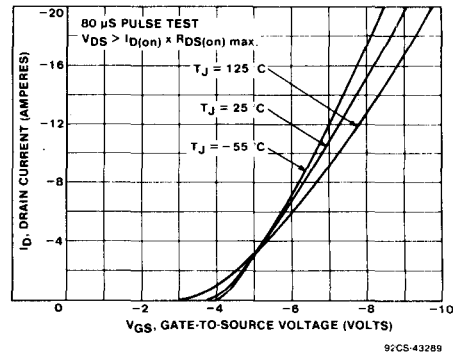


Fig. 2 - Typical Transfer Characteristics

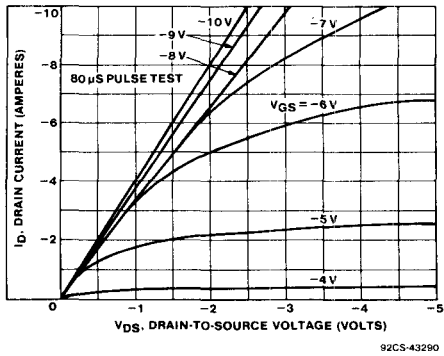


Fig. 3 - Typical saturation characteristic.

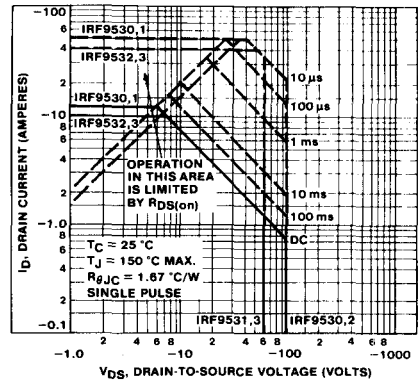


Fig. 4 - Maximum safe operating area.

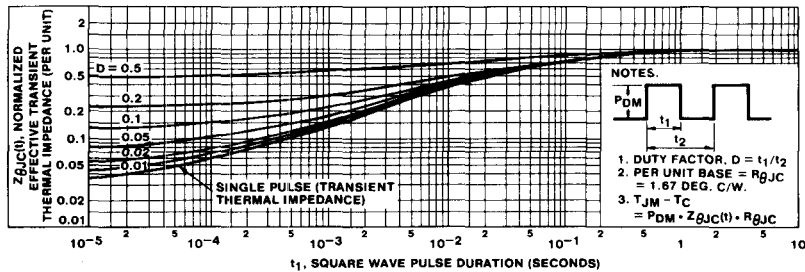


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

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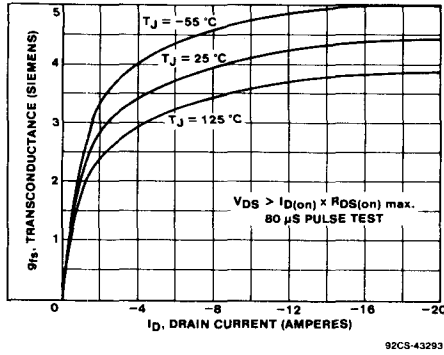


Fig. 6 - Typical transconductance vs. drain current.

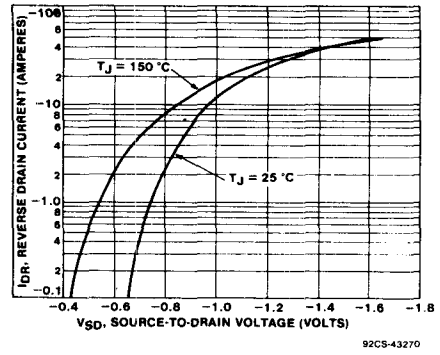


Fig. 7 - Typical source-drain diode forward voltage.

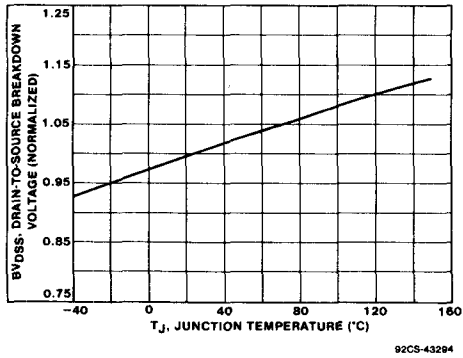


Fig. 8 - Breakdown voltage vs. temperature.

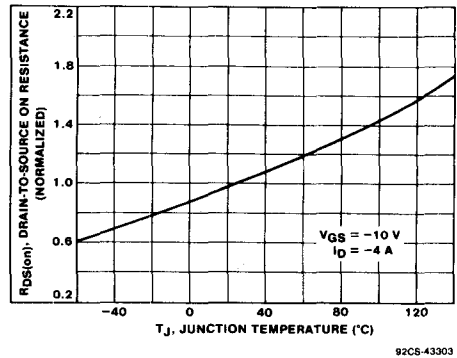


Fig. 9 - Normalized on-resistance vs. temperature.

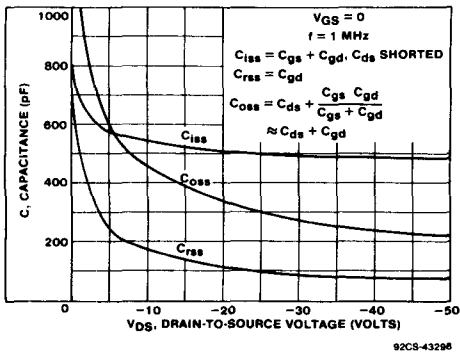


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

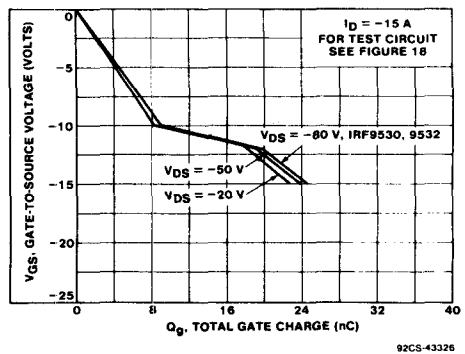


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRF9530, IRF9531, IRF9532, IRF9533

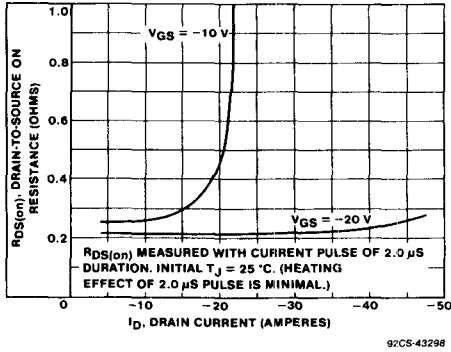


Fig. 12 - Typical on-resistance vs. drain current.

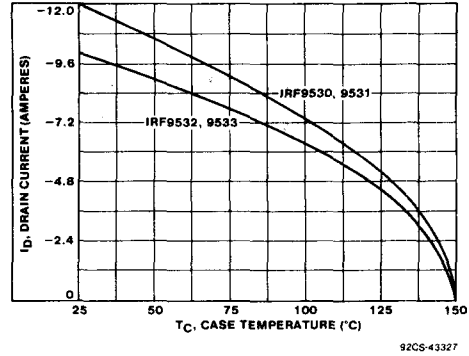


Fig. 13 - Maximum drain current vs. case temperature.

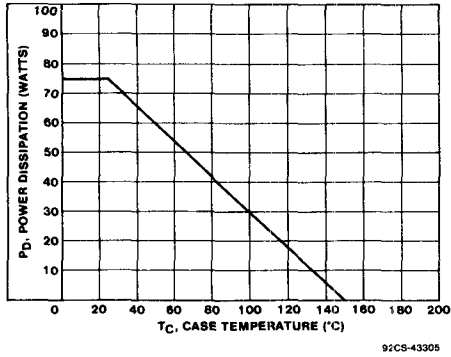


Fig. 14 - Power vs. temperature derating curve.

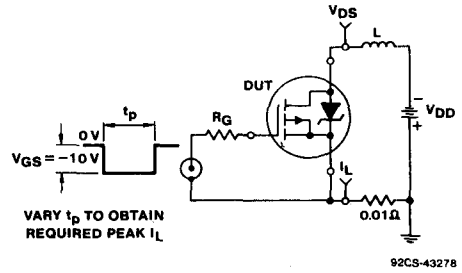


Fig. 15 - Unclamped inductive test circuit.

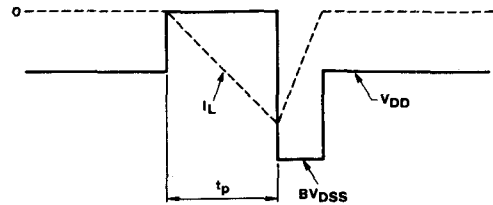


Fig. 16 - Unclamped inductive waveforms.

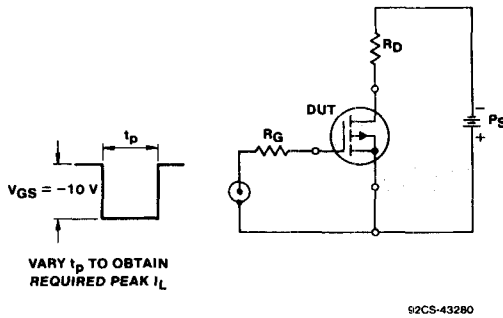


Fig. 17 - Switching time test circuit.

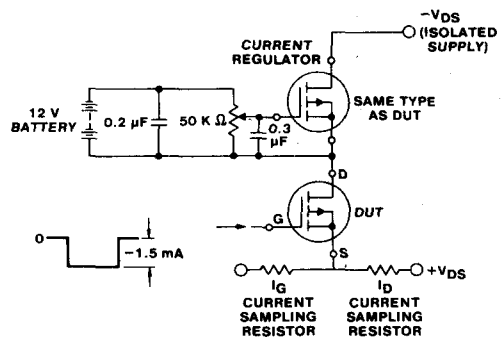


Fig. 18 - Gate charge test circuit.