

1-Mbit (64K × 16) Static RAM

Features

- Temperature Ranges:
 - Industrial: -40 °C to 85 °C
 - Automotive-A: -40 °C to 85 °C
- Pin and Function Compatible with CY7C1021B
- High Speed
 - t_{AA} = 10 ns
- Low Active Power
 - I_{CC} = 80 mA at 10 ns
- Low CMOS Standby Power
 - I_{SB2} = 3 mA
- 2.0 V Data Retention
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Independent Control of Upper and Lower Bits
- Available in Pb-free 44-pin 400 Mills Wide Molded SOJ and 44-pin TSOP II Packages

Functional Description

The CY7C1021D is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an

automatic power down feature that significantly reduces power consumption when deselected. The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

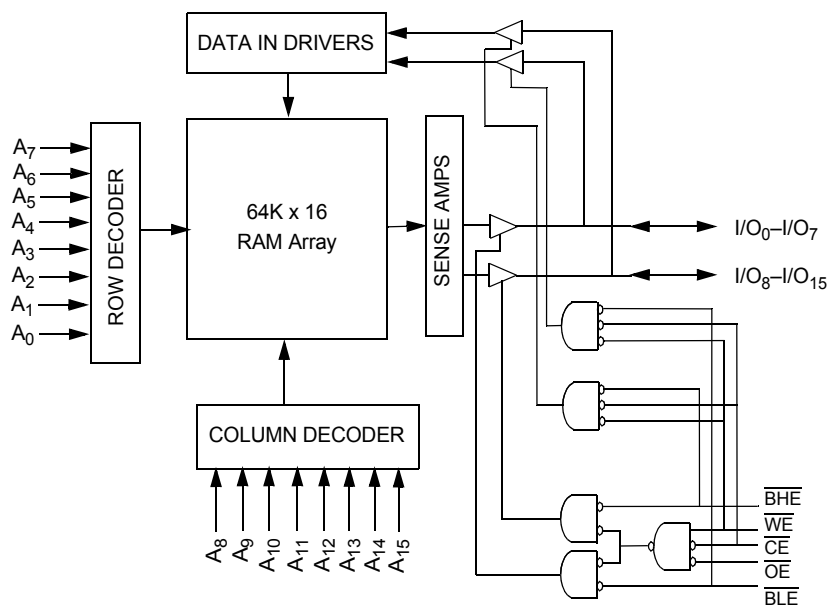
Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7 . If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the [Truth Table on page 10](#) for a complete description of read and write modes.

The CY7C1021D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Contents

Pin Configurations	3	Ordering Information	11
Selection Guide	3	Ordering Code Definitions	11
Maximum Ratings	4	Package Diagrams	12
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	17
Data Retention Characteristics	6	Worldwide Sales and Design Support	17
Data Retention Waveform	6	Products	17
Switching Characteristics	7	PSoC@Solutions	17
Switching Waveforms	8	Cypress Developer Community	17
Truth Table	10	Technical Support	17

Pin Configurations

Figure 1. 44-pin SOJ / 44-pin TSOP II pinout (Top View) ^[1]

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
I/O ₀	7	38	I/O ₁₅
I/O ₁	8	37	I/O ₁₄
I/O ₂	9	36	I/O ₁₃
I/O ₃	10	35	I/O ₁₂
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₄	13	32	I/O ₁₁
I/O ₅	14	31	I/O ₁₀
I/O ₆	15	30	I/O ₉
I/O ₇	16	29	I/O ₈
WE	17	28	NC
A ₁₅	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Selection Guide

Description	-10 (Industrial / Automotive-A)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	3	mA

Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature
with Power Applied -55 °C to +125 °C

Supply Voltage
on V_{CC} to Relative GND^[2] -0.5 V to +6.0 V

DC Voltage Applied to Outputs
in High Z State ^[2] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage ^[2] -0.5 V to $V_{CC} + 0.5$ V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) > 2001 V

Latch Up Current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	-40 °C to +85 °C	5 V $\pm$ 10%	10 ns
Automotive-A			

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial / Automotive-A)		Unit
				Min	Max	
V _{OH}	Output HIGH Voltage	I _{OH} = −4.0 mA		2.4	–	V
		I _{OH} = −0.1 mA		–	3.4 ^[3]	
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA		–	0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.5 V	V
V _{IL}	Input LOW Voltage ^[2]			−0.5	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		−1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled		−1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{max} = 1/t _{RC}	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I _{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V _{CC} , $\overline{\text{CE}} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{max}		–	10	mA
I _{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V _{CC} , $\overline{\text{CE}} \geq V_{CC} - 0.3 \text{ V}$, V _{IN} ≥ V _{CC} − 0.3 V, or V _{IN} ≤ 0.3 V, f = 0		–	3	mA

Note

- $V_{IL}(\text{min}) = -2.0$ V and $V_{IH}(\text{max}) = V_{CC} + 1$ V for pulse durations of less than 5 ns.
- Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

Capacitance

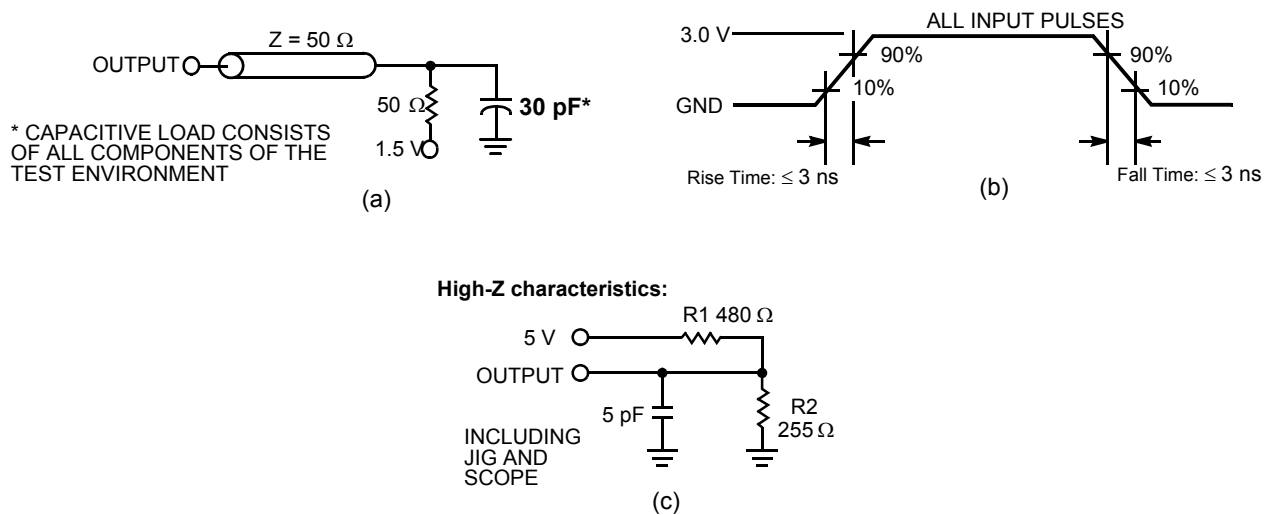
Parameter ^[4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[4]	Description	Test Conditions	44-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3×4.5 inch, four-layer printed circuit board	59.52	53.91	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		36.75	21.24	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[5]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

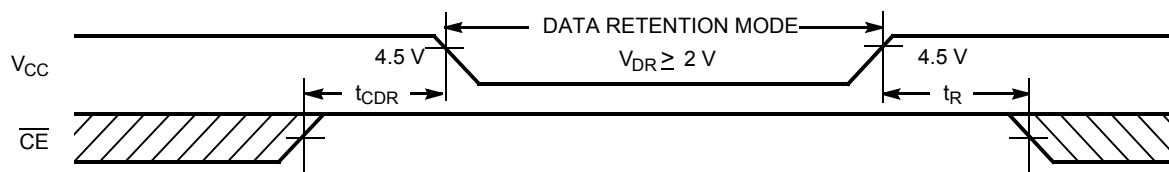
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0	–	ns
$t_R^{[7]}$	Operation Recovery Time		t_{RC}	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

6. $V_{IL}(\text{min}) = -2.0\text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 1\text{ V}$ for pulse durations of less than 5 ns.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 50\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 50\text{ }\mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[8]	Description	-10 (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t _{power} ^[9]	V _{CC} (typical) to the first access	100	–	μs
t _{RC}	Read Cycle Time	10	–	ns
t _{AA}	Address to Data Valid	–	10	ns
t _{OHA}	Data Hold from Address Change	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid	–	10	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid	–	5	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[10]	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[10, 11]	–	5	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[10]	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[10, 11]	–	5	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0	–	ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down	–	10	ns
t _{DBE}	Byte Enable to Data Valid	–	5	ns
t _{LZBE}	Byte Enable to Low Z	0	–	ns
t _{HZBE}	Byte Disable to High Z	–	5	ns
Write Cycle ^[12, 13]				
t _{WC}	Write Cycle Time	10	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	7	–	ns
t _{AW}	Address Setup to Write End	7	–	ns
t _{HA}	Address Hold from Write End	0	–	ns
t _{SA}	Address Setup to Write Start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	7	–	ns
t _{SD}	Data Setup to Write End	6	–	ns
t _{HD}	Data Hold from Write End	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[10]	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[10, 11]	–	5	ns
t _{BW}	Byte Enable to End of Write	7	–	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of [Figure 2 on page 5](#). Transition is measured when the outputs enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write, and a LOW to HIGH transition on any of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
13. The minimum write cycle pulse width for the Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

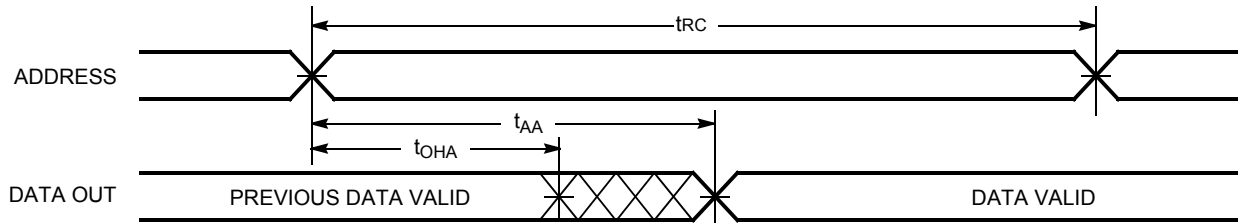
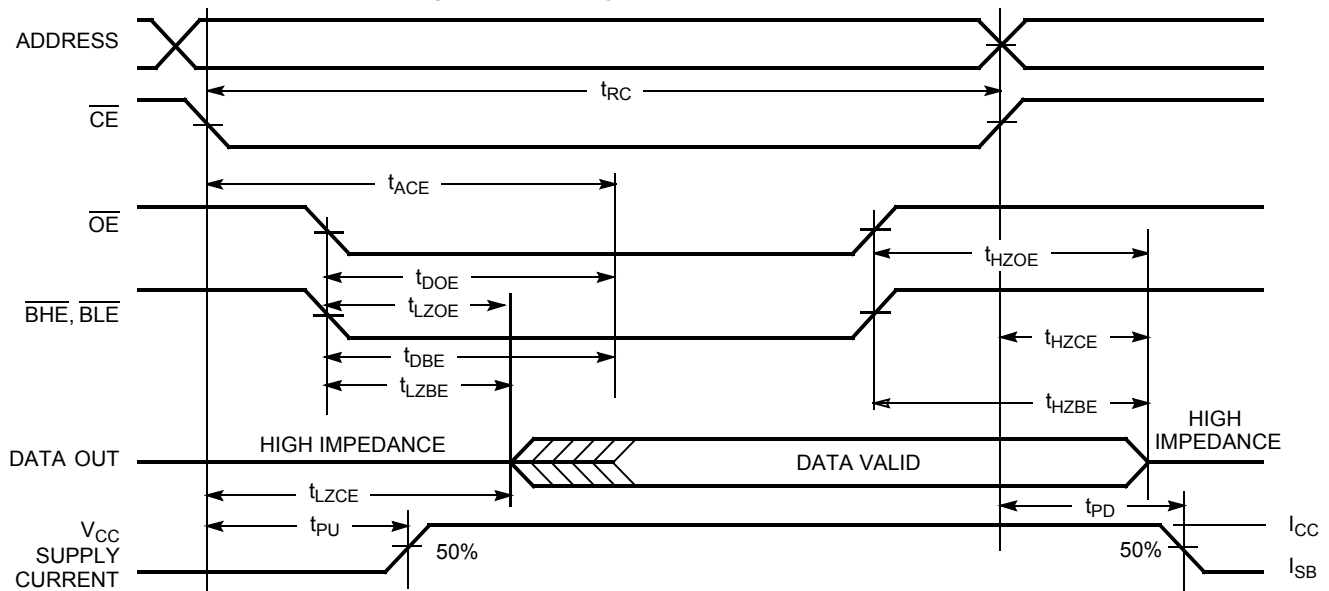


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16]



Notes

14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL} .
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [17, 18]

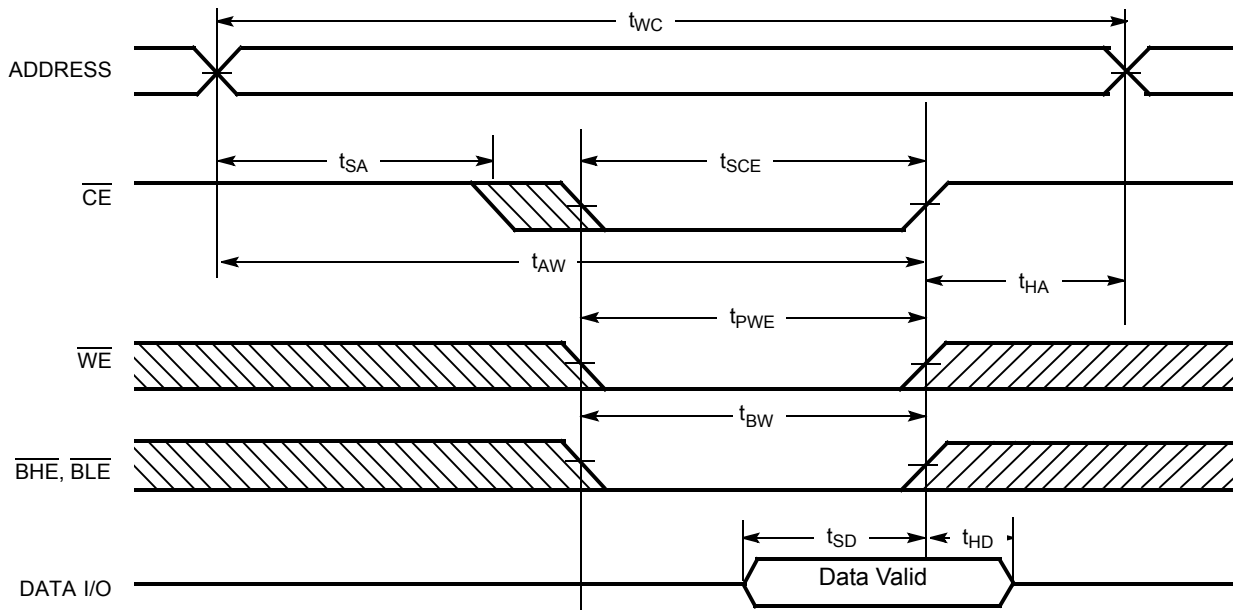
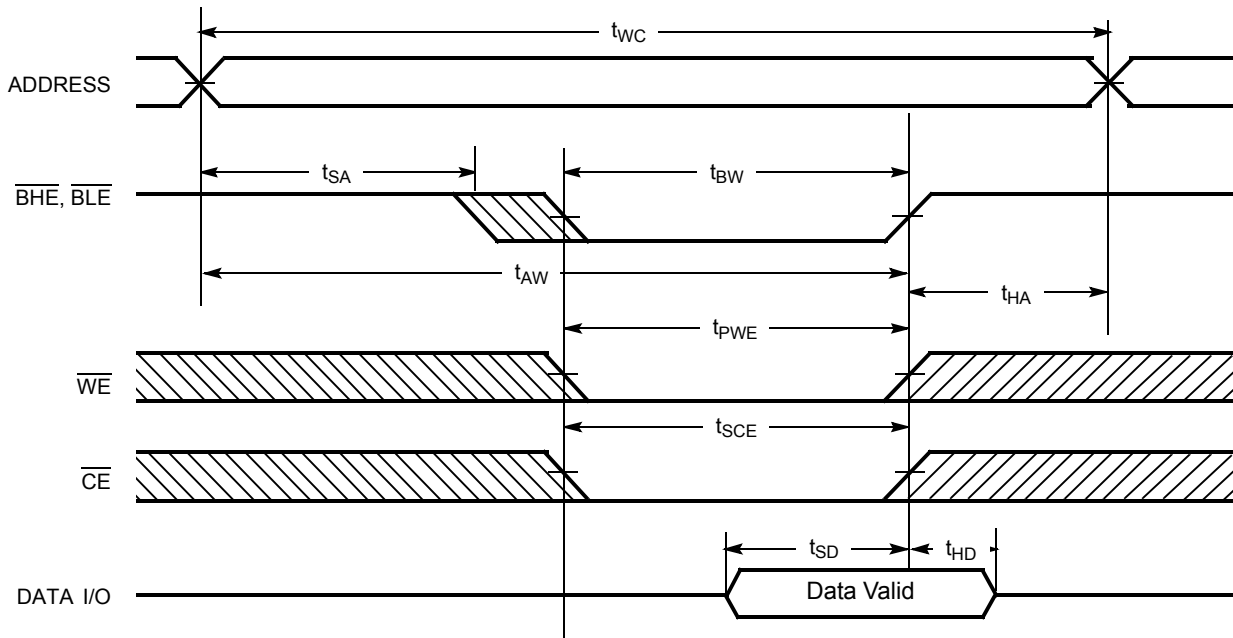


Figure 7. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



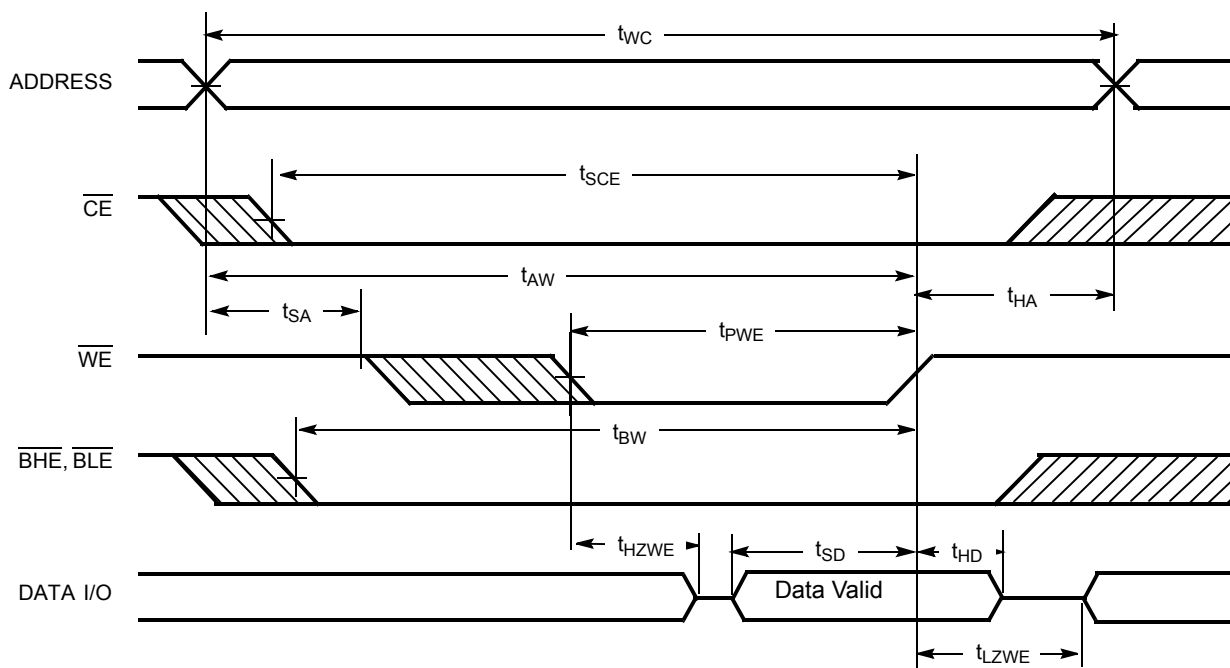
Notes

17. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.

18. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)



Truth Table

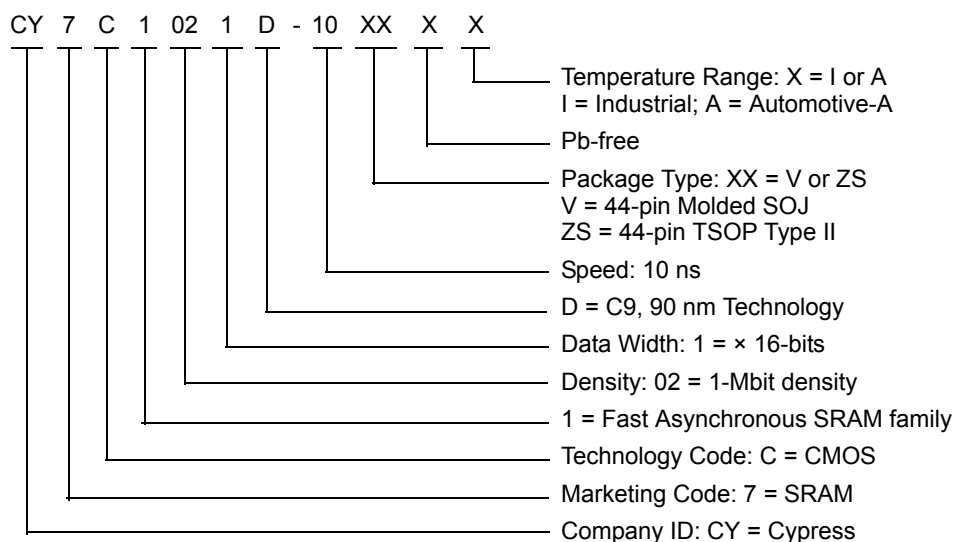
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021D-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1021D-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021D-10ZSXA			Automotive-A

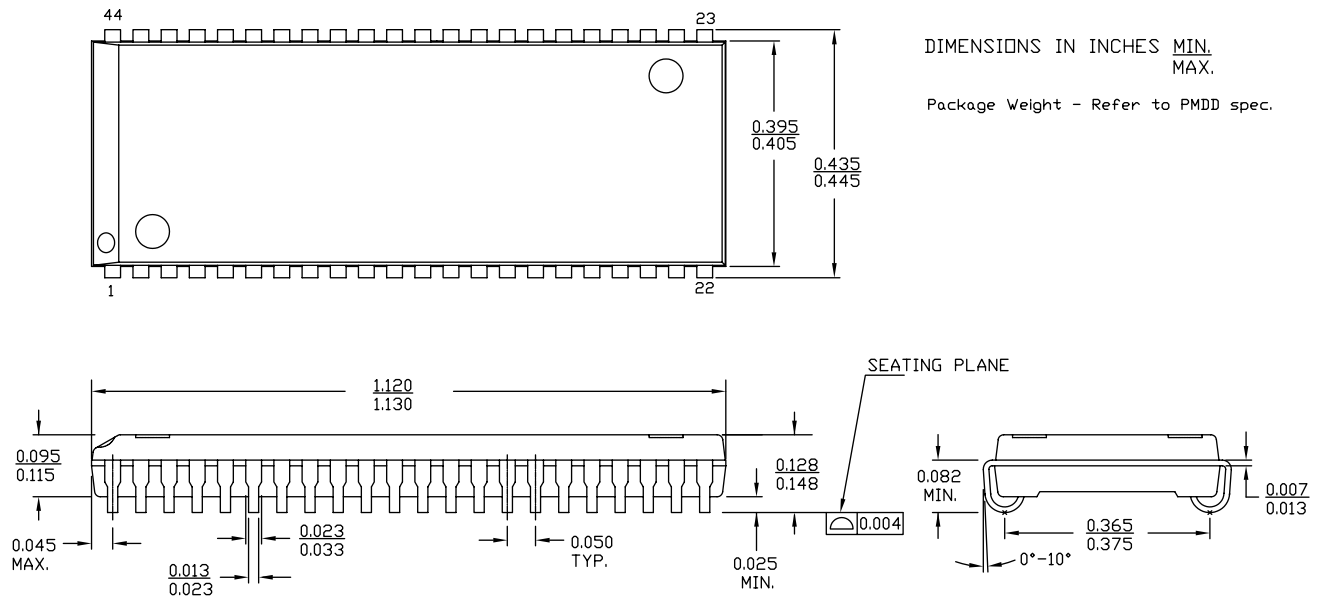
Shaded areas contain advance information. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

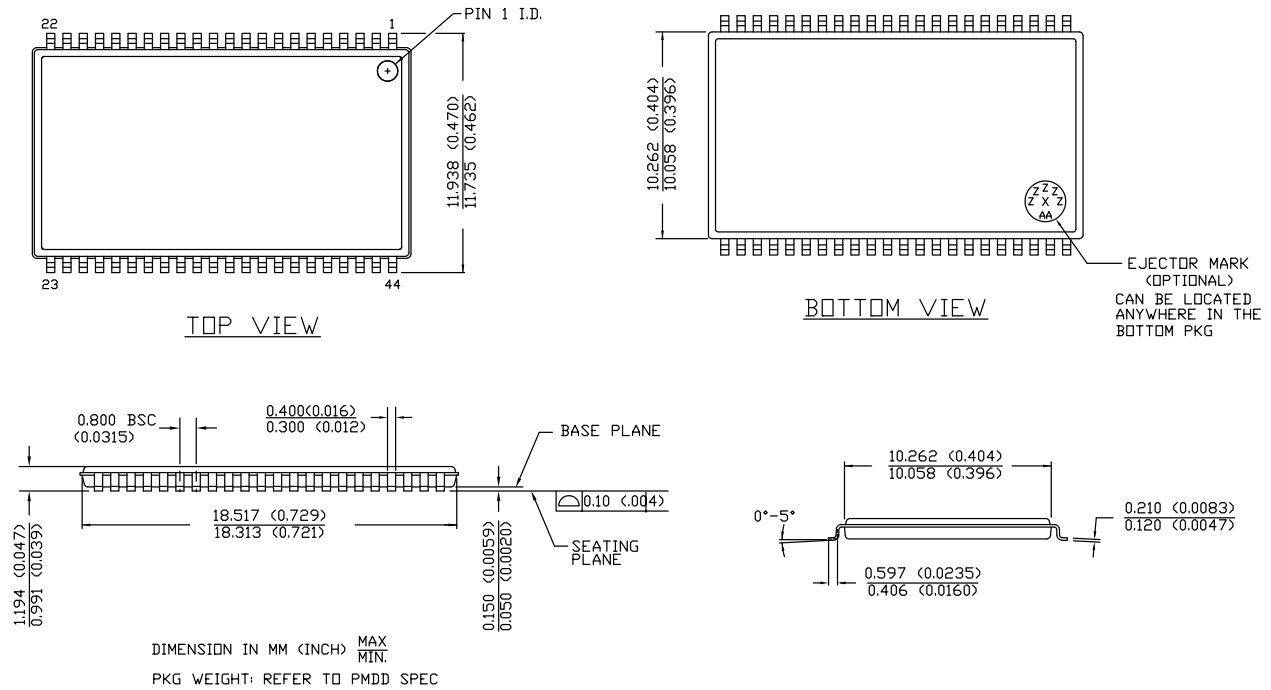
Figure 9. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



51-85082 *E

Package Diagrams (continued)

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021D, 1-Mbit (64K × 16) Static RAM Document Number: 38-05462				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance Information data sheet for C9 IPP
*A	233695	RKF	See ECN	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in the Ordering Information
*B	263769	RKF	See ECN	Added Data Retention Characteristics Table Added T _{power} Spec in Switching Characteristics Table Shaded Ordering Information
*C	307601	RKF	See ECN	Reduced Speed bins to –10 and –12 ns
*D	520647	VKN	See ECN	Changed status from Preliminary to Final. Removed Commercial Operating range Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Added Automotive Product Information Updated Ordering Information Table Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #4
*E	802877	VKN	See ECN	Changed Commercial operating range I _{CC} spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz Changed Automotive operating range I _{CC} spec from 100 mA to 120 mA for 83MHz, 90 mA to 100 mA for 66MHz, 60 mA to 63 mA for 40MHz
*F	2751755	VKN / PYRS	08/14/09	For 12 ns speed, changed I _{CC} spec from 120 mA to 90 mA For 12 ns speed, changed I _{SB1} spec from 50 mA to 10 mA and I _{SB2} spec from 15 mA to 10 mA
*G	2898399	AJU	03/24/2010	Updated Package Diagrams .
*H	3109897	AJU	12/14/2010	Added Ordering Code Definitions .
*I	3245199	PRAS	04/30/2011	Dislodged Automotive information to new datasheet (001-68372). Removed the Note “Automotive Product Information is Preliminary.” in page 3. Added Acronyms and Units of Measure . Updated to new template.
*J	3086499	AJU	06/07/2011	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”).
*K	3540685	TAVA / AJU	03/06/2012	Updated Features (Included Automotive-A Range information). Updated Selection Guide (Included Automotive-A Range information). Updated Operating Range (Included Automotive-A Range information). Updated Electrical Characteristics (Included Automotive-A Range information). Updated Switching Characteristics (Included Automotive-A Range information). Updated Ordering Information (included the part number CY7C1021D-10ZSXA). Updated Package Diagrams .
*L	3998493	MEMJ	05/13/2013	Replaced all instances of IO with I/O across the document. Updated Switching Characteristics : Updated Note 12. Updated Switching Waveforms : Updated Figure 6 , Figure 7 , Figure 8 . Updated Package Diagrams : spec 51-85082 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *D to *E. Completing Sunset Review.

Document History Page (continued)

Document Title: CY7C1021D, 1-Mbit (64K × 16) Static RAM Document Number: 38-05462				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*M	4033925	MEMJ	06/19/2013	Updated Functional Description . Updated Electrical Characteristics : Added one more Test Condition " $I_{OH} = -0.1\text{mA}$ " for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 3 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition " $I_{OH} = -0.1\text{mA}$ ".
*N	4573121	MEMJ	11/18/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end.
*O	5293980	VINI	06/02/2016	Updated Switching Characteristics : Added Note 13 and referred the same note in "Write Cycle". Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2004-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.